

Silicon Photo Multiplier Design Using Silicon on Insulator Technology

Tuesday, 27 November 2018 18:18 (2 minutes)

A 6×6 silicon photomultiplier (SiPM) array aimed at one-to-one coupling to a finely separated scintillator array was fabricated and characterized. All SiPMs were formed in the bulk substrate layer of a silicon on insulator (SOI) wafer for enabling future SiPMs which consists of 3-D integrated electronics without mechanical bump bonding. Each channel had a size of $250 \times 250 \mu\text{m}^2$ and was arranged for satisfying the counting-rate requirements of over 2 Mcps/mm^2 in energy-resolvable X-ray photon counting computed tomography (PCCT). In this study, the basic performance of SOI-SiPM prototype was characterized. Several features, such as a fast recovery time around 16 ns and a gain of 1×10^5 were within requirements to realize Photon counting computed tomography.

Primary authors: Mr KOYAMA, Akihiro (The University of Tokyo); Mr HAMASAKI, Ryutaro (The Graduate University for Advanced Studies); Prof. SHIMAZOE, Kenji (The University of Tokyo); Prof. TAKAHASHI, Hiroyuki (The University of Tokyo); Prof. TAKESHITA, Tohru (Shinshu University); Prof. KURACHI, Ikuo (High Energy Accelerator Research Organization); Prof. MIYOSHI, Toshinobu (High Energy Accelerator Research Organization); Prof. NAKAMURA, Isamu (High Energy Accelerator Research Organization); Prof. KISHIMOTO, Shunji (High Energy Accelerator Research Organization); Prof. ARAI, Yasuo (High Energy Accelerator Research Organization)

Presenter: Mr KOYAMA, Akihiro (The University of Tokyo)

Session Classification: Poster session