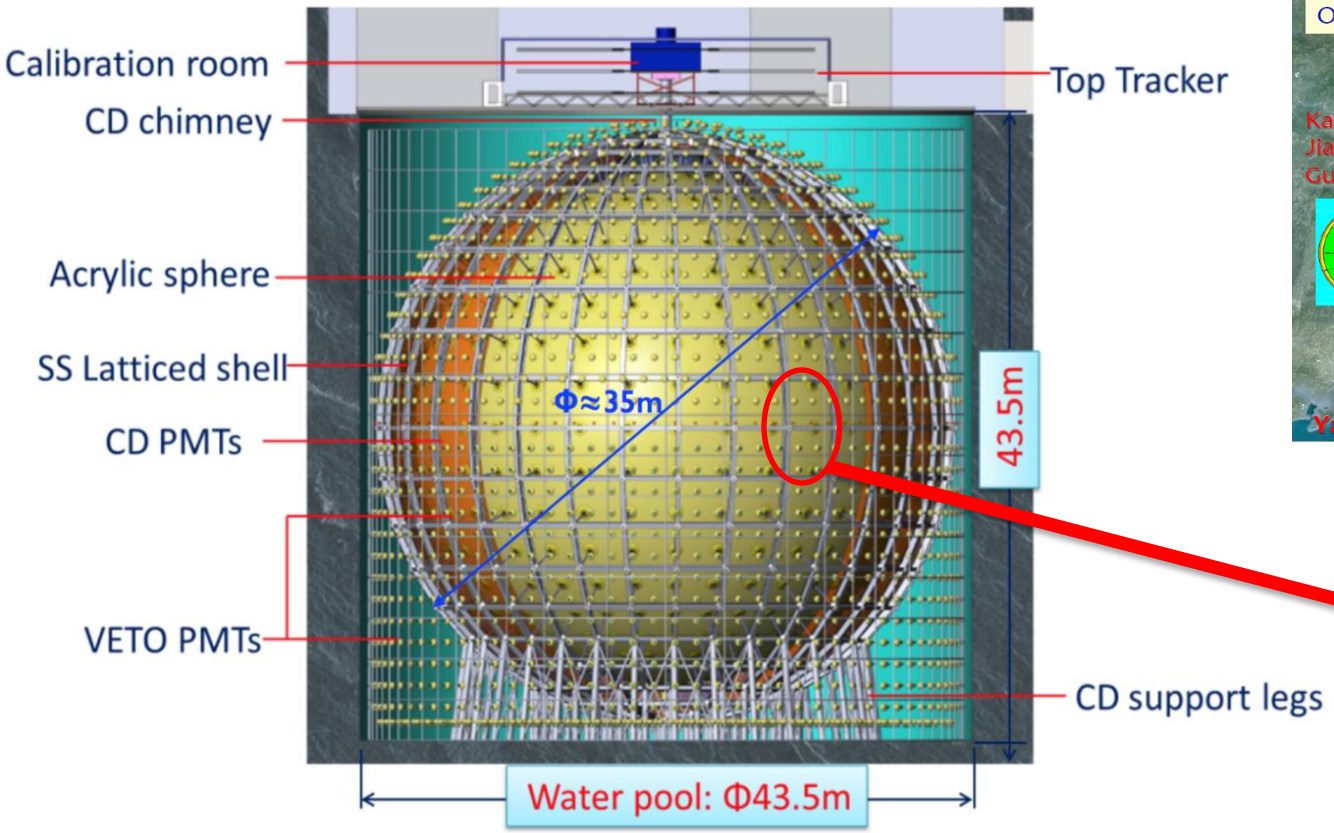
CATIROC : smart readout ASIC for JUNO SPMT

S. BLIN, S. CONFORTI, C. de LA TAILLE, F. DULUCQ, G. MARTIN-CHASSARD

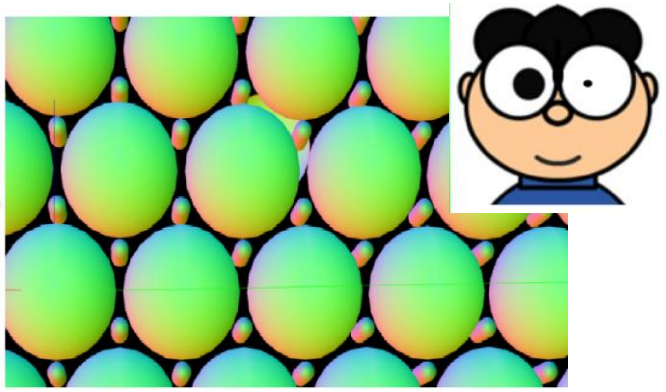
JUNO (Jiangmen Underground Neutrino Observatory)

A multipurpose **neutrino experiment** designed to determine neutrino mass hierarchy with a **20,000 tons liquid scintillator detector** at 700-meter deep underground



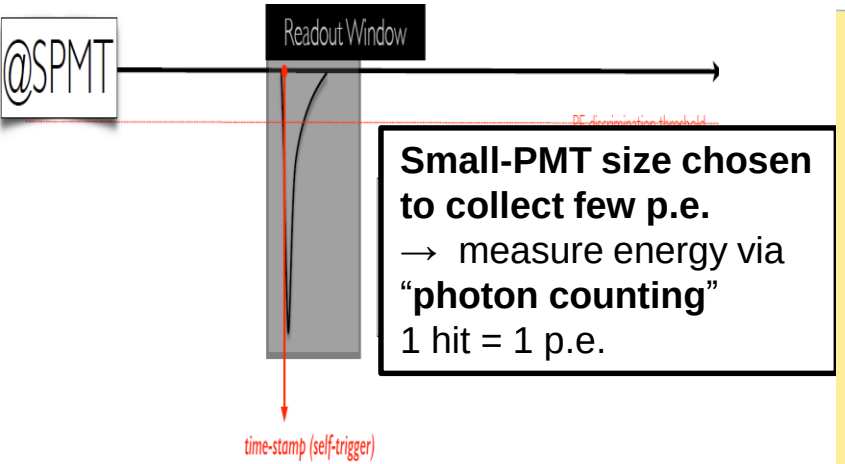
Schedule

Civil engineering: 2013-2014
Civil construction: 2014-2017
Detector component production: 2016-2017
PMT production: 2016-2019
Detector assembly & installation: 2018-2019
Filling & data taking: 2020

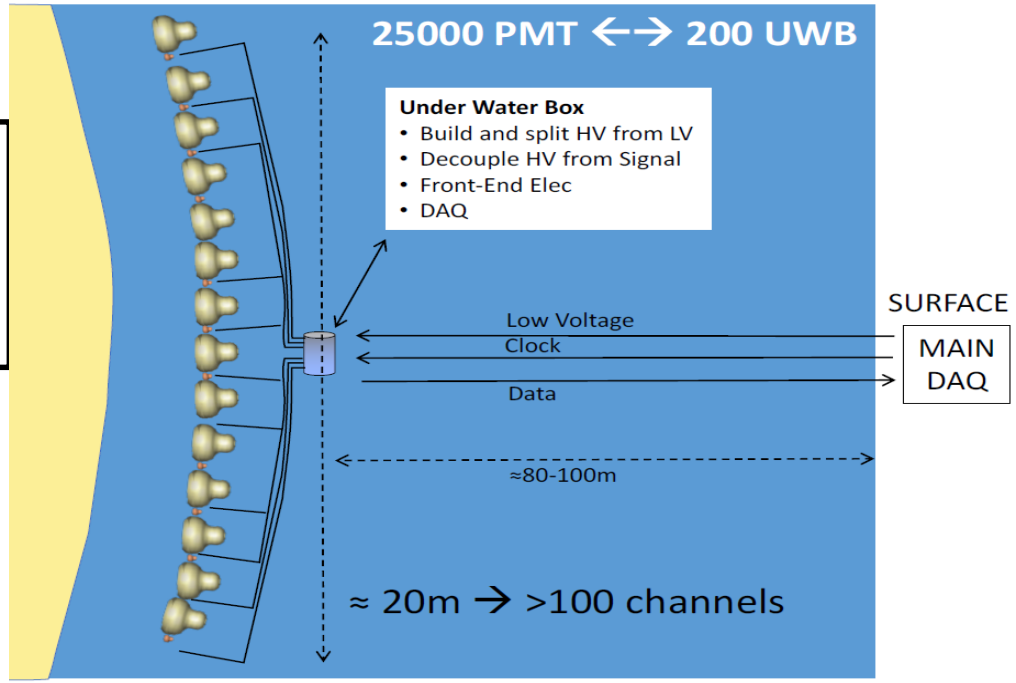


~ 18,000 PMTs (20” diameter) → Large-PMT system (LPMT) → **75 % of the inner surface**
~ 25,000 PMTs (3” diameter) → Small-PMT system (SPMT) → Increase coverage of the surface → Improve energy reconstruction
Cross calibration

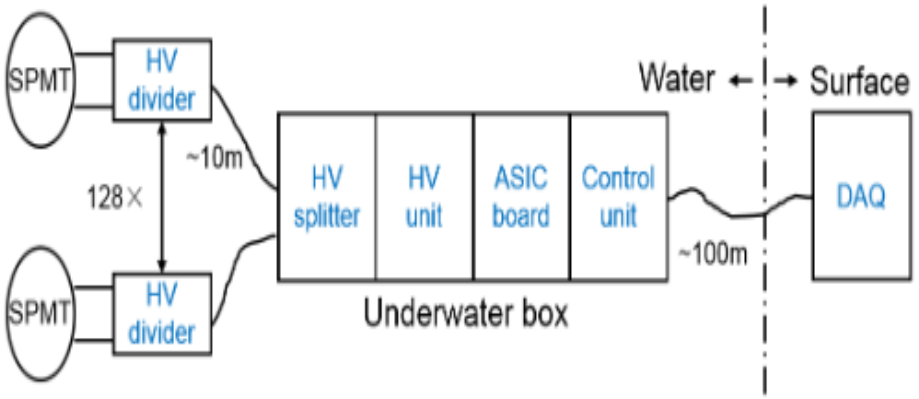
Small PMT (SPMT) system



Small-PMT size chosen to collect few p.e.
→ measure energy via "**photon counting**"
1 hit = 1 p.e.



HZC Photonics (XP72B22)
Production rate: 2000/month
Gain (at JUNO): 3 10^6
QE x CE (at 420nm): 24%
SPE Resolution: 35%
Dart Rate at ¼ PE: 1kHz
Transit Time Spread: 5ns

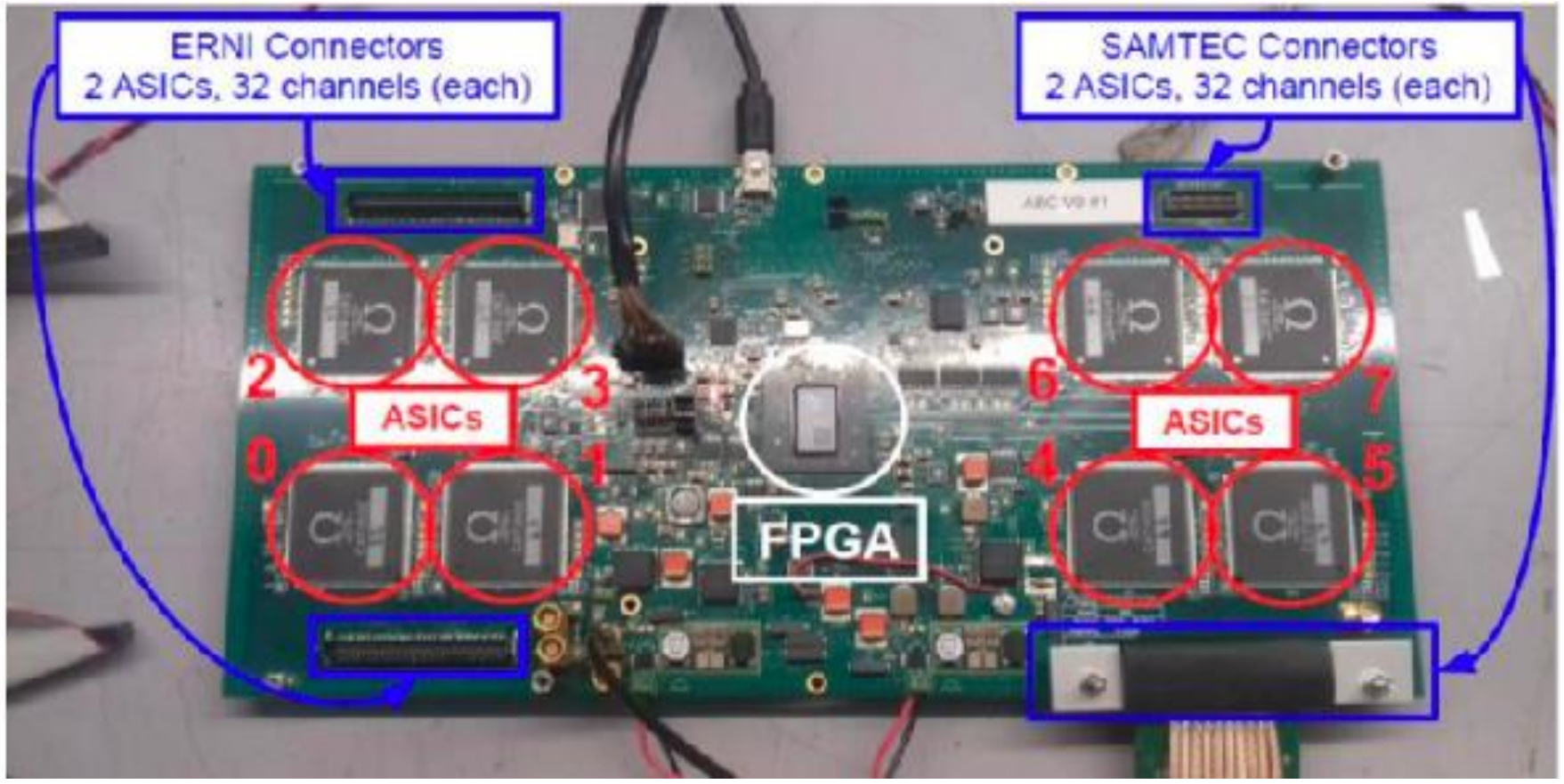


- **Small PMT : single photon counting mode**
- **128 Small PMTs** with a read-out system: **the Under Water Box (UWB)**
- Control Unit: Same board as LPMT system
- A dedicated FEB based **8 CATIROCs:**
  - Auto trigger
  - Gain variable (HV non uniformity correction)

Small PMT front-end board

- SPMT front-end with **8 ASIC CATIROC** each of 16 channels
- **FPGA** (Kindex 7 425-T)+ 2GB DDR3 **RAM memory** (large storage and processing on board)
- **4 connector (2 ERNI, 2 SAMTEC)** x 32 signals (CATIROC inputs)
- Power supply for ASIC and FPGA
- Low cost concept (**one board/ 128 PMTs/** one under water cable to send out data)

=> Test ongoing



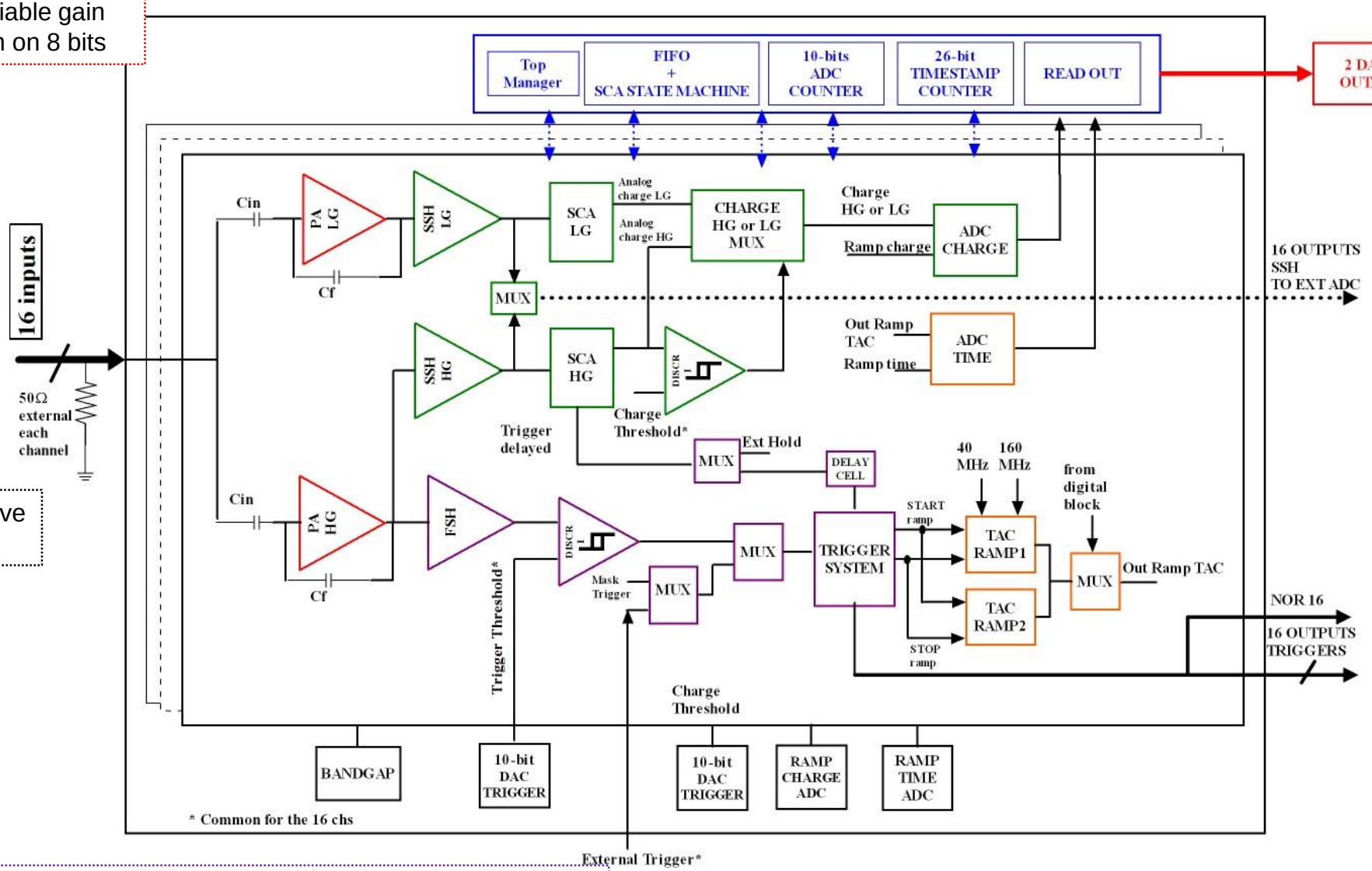
CATIROC for JUNO

A complex System on Chip (SoC). Technology: 0.35 µm SiGe AMS

CATIROC general features	Application to JUNO
16 independent channels	**Reduce the number of electronic** board (only 200 boards for 25,000 SPMTs)
Analog F.E. with **16 trigger outputs** + **charge and time digitization**	**Single Photon counting** + **charge and time measurements**. Resolutions very good
Autotrigger mode: all the PMTs signals above the threshold (1/3 p.e.) generate a trigger and are converted in digital data	Simplify online-DAQ
100% trigger efficiency @ 1/3 p.e.	**Good 1 p.e. detection** photon counting mode
Dual gain front-end: HG and LG channel Charge dynamic range 0 to 400p.e. (at PMT gain 10^6)	Only **HG** actually used (only few p.e. expected)
Time stamping (resolution ~ 170 ps rms)	< **1 ns required**
Each channel has a **variable gain**	**To compensate gain vs HV spread** for the 16 PMTs
One output for **DATA**	**Less number of cables to the surface**
Hit rate 100 kHz/ch (all channels hit) **50 bits of data / hit channel**	**Very "light" data output** (compared to a FADC waveform)

CATIROC schematic: 16 channel totally independent

Amplification stage
with variable gain
ch by ch on 8 bits



16 negative inputs

DATA: Charge and Time measurement

Charge path

- Shaping (variable shaping time)
- Switched capacitor array (**2 Capacitors: ping-pong mode)**
- 10 bits ADC conversion @ 160 MHz

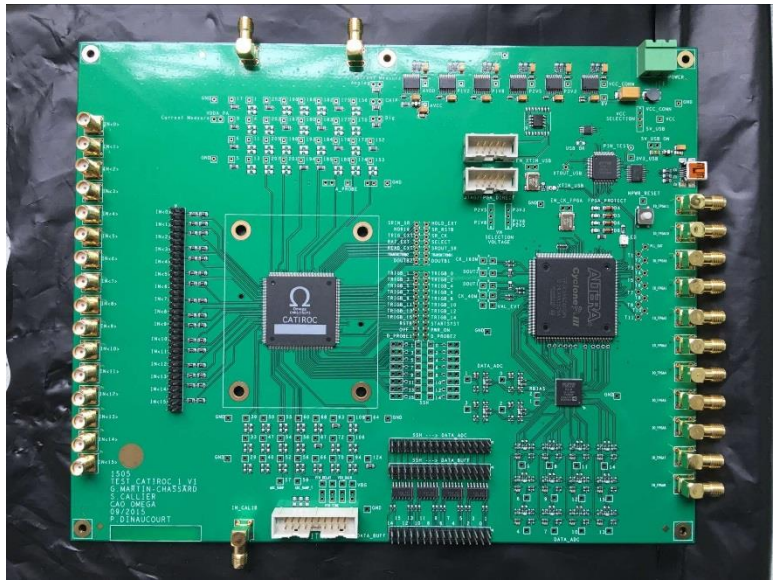
Time:

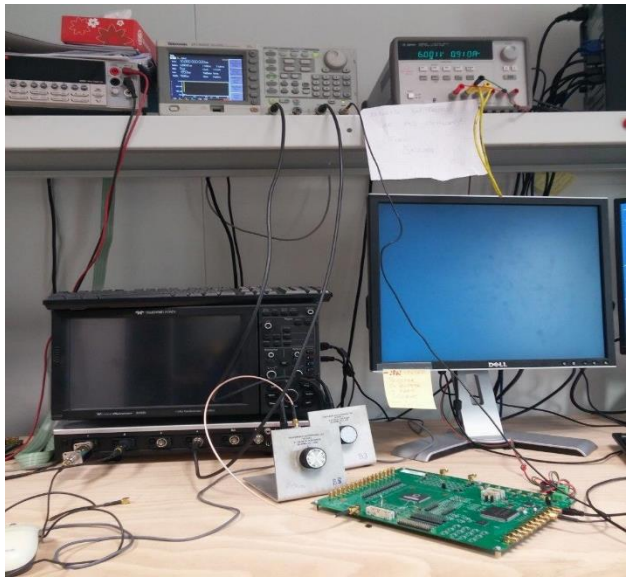
Coarse time: 40MHz counter

Fine time: Time Amplitude Converter

Trigger path: AUTO TRIGGER DESIGN

CATIROC performances





Chip status:

Submission: **February 2015**

Received: July 2015

Process: **AMS 0.35 µm SIGe**

Die dimensions: 3.3 mm x 4 mm (13.2 mm²)

Packaging: **TQFP208**

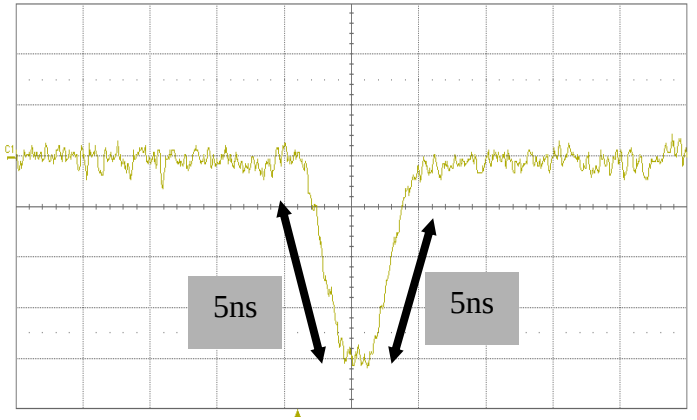
Power Supply: 3.3V

Dissipation: **20mW/ch** on 3.3 V

Clocks: 40 MHz (Coarse time) and 160 MHz (Conversion)

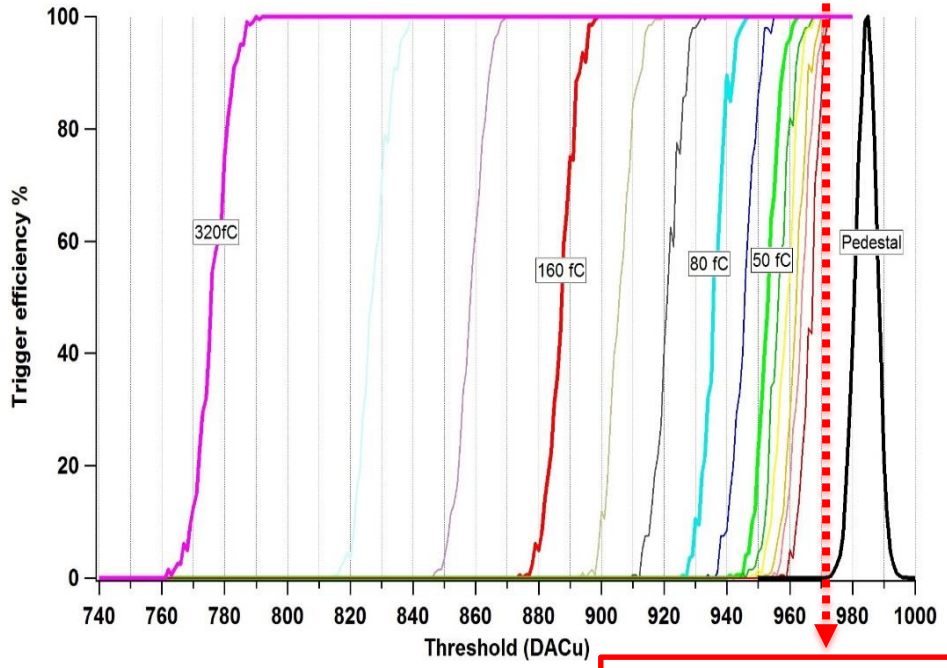
The input signal is made by a pulse generator signal: a negative voltage pulse (rise time= 5ns, fall time= 5ns, width= 10 ns, Amplitude @1 p.e.~ 0.8 mV).

The M.I.P. is 1 p.e.= 160 fC @ PMT gain 10^6

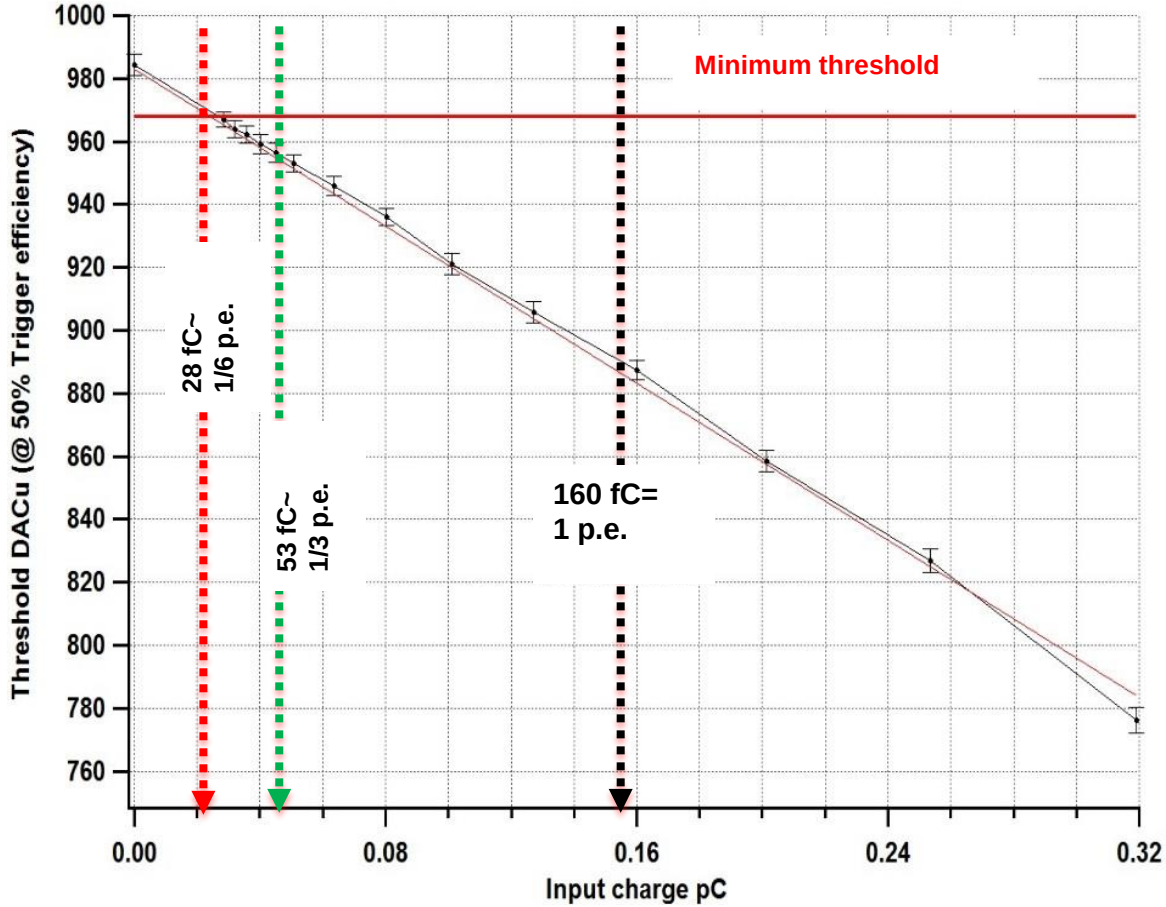


Trigger efficiency

The trigger efficiency is investigated by scanning the threshold (by the internal DAC) for a fixed channel and monitoring the discriminator response.



Minimum Threshold
@ 968 DACu ~ 28 fC **< 1/3 of pe**



1 p.e.= 160 fC @ PMT gain 10^6

DAC resolution: 0.6 DACu/fC

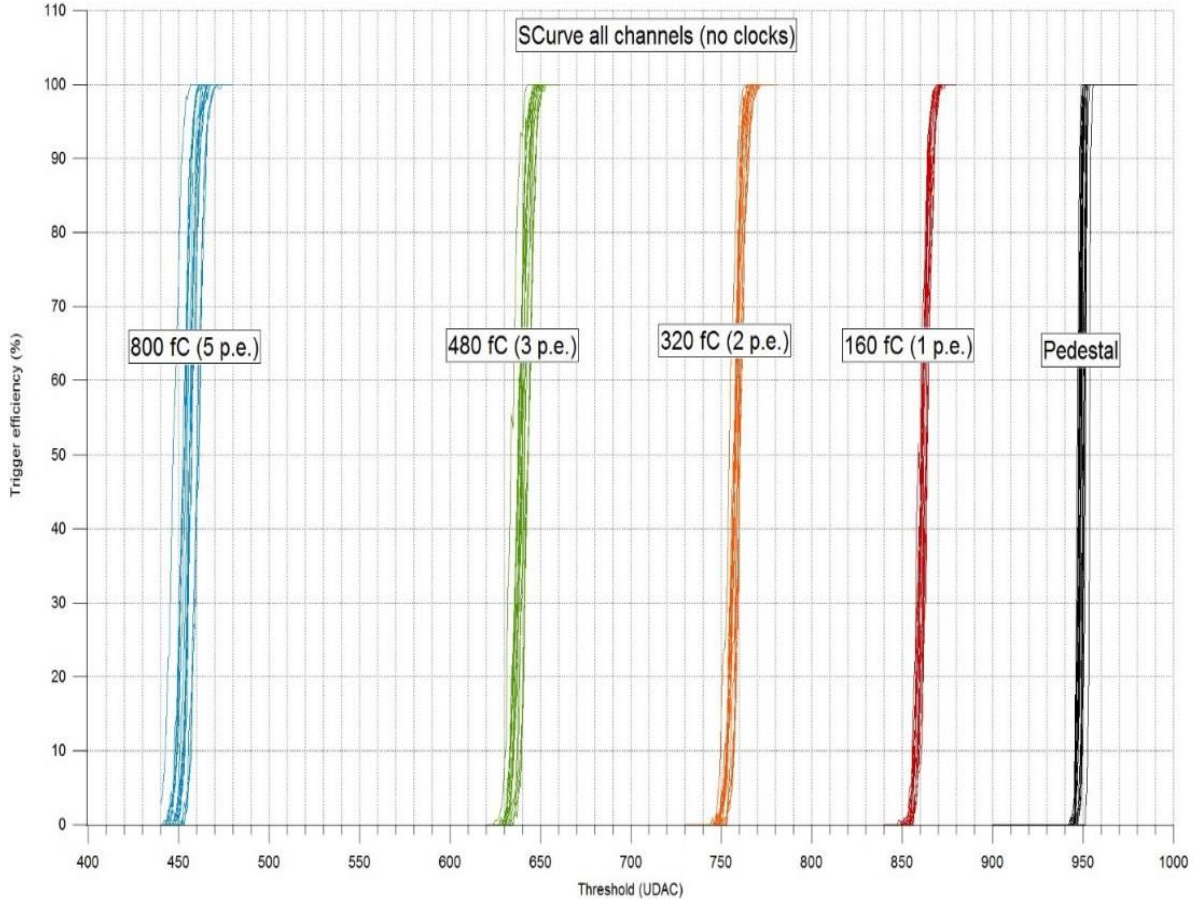
Sensitivity ~ 100 DACu/ p.e.

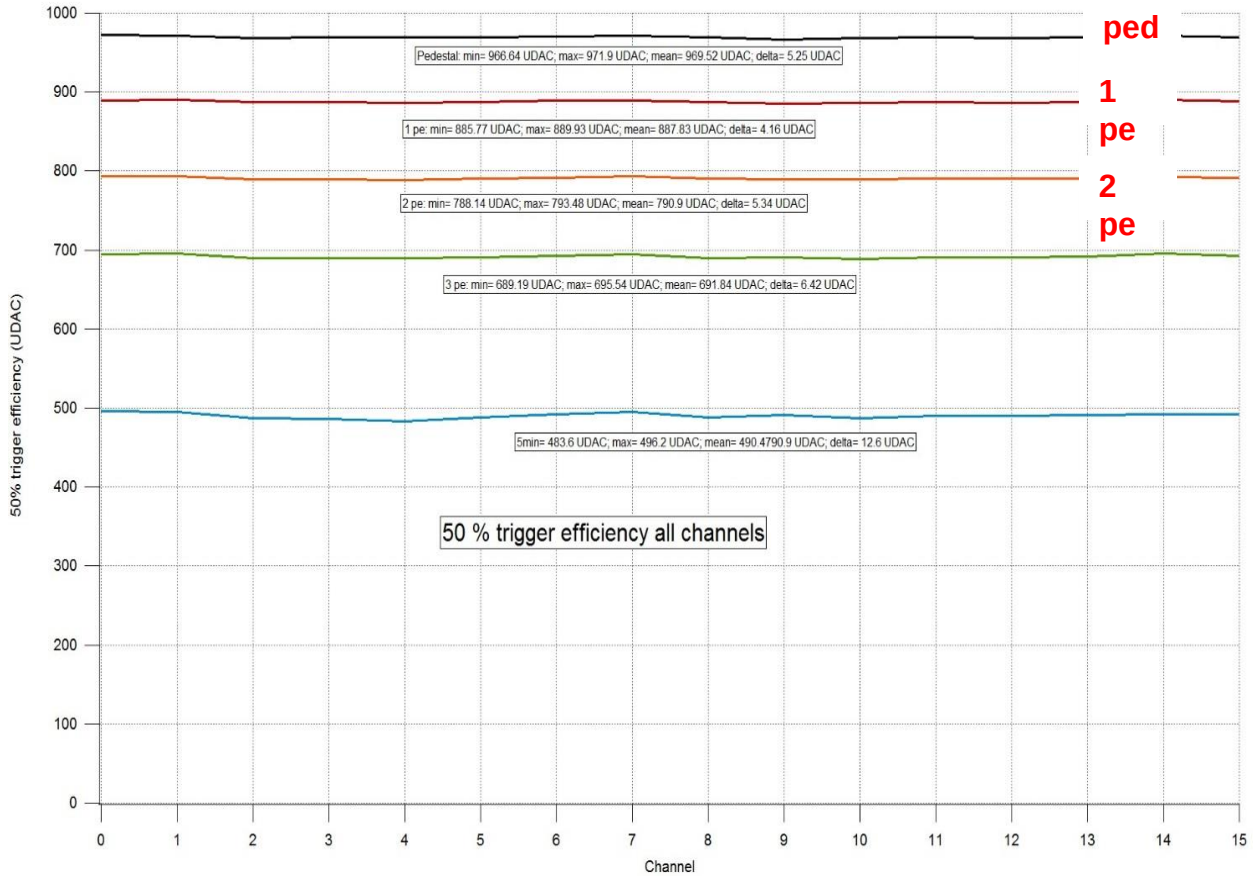
σ (noise)= 3.5 DACu= 5.6 fC

Pedestal= 984 DACu

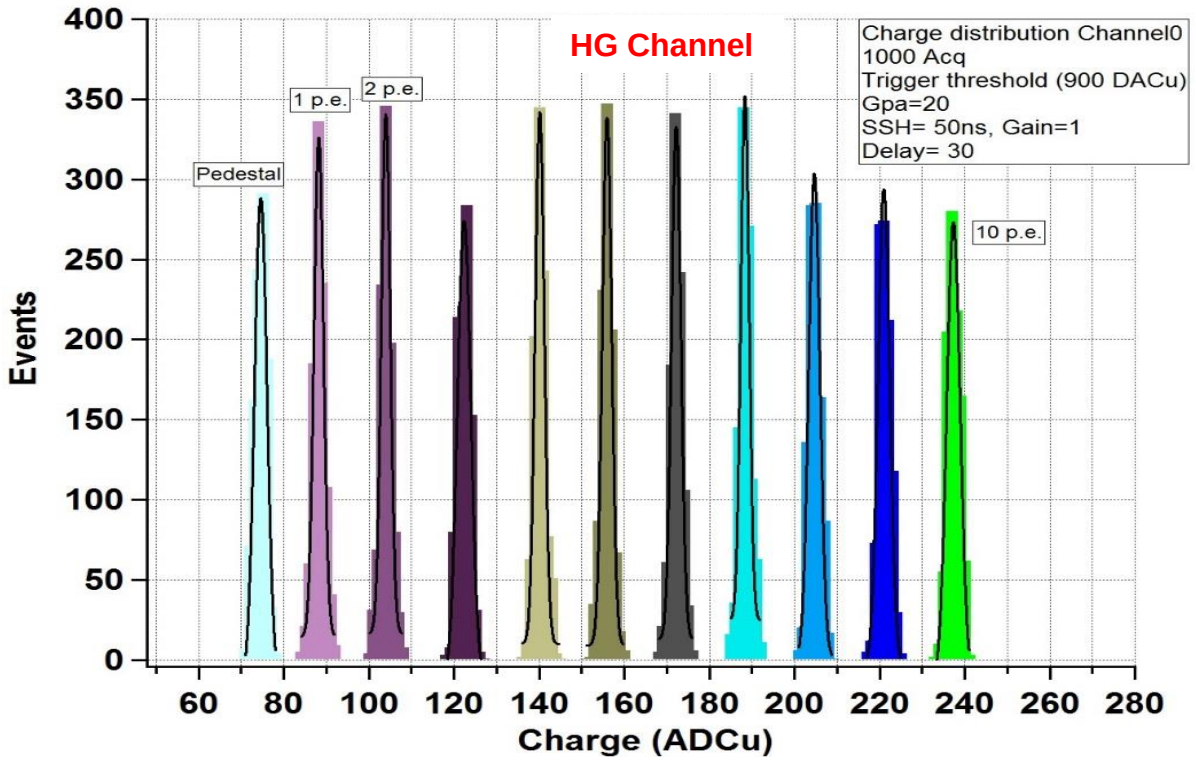
Minimum threshold= Pedestal mean value (DACu)- 5 σ (DACu)= 968 DACu (~ 28 fC)

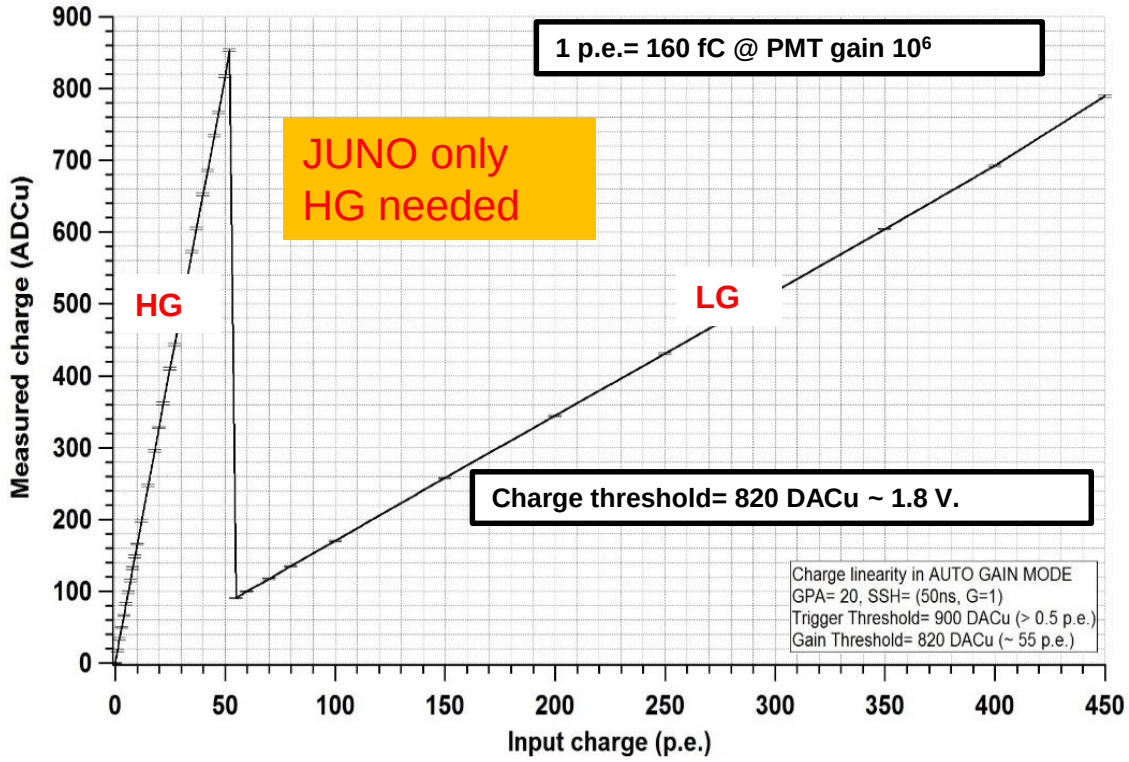
Scurves uniformity





Charge resolution and linearity





	HG charge performance	LG charge performance
Linearity residuals	< 0.7 % Up to 50 p.e.	< 1 % up to 400 p.e.
LSB	10 fC/ADCu → 16 ADCu/ 1 p.e.	80 fC/ADCu
Charge resolution	1.5 ADCu (HG) ~ **15 fC**	1.2 ADCu (LG) ~ 100 fC

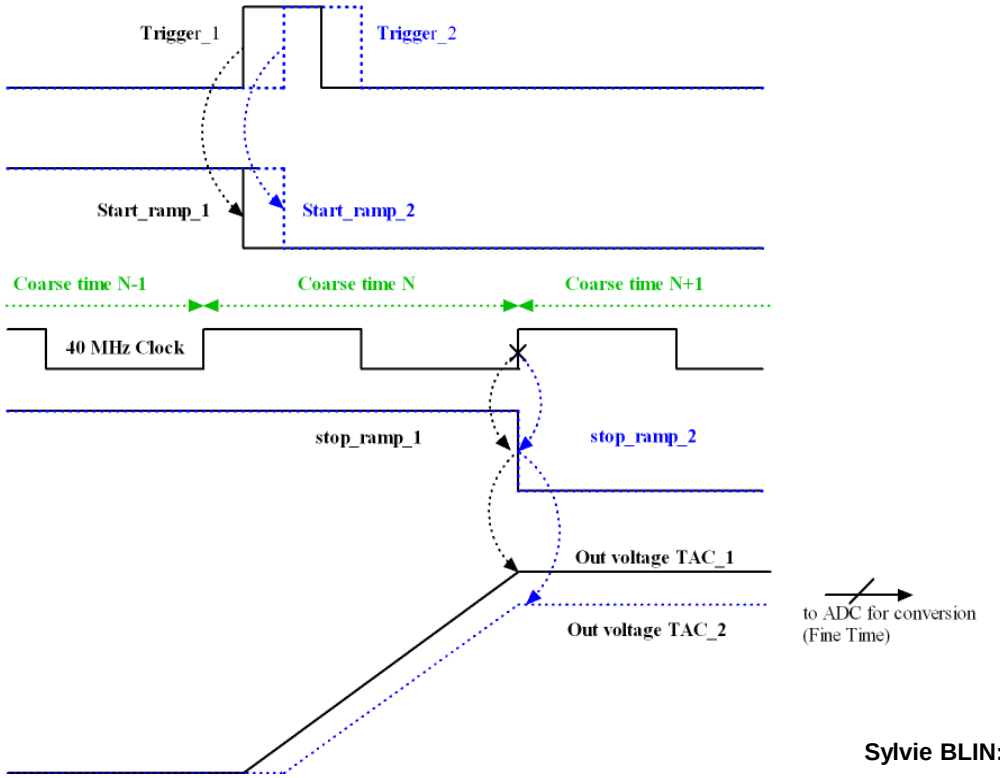
JUNO Application:
photon counting mode
=> only the HG path.

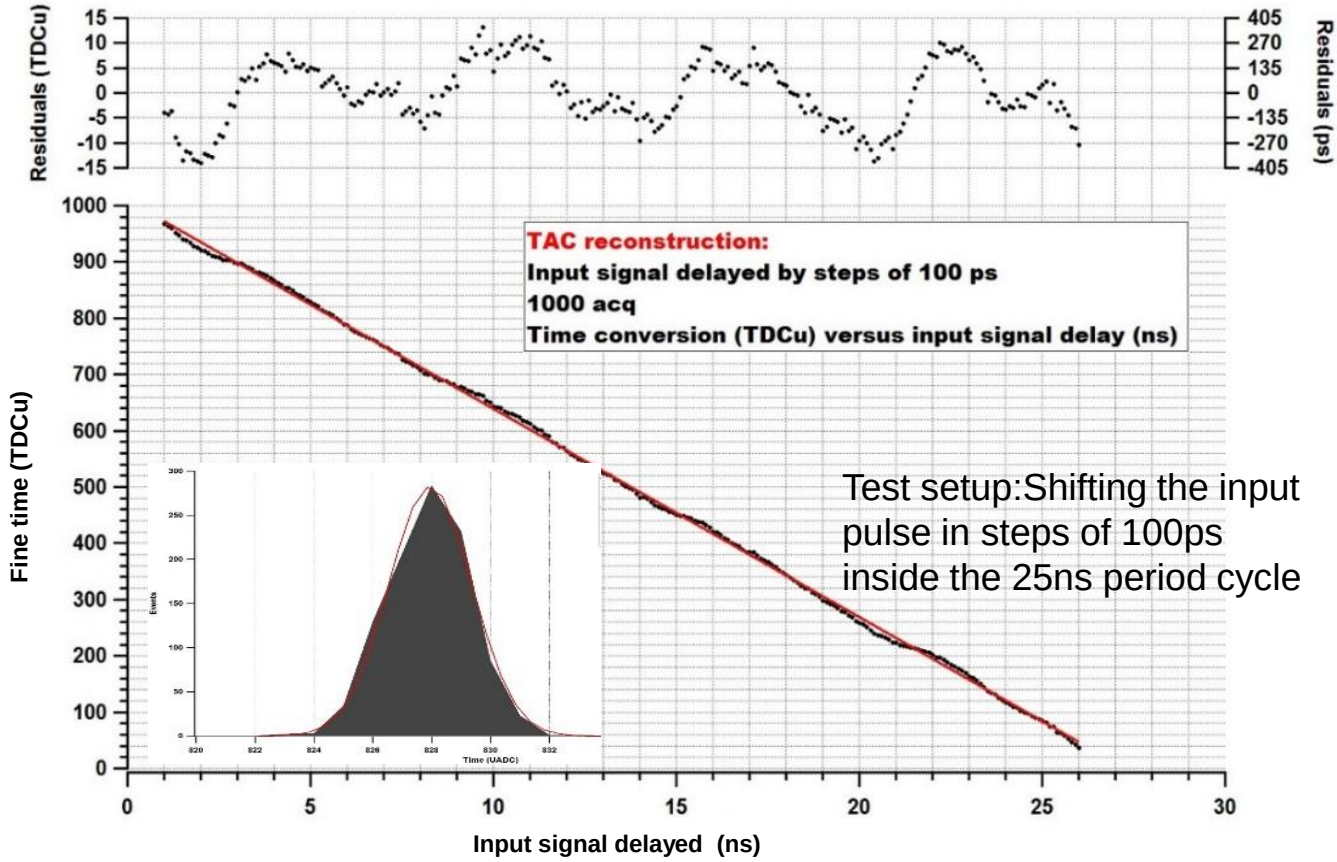
charge resolution and linearity are OK

Time measurements

The ASIC provides the signal “time of arrival” operating in self-triggered mode.
The time measurement is composed of two values:

- The “coarse time” (Timestamp)
  - 26-bit Gray Counter with a resolution of 25 ns
  - This time is saved in a 26-bit register when the channel has a trigger indicating a detected signal.
- The “fine” time
  - Two TAC ramps in each channel to reach 200ps resolution





Test setup:Shifting the input pulse in steps of 100ps inside the 25ns period cycle

TDC measurements: fine time (10 bits)

INL: [-375.3, 356.4] ps

TDC bin= 27 ps

TDC non linearity= 167 ps rms

TDC noise= 38 ps

Residuals dominated by 160 MHz clock coupling

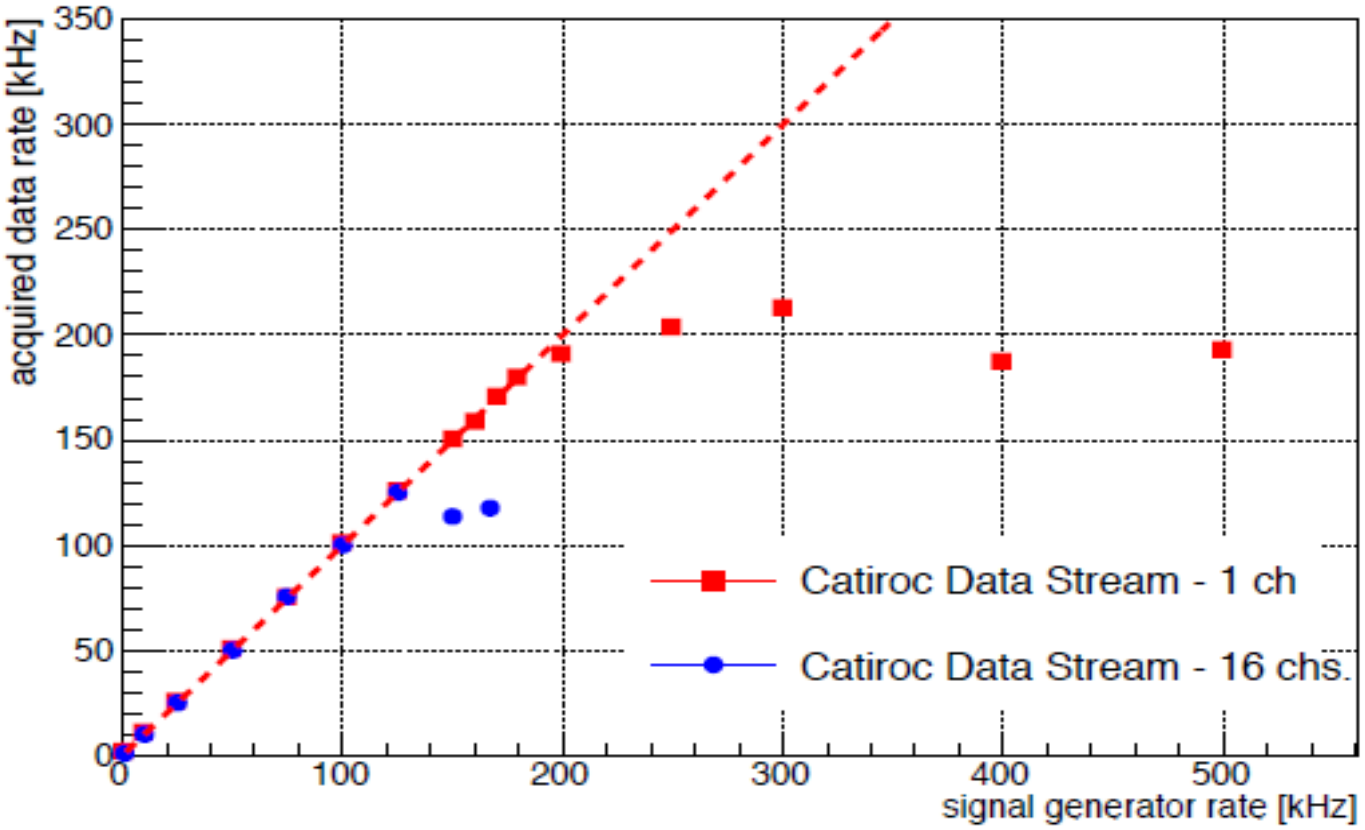
JUNO Application:
< 1ns

Hit rate measurements

HIT RATE			
Tconv (1 ch)	6.4 µs	Tconv (16 ch)	6.4 µs
Tread-out (1 ch)	0.36 µs	Tread-out (16 ch)	3 µs
Tcycle (1 ch)	6.8 µs	Tcycle (16 ch)	9.4 µs
Hit rate (1 ch)	150 kHz	**Hit rate (16 ch)**	100 kHz

The maximum conversion time $Tconv = \frac{2^n}{F_{conv}}$ = 6.4 µs

The maximum readout time $TimeRO = \frac{Nchannels\ x\ Nbits}{F_{\mathrm{RO}}}$



HIT RATE on CATIROC data output

Worst case (16 cannels): hit rate < 120kHz

=> acceptable for JUNO events

For some rare event case (supernova): too low

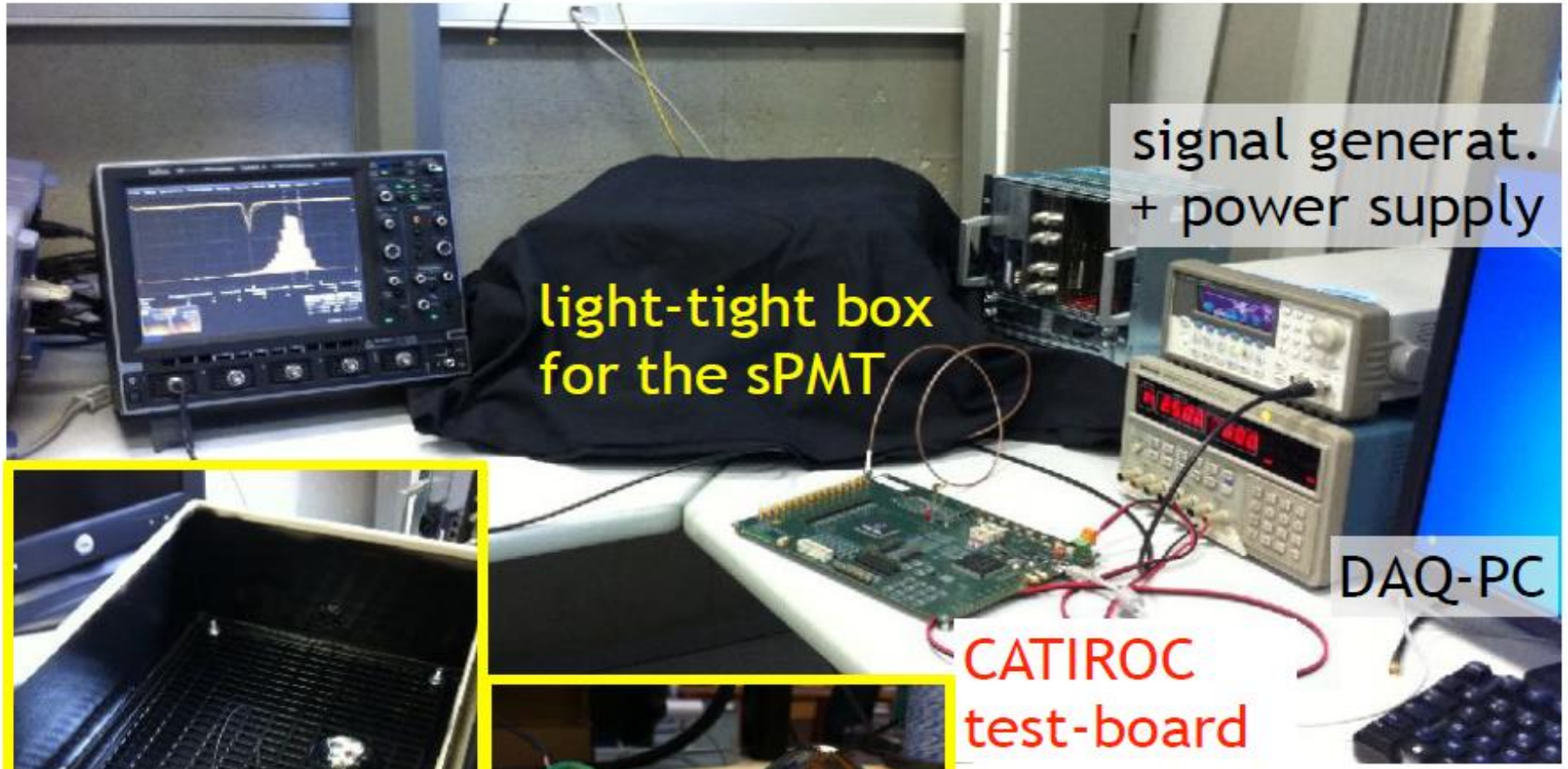
⇒ Photon counting with the 16 triggers

⇒ Photon counting double pulse

resolution= ~ 15MHz

JUNO: charge measurement + counter trigger

Test-bench @ Subatech Nantes



Test-bench @ Subatech

Top: *test-bench with sPMT and CATIROC test-board*

Bottom: *light-tight box and HZC-PMT*

light-tight box of 1m x 1m

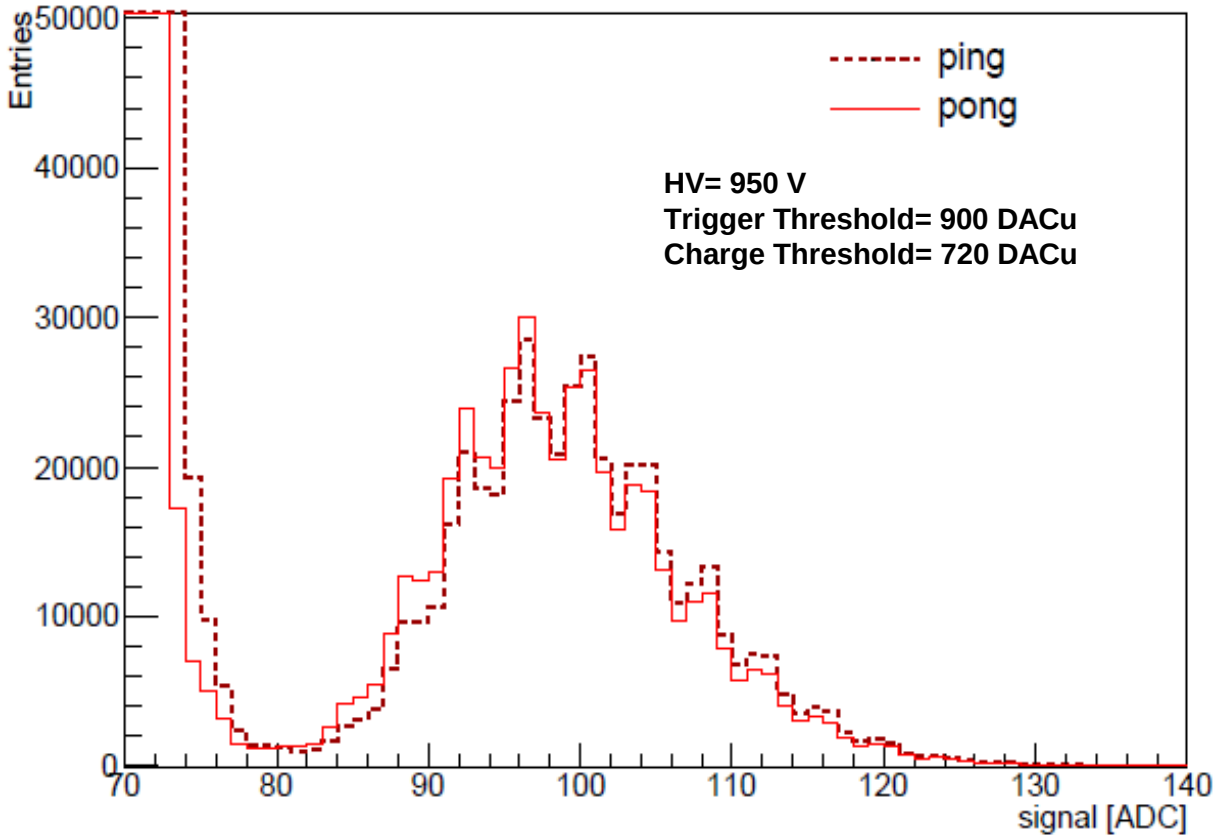
3" PMT HZC XP72B22

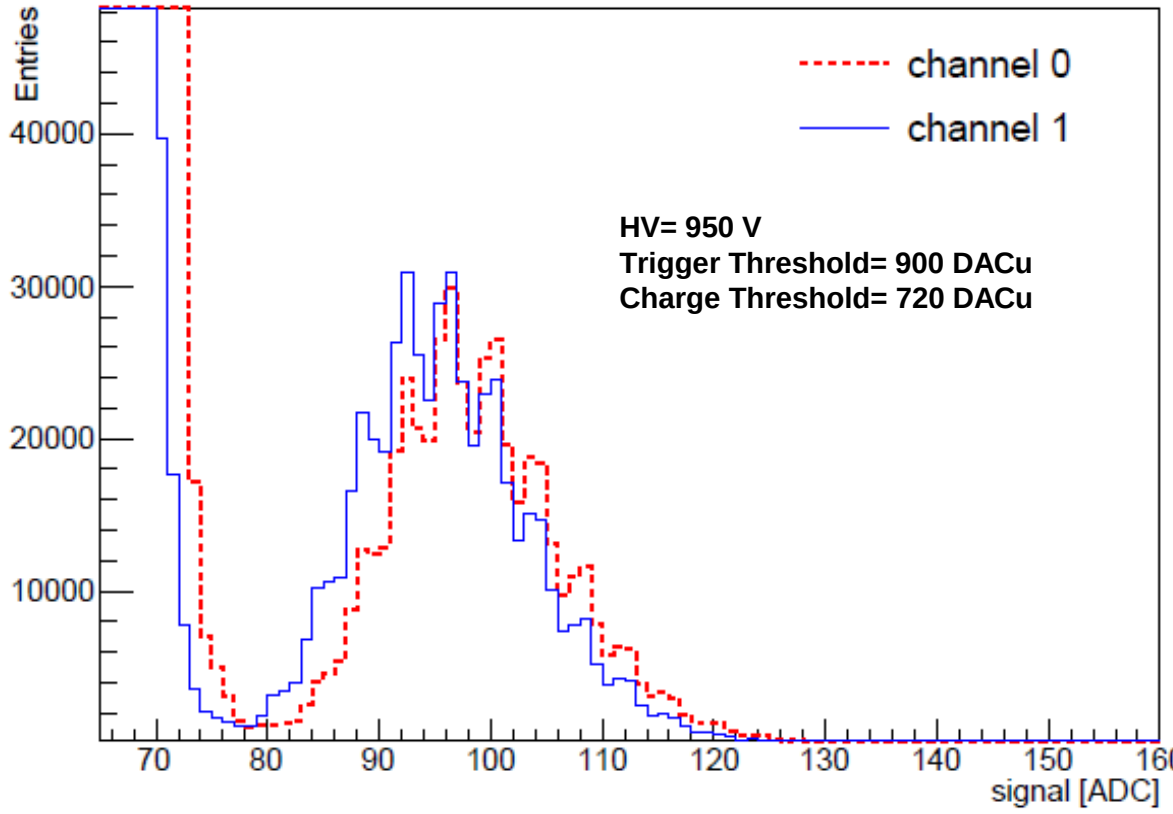
LED : λ=470 nm

Subatech

JUNO SPMT

Single p.e. with PMT + Catiroc



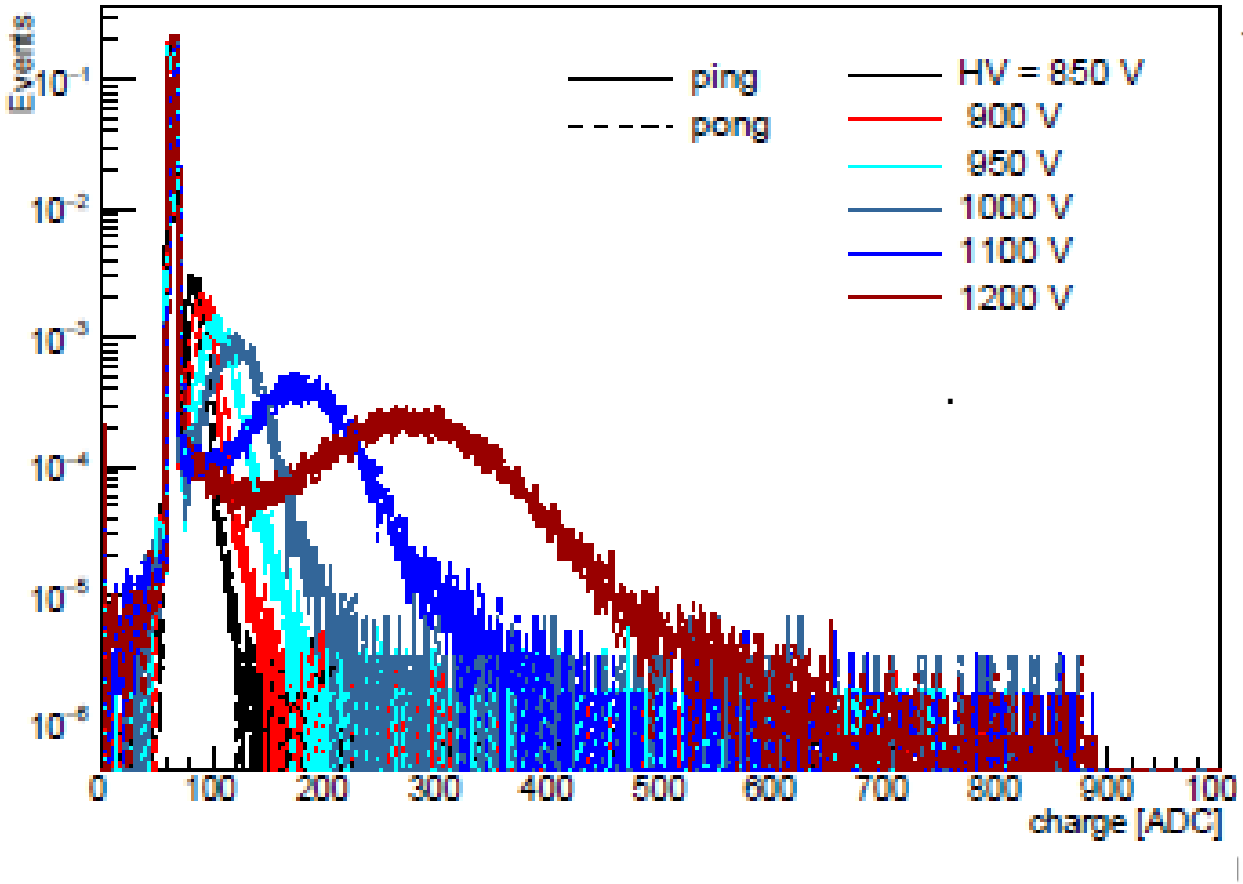


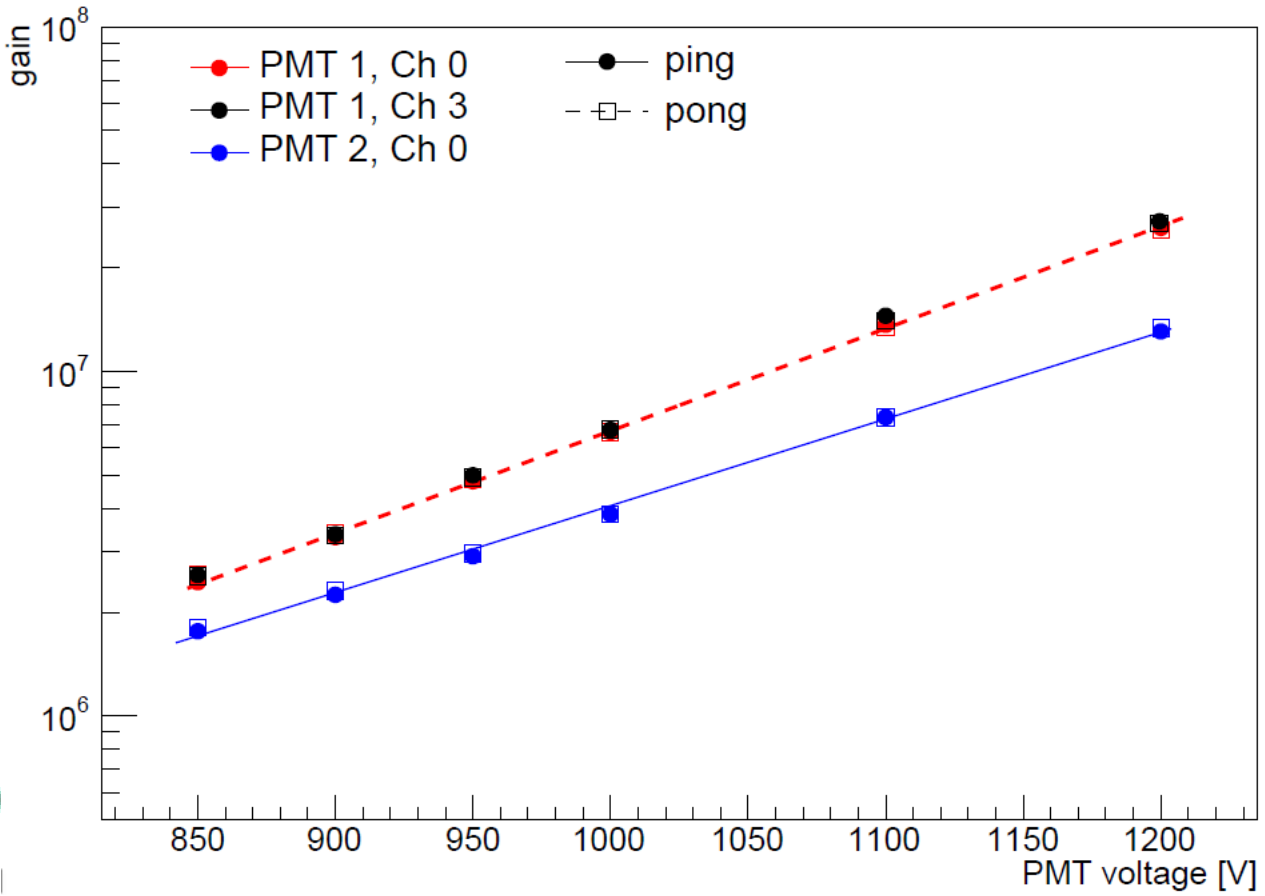
Ping-pong: charge difference < 5 %

Good **charge uniformity** (only 2 chs)

Wiggles due to the clock coupling : do not affect spe accuracy

Spectrum for different HV





Conclusions

- CATIROC is an innovative concept for cost-effective readout of large photomultiplier areas
  - Auto-triggered, zero-suppressed charge and time measurement on 16 independent channels
- CATIROC performances fit well the needs of JUNO-SPMT:
  - 100% trigger efficiency @ **1/3 p.e.** (50 fC @ PMT gain 10^6)
  - Charge resolution (**only HG used**) : 1.5 ADCu ~ **15 fC** (160fC @ PMT gain 10^6)
  - Time resolution= **167 ps rms**

Project ongoing:

- Tests with the HZC 3” PMT show
  - **Good p.e. spectrum**
  - Some features (ping/pong and wiggles) that have no significant effects on the data taking
- 9000 SPMTs (HZC XP72B22) have been produced and tested (1% rejected)
- Front End Board V0 is testing => new version (beginning of 2019)
- **2000 ASICs** CATIROC production at the end of 2018
  - Clock coupling corrected

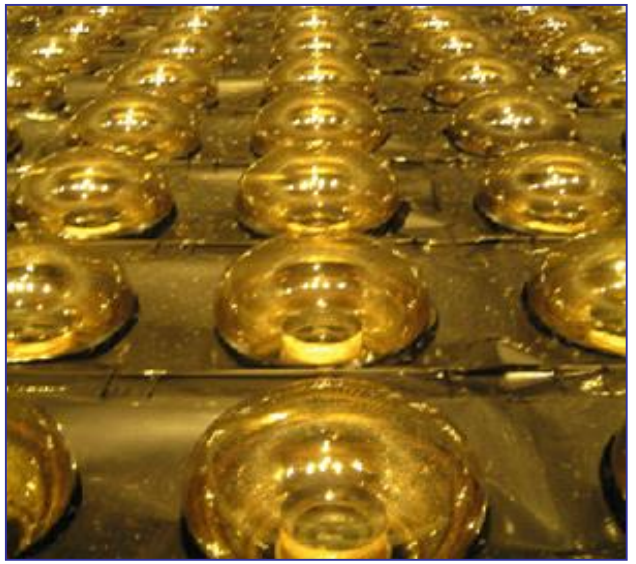
CATIROC datasheet:

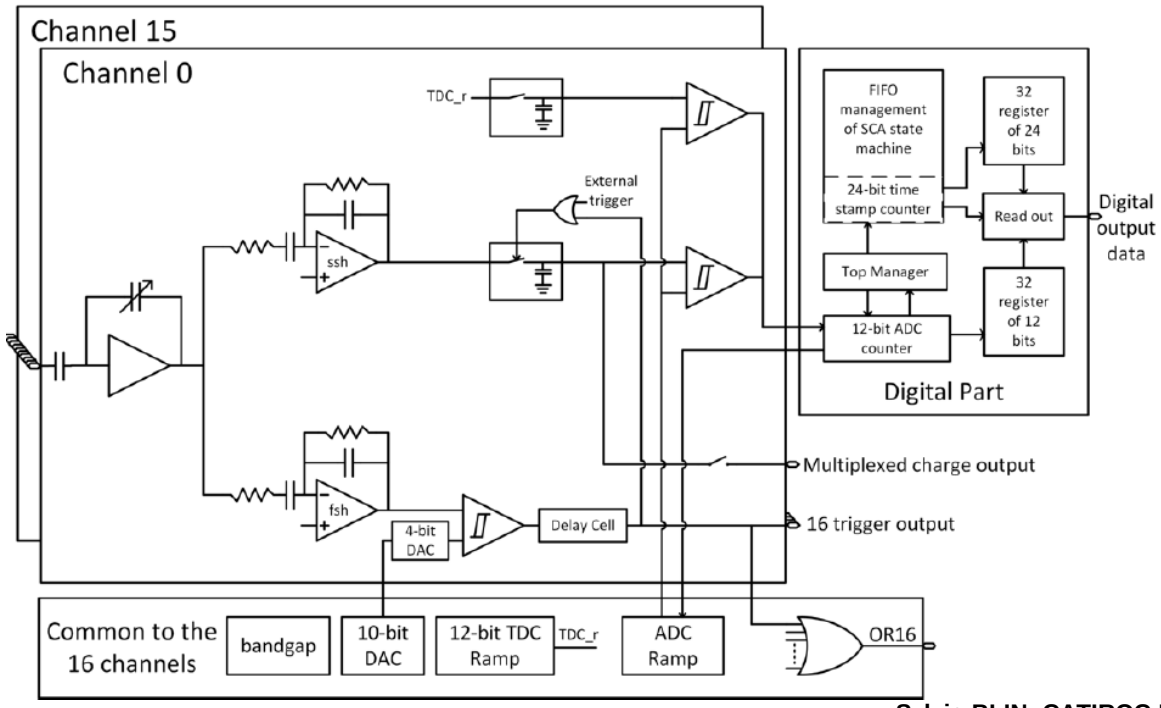
Selma Conforti
sconforti@omega.in2p3.fr

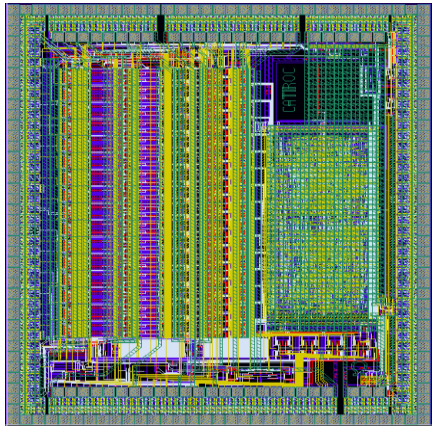
backup

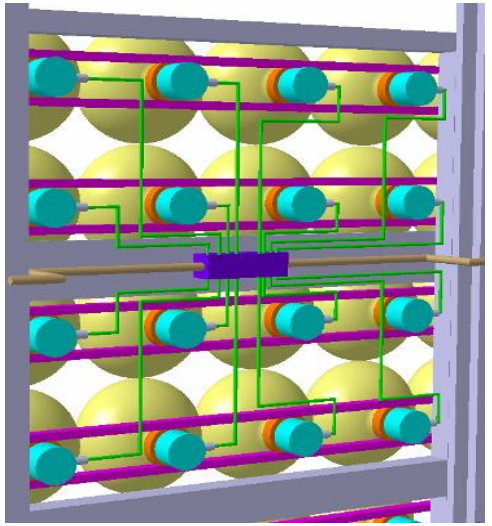
Application of PMm² project : PARiSROC & CATIROC

- Photomultiplier ARray Integrated SiGe Read Out Chip (2010)
  - « Large area PMT array » with centralized ASIC
  - Auto-trigger at 1/3 p.e.
  - Charge and time measurement (10-12 bits)
  - Data driven : « One cheap wire out »
- Evolved into CATIROC : Charge and Time Reat Out Chip (2015)
  - Larger readout rate (~50 kHz)



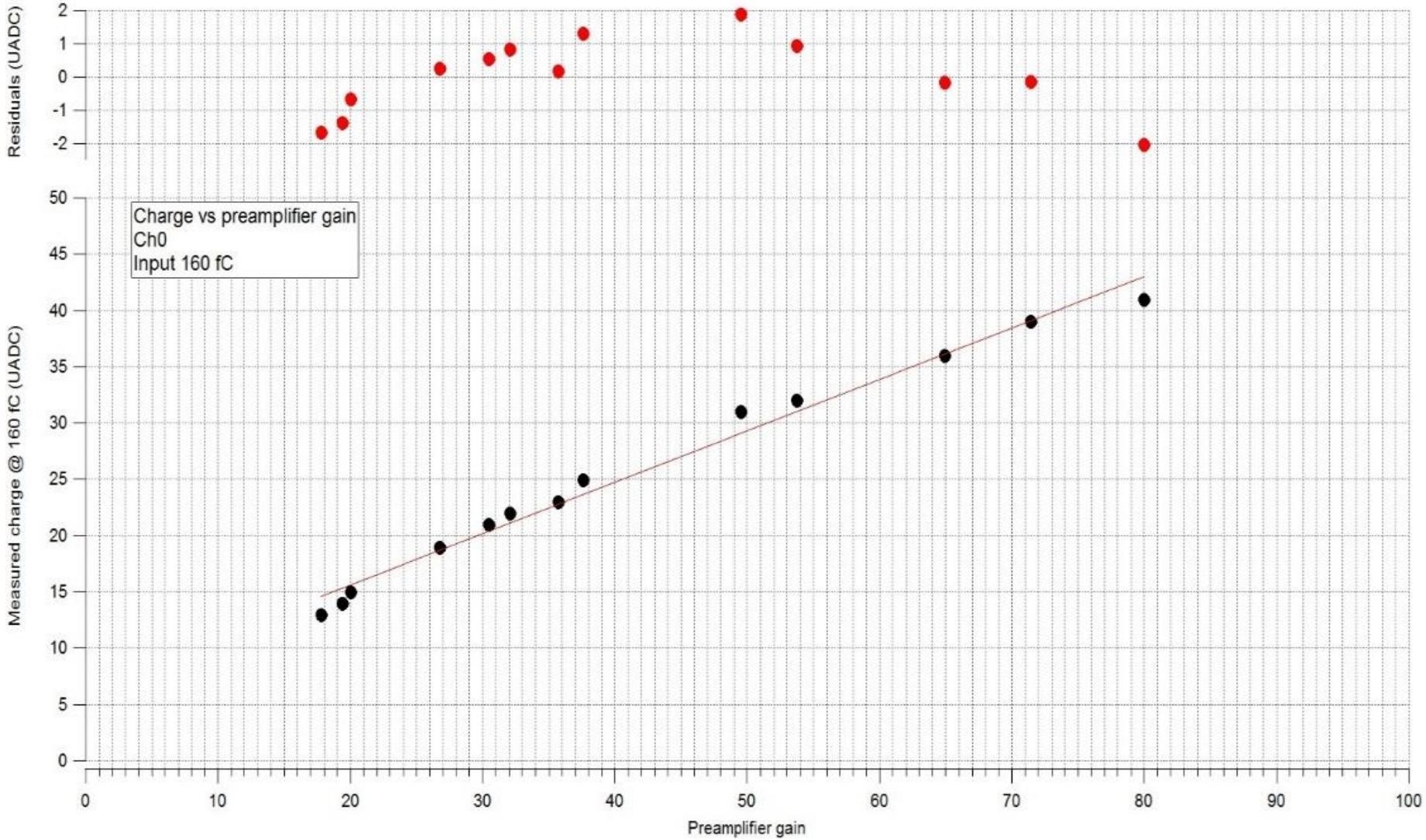






Gain adjustment

- 8 bits channel-wise : 1 to 4 range, per-cent accuracy



Electronics jitter and time walk

- Jitter measured on discriminator output
- Time walk ~ 5 ns