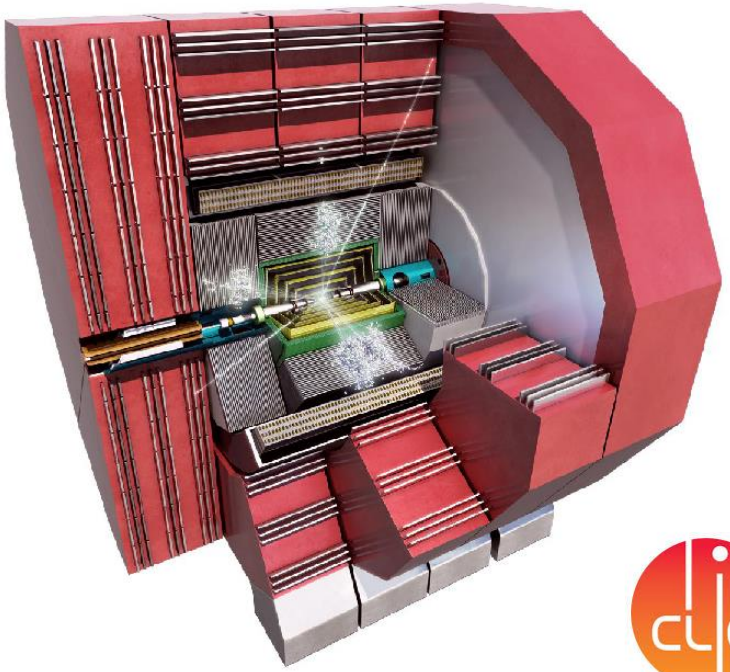
Characterisation and Temperature Stabilisation of a system with 22000 MPPCs

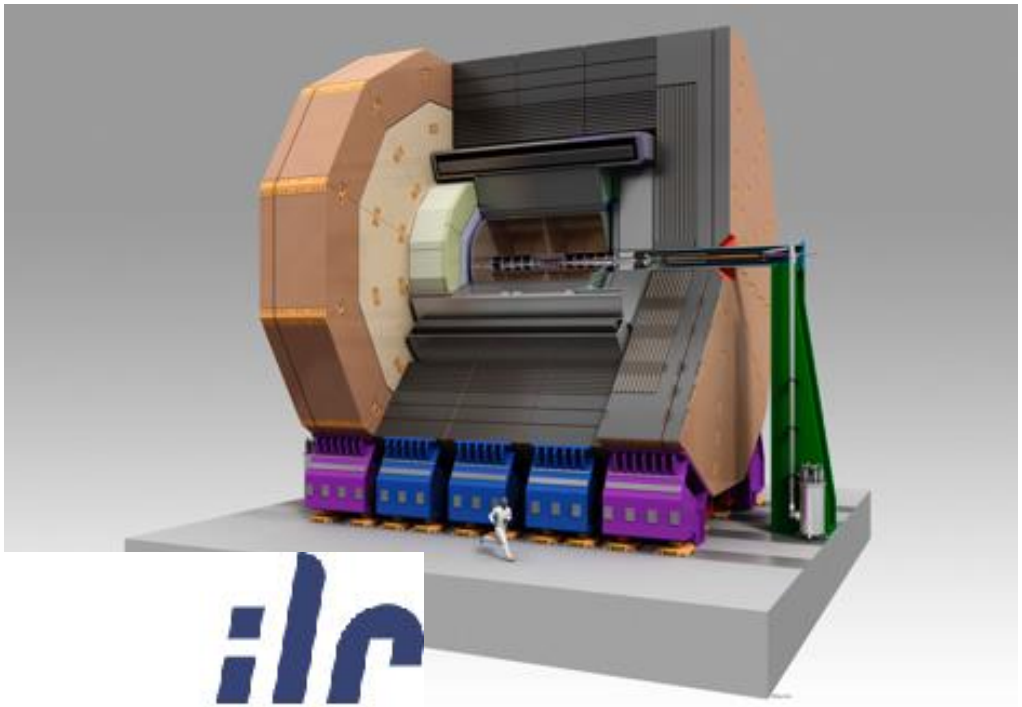
28.11.2018

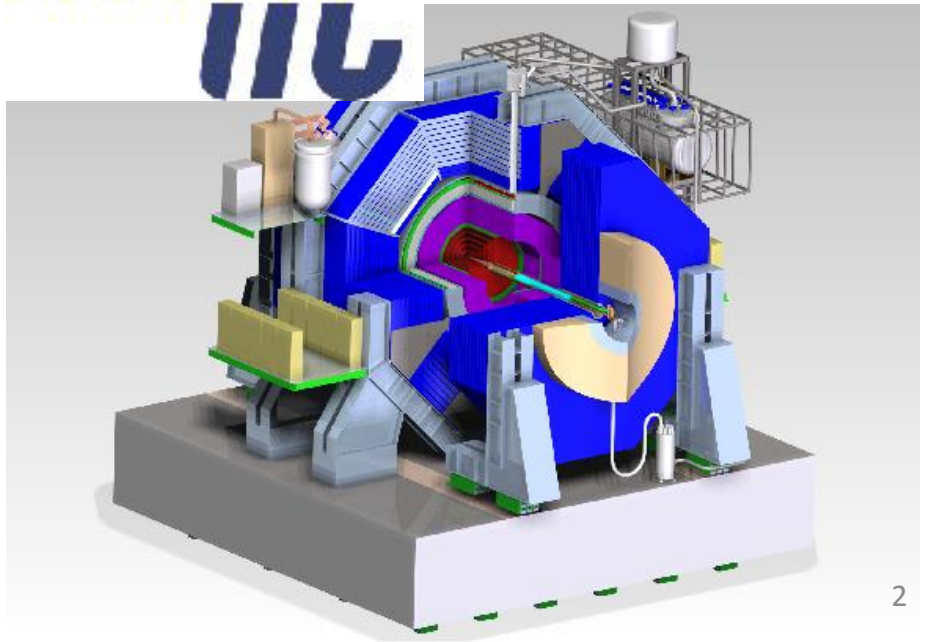
5th International Workshop on New Photon-Detectors (PD18)

Yuji Sudo (DESY)

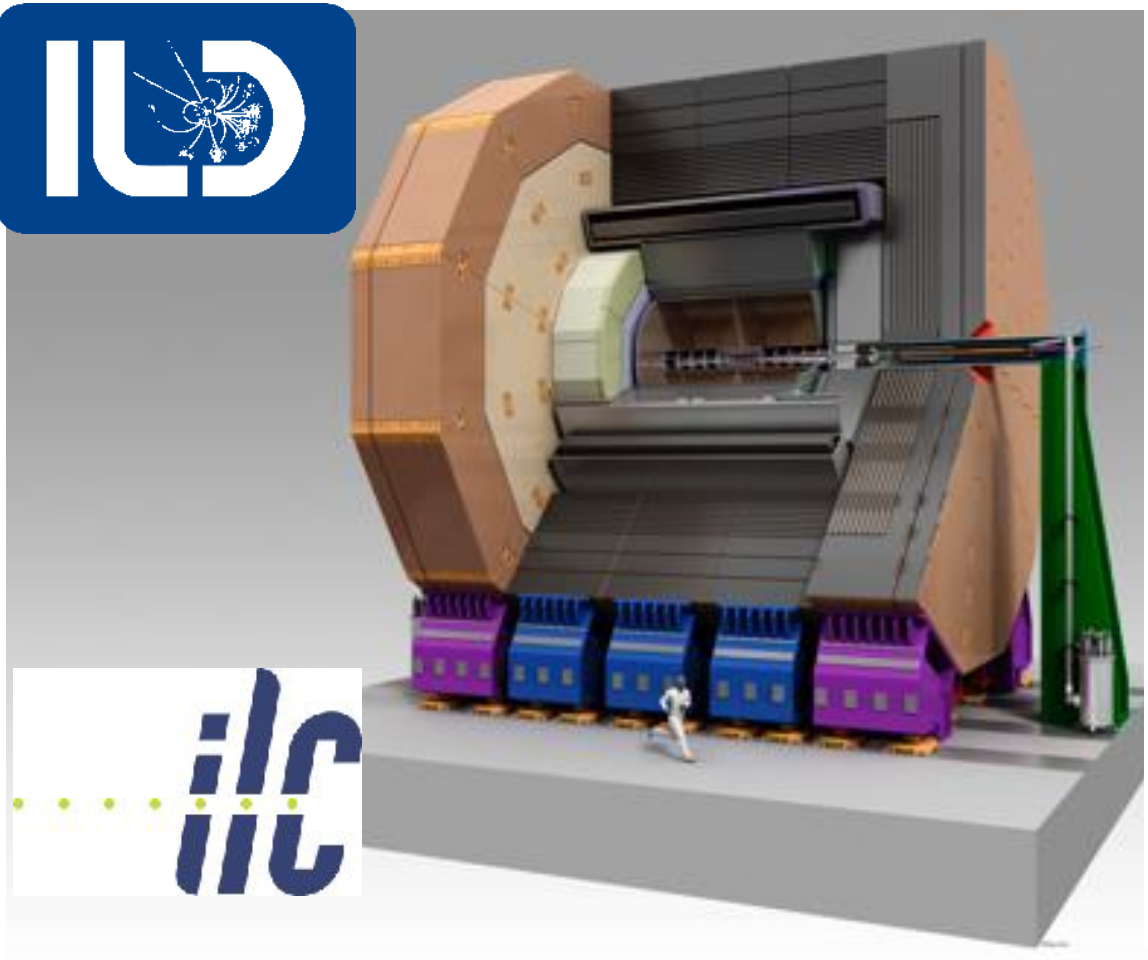
Future Detectors for e+ e- Collider Experiments



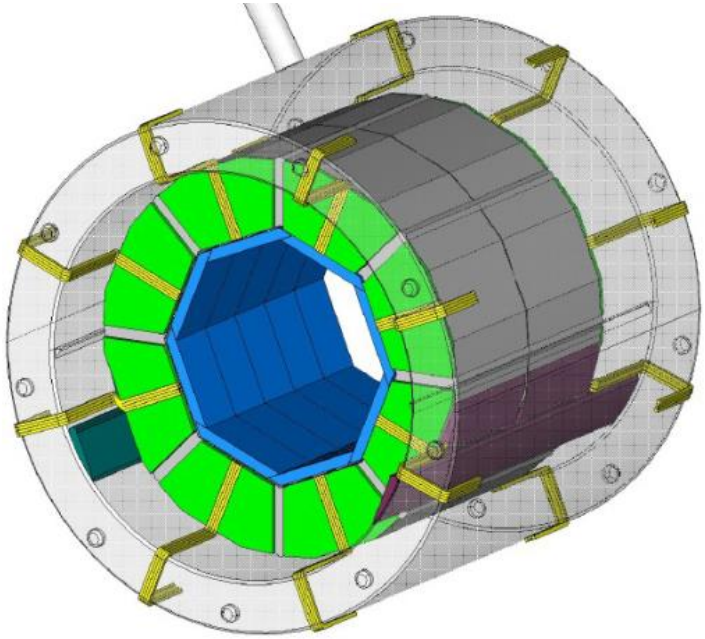




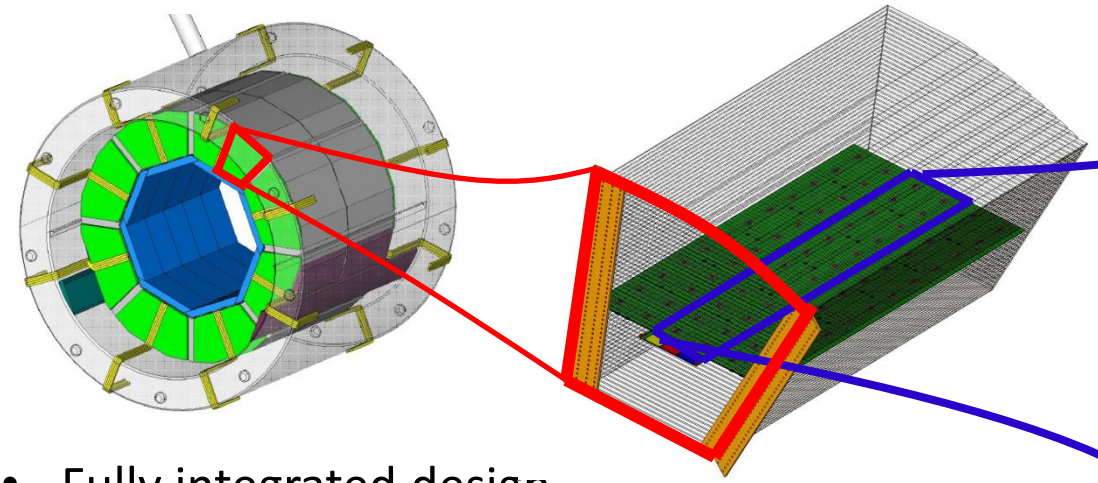
ILD for the ILC
and Analogue Hadron Calorimeter (AHCAL)

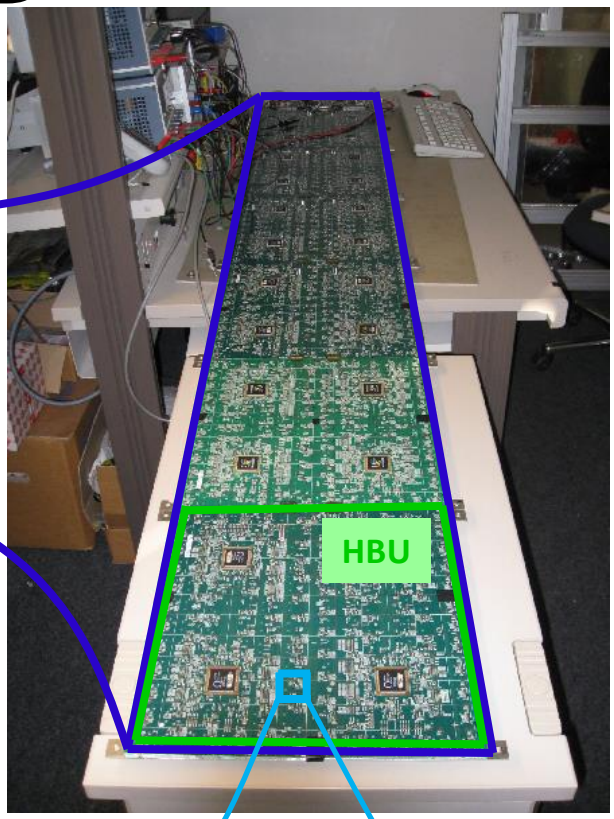


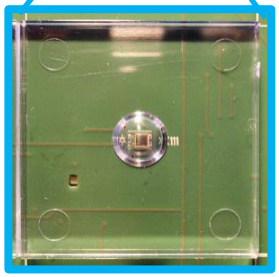
- Millions of channels for the full AHCAL for the ILD



AHCAL for ILD



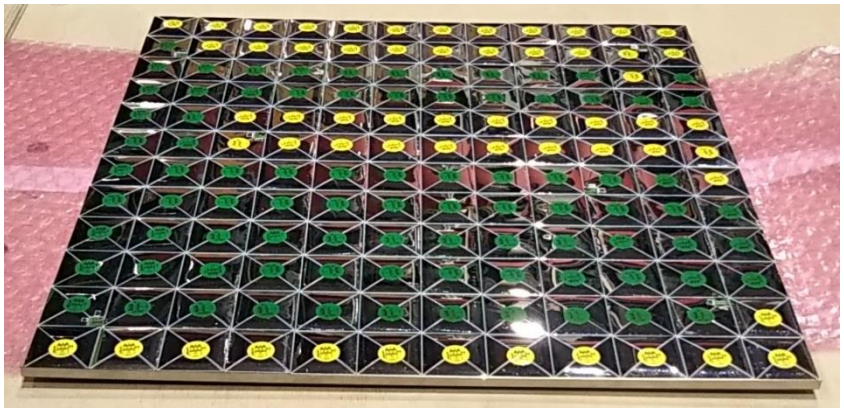


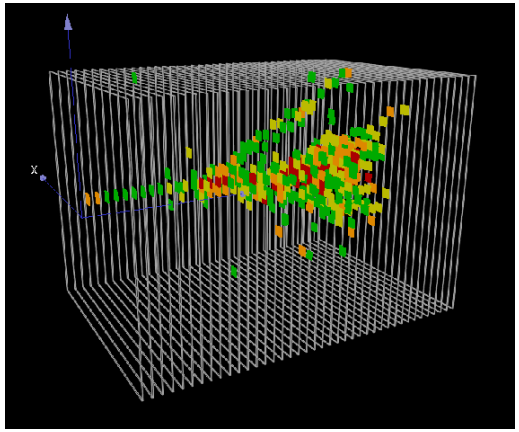


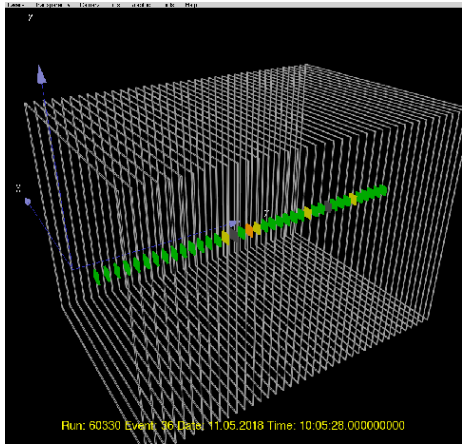
- Fully integrated design
  - front-end electronics, readout
  - voltage supply, LED system for calibration
  - no cooling within active layers
- Power-pulsed electronics
- Scalable to full detector (millions of channels)
- HCAL Base Unit: 36*36 cm2, 144 tiles, 4 ASIC
  - slabs of 6 HBUs
  - up to 3 slabs per layer
- One set of interface boards per layer

The Large AHCAL Technological Prototype

- TB at CERN / SPS H2 beam line in 2018
- Large prototype: 38/39 active layers of 72x72cm^2 in steel absorber, ~22000 channels, ~4λ







Outline

Testbeam prototype

- 600 ASICs, 700 configuration parameters each

MPPC low noise and good uniformity

→ Simplification of design and operation

Bias adjustment

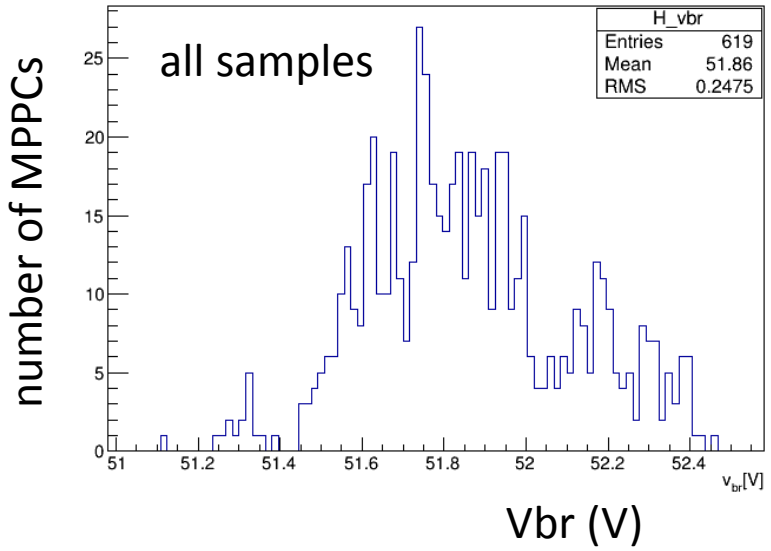
Channel by channel → Module by module

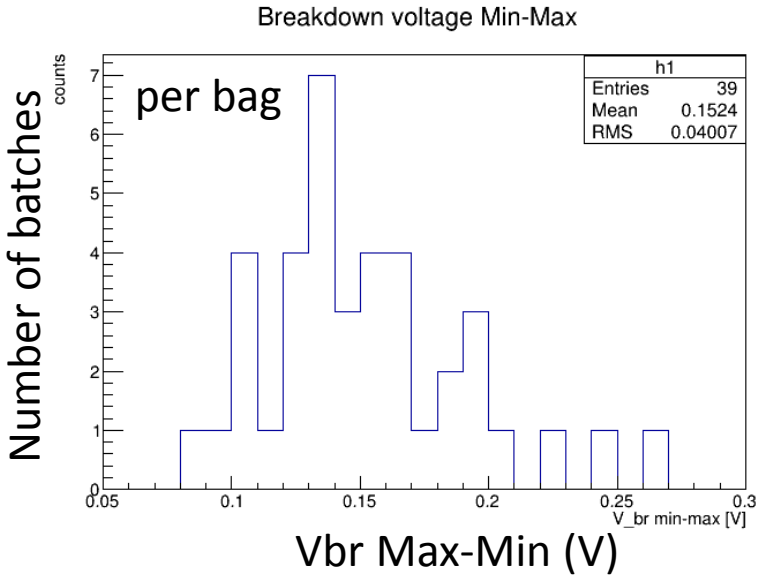
- Gain uniformity
- AHCAL response to MIP
- Self-triggering capability
- Vop temperature compensation

Homogeneity of 22000 MPPCs

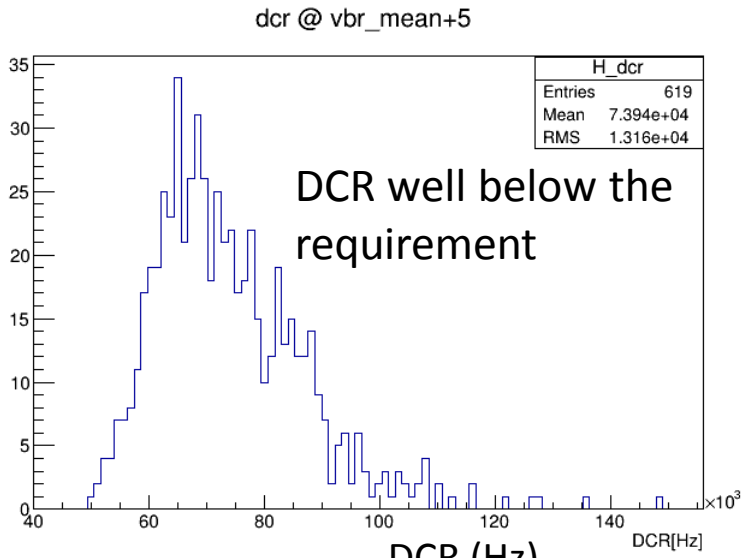
- 600 MPPCs in a bag (Vop±100mV)
  Pick 16 MPPCs up and test them at Heidelberg University
  576 MPPCs soldered on PCB at DESY

- Good homogeneity of Vop
  → No bias voltage adjustment for each MPPC
  → Module by module bias voltage adjustment is enough
  576 MPPCs/module

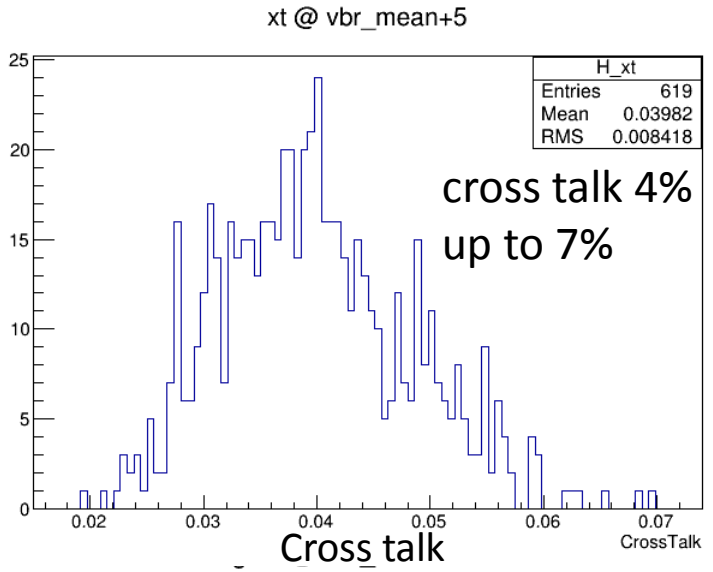




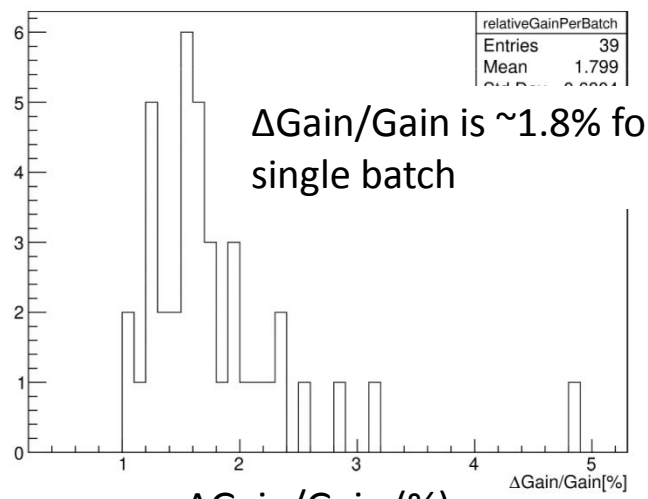
Result of Sampling Test at Uni. Heidelberg



DCR (Hz)

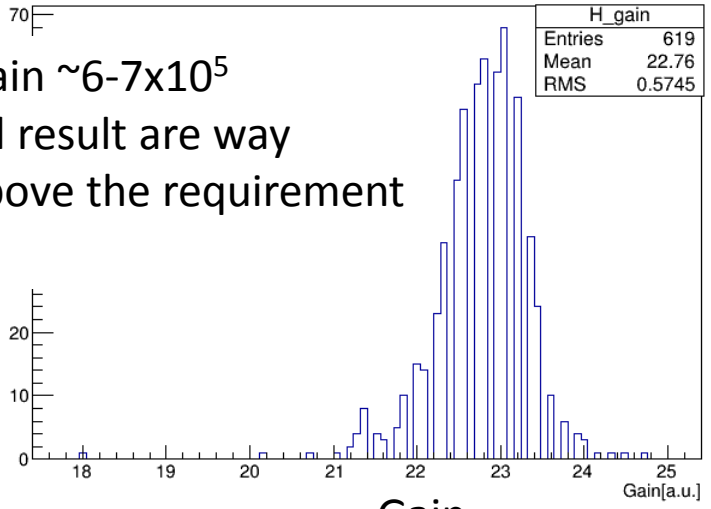


Cross talk



ΔGain/Gain (%)

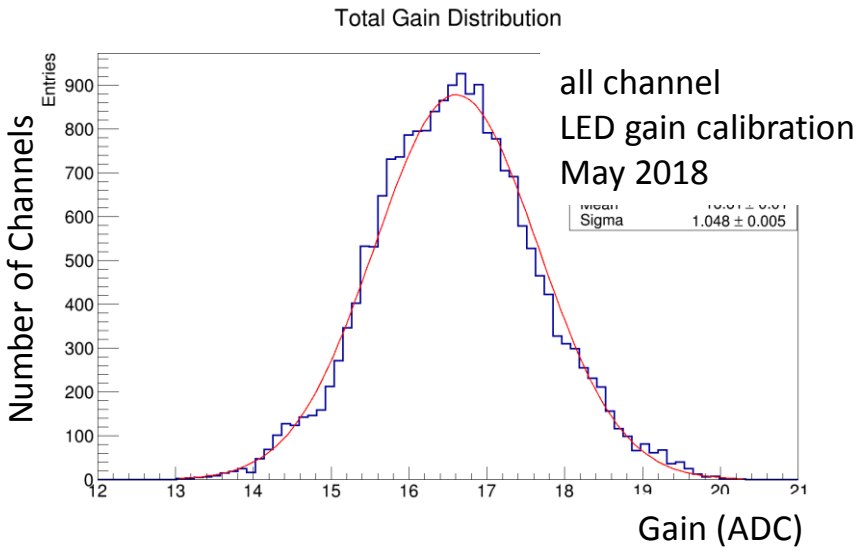
Gain ~6-7x10^5
All result are way above the requirement

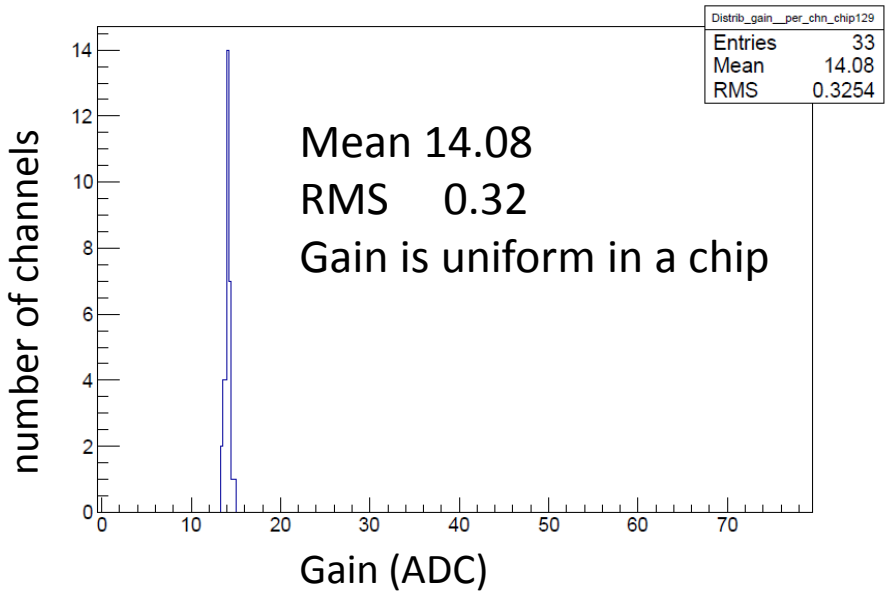


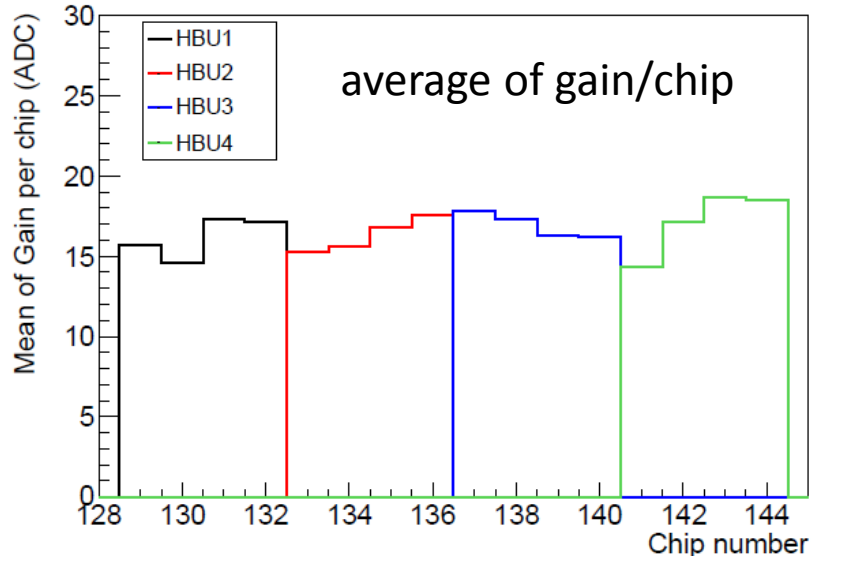
Gain

Uniformity of Gain on HBU

- Gain of ~22000 MPPCs are within 13-20 (ADC) by module-wise V_{bias} adjustment
- Gain in a chip is uniform: RMS <~3%



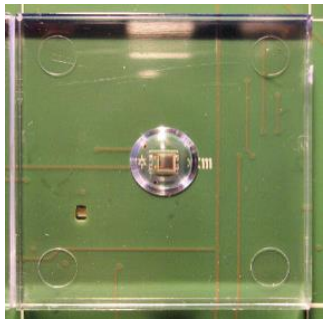


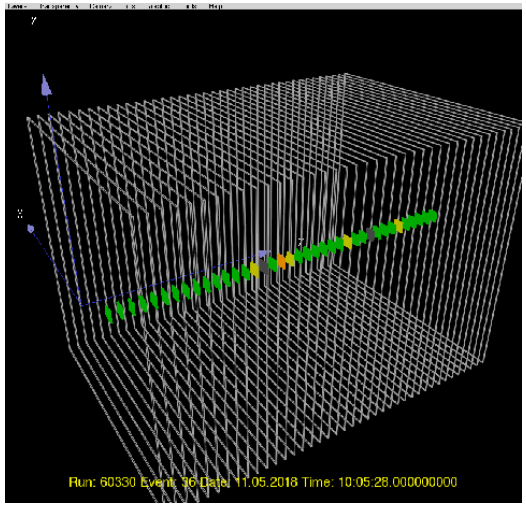


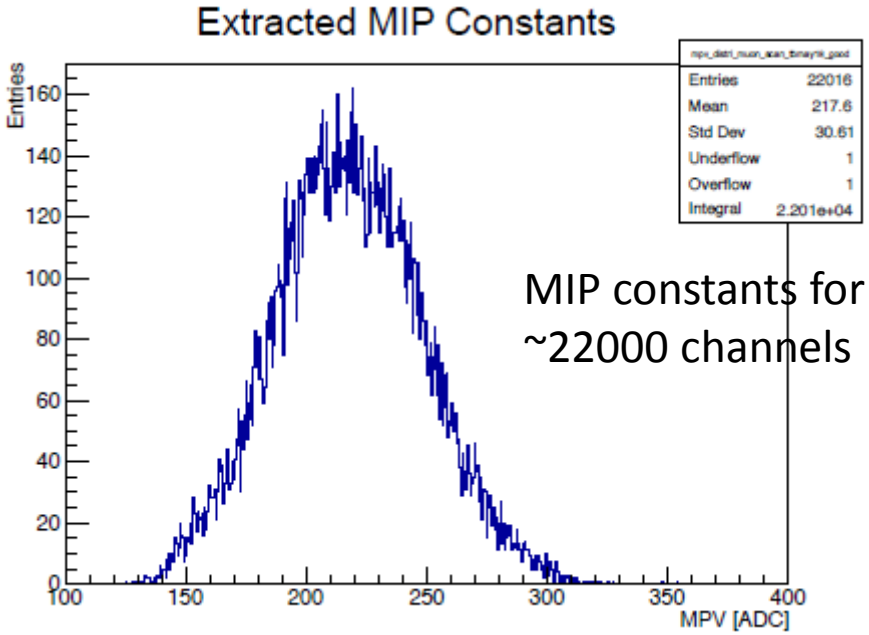
Response to 40 GeV Muon (MIP Calibration)

- MIP signals are reasonably large
- MIP signal >10 p.e.

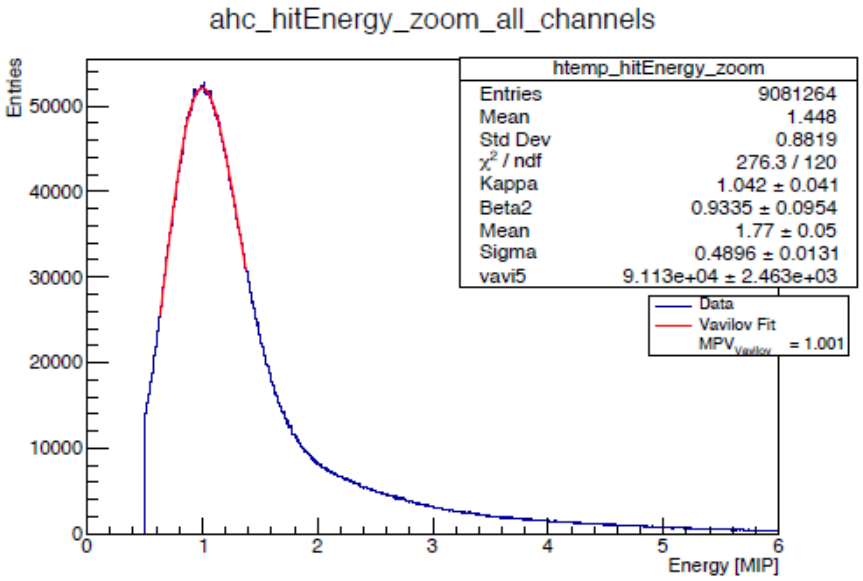
- Dead channels < 20 out of ~22000







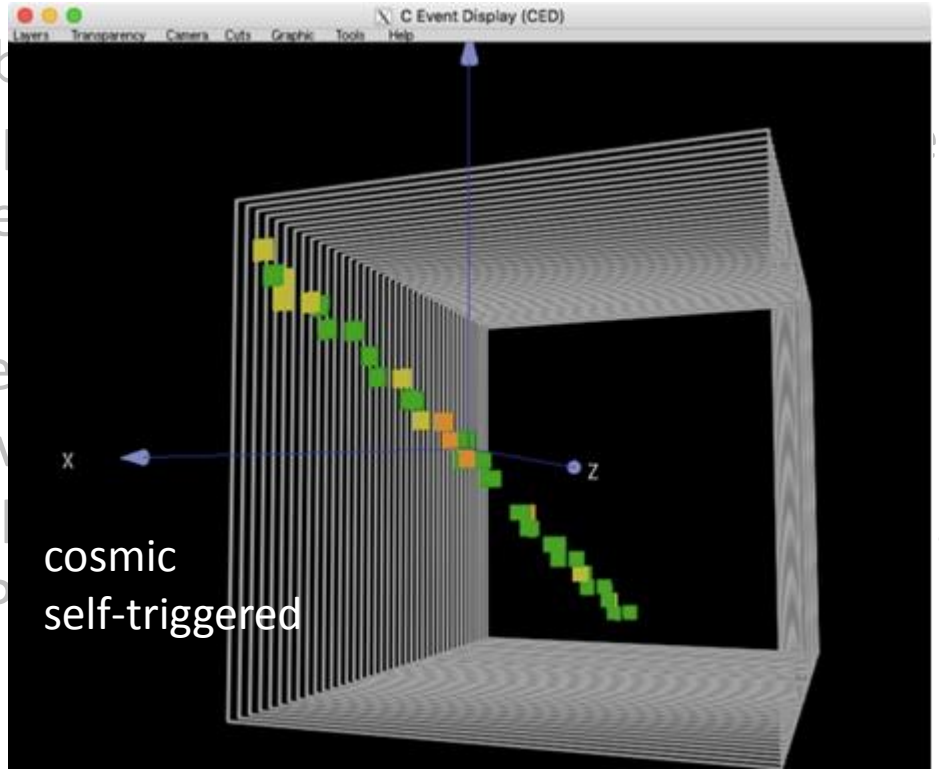
MIP constants for ~22000 channels



Homogeneity of 22000 MPPCs

- 600 MPPCs in a b
  pick 16 MPPCs u ersity
  576 MPPCs solde

- Good homogene
  → No bias v
  → module l s enough
  576 MPP



- Low noise rate
  → common trigger threshold aiming 0.3 MIP
  (0.5 MIP for data analysis)

  + Uniform light yield of tile
  → Low event rate triggered by noise without any external validation signal

Temperature Compensation for MPPC

- MPPC gain depends on temperature. Because breakdown voltage depends on temperature.

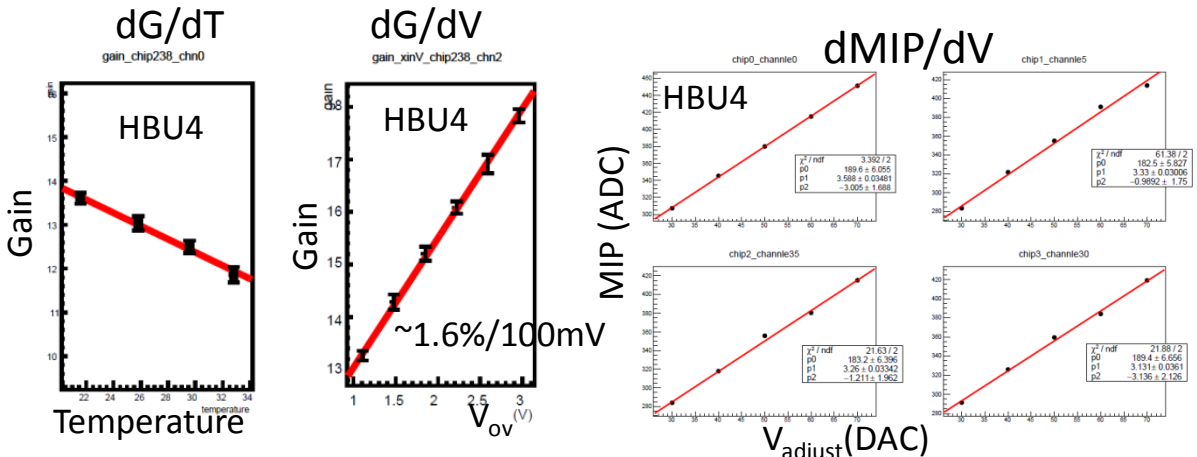
  complete discussion of temperature dependence on gain by HPK.
  https://hub.hamamatsu.com/sp/hc/resources/Temperature_Gain_SiPM.pdf

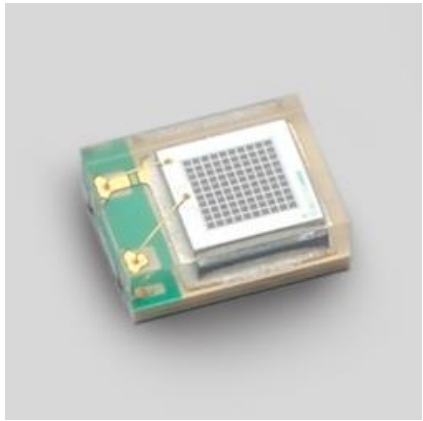
$\text{Gain} \propto V_{ov}$
$V_{ov} = V_{bias} - V_{break\ down}$

- We want to keep V_{ov} same as a value at a reference point. Adjust bias voltage against temperature changes.

→Automatic HV adjustment

- HPK S13360-1325
- dMIP/dV is ~1.1%/DAC (1 DAC ~ 37mV)

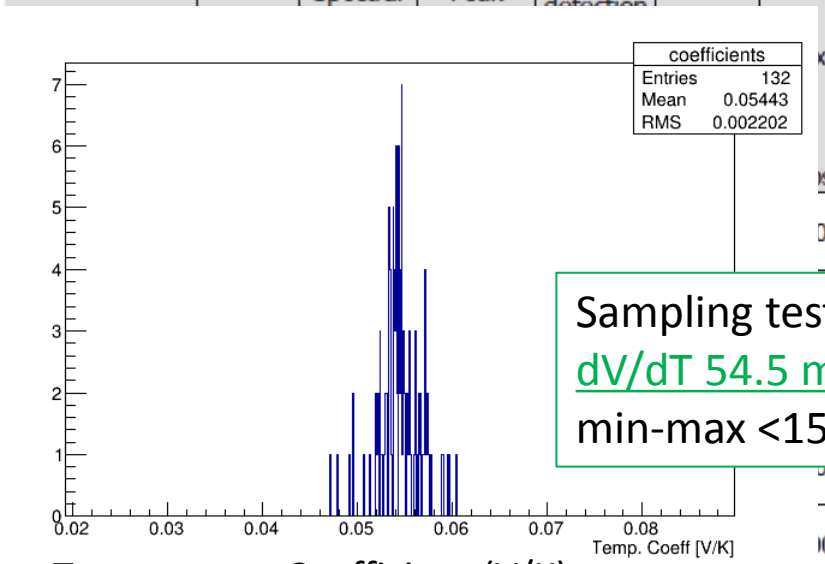




Specification of the S13360 Series

Electrical and optical characteristics (Typ. Ta=25 °C, unless otherwise noted)

		Spectral	Peak	Photon	Dark count*5		Terminal capacitance Ct	Gain M	Breakdown voltage VBR	Crosstalk probability	Recommended operating voltage Vop	Temperature coefficient at recommended operating voltage ΔTVop
							(pF)		(V)	(%)	(V)	(mV/°C)
S13360-6050PE		320 to 900										
S13360-1375CS	Vover =3 V	270 to 900										
S13360-1375PE		320 to 900										
S13360-3075CS		270 to 900										
S13360-3075PE		320 to 900										
S13360-6075CS		270 to 900										
S13360-6075PE		320 to 900										



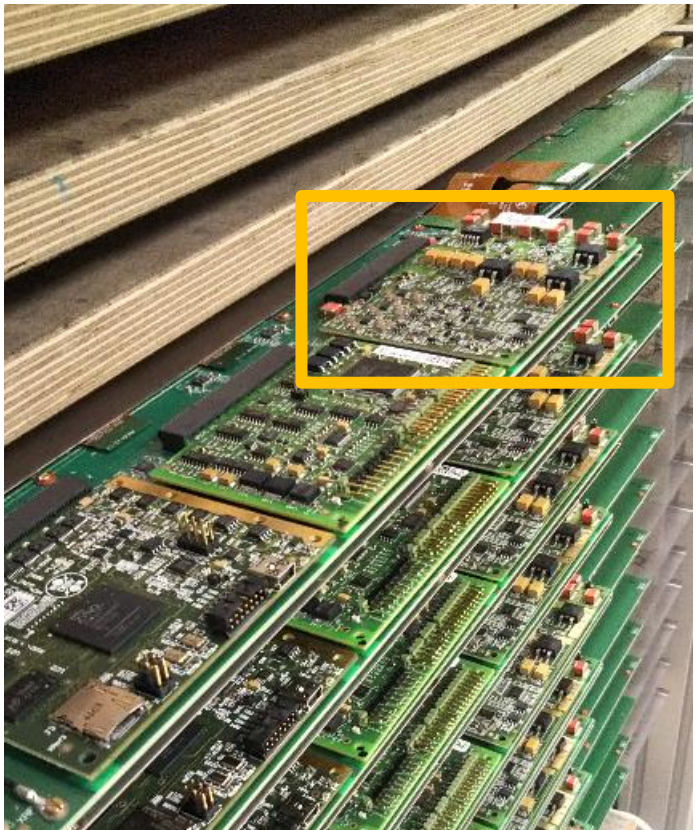
Temperature Coefficient (V/K)

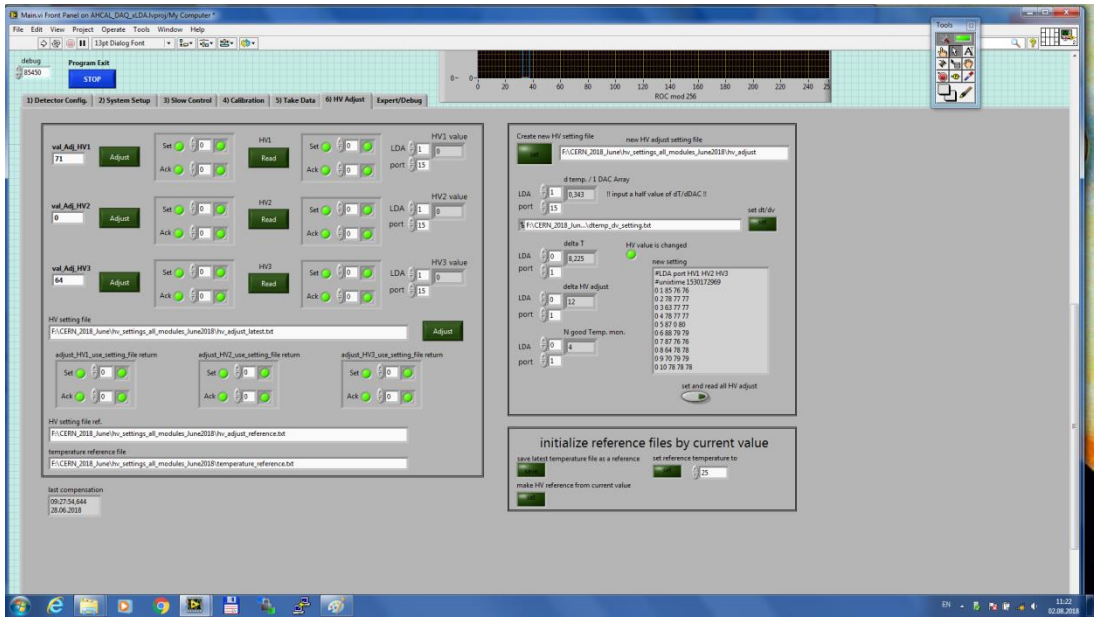
Sampling test at Uni. Heidelberg
dV/dT 54.5 mV/K
min-max <15 mV/K

Temperature coefficient of V_{br} = 54mV/˚C
→0.685˚C/1DAC

HV Adjustment by Power Board on CIB

- The power board has a function of bias voltage adjustment
- Range 0-127 DAC (~37mV/DAC) (in principle covers ±40 ℃)
- Implement automatic HV adjust application in DAQ LabView interface

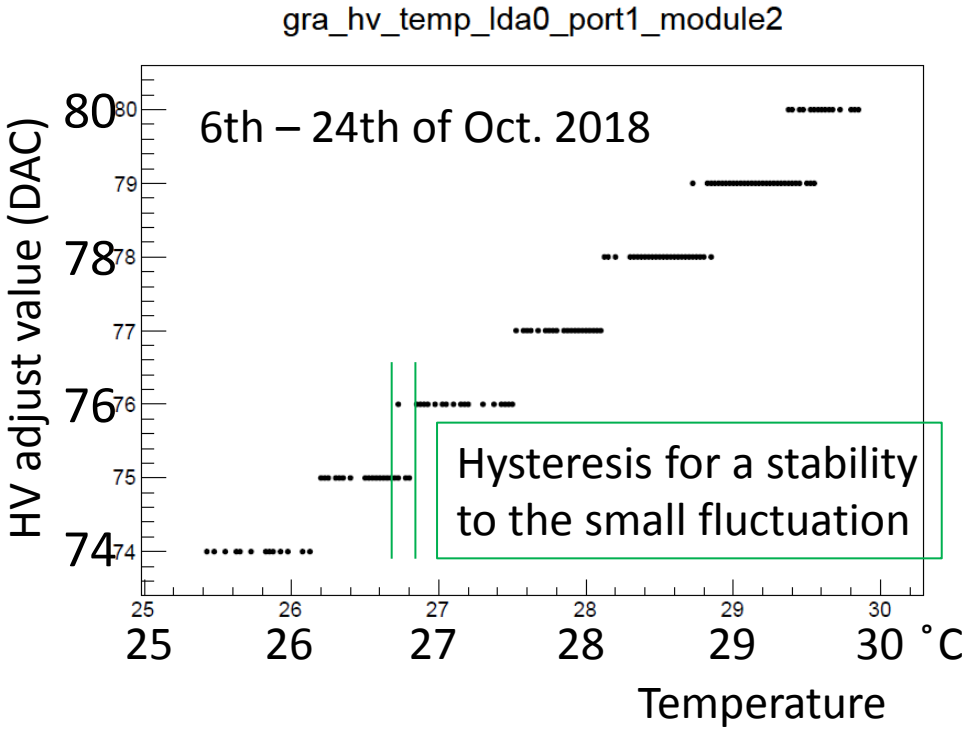


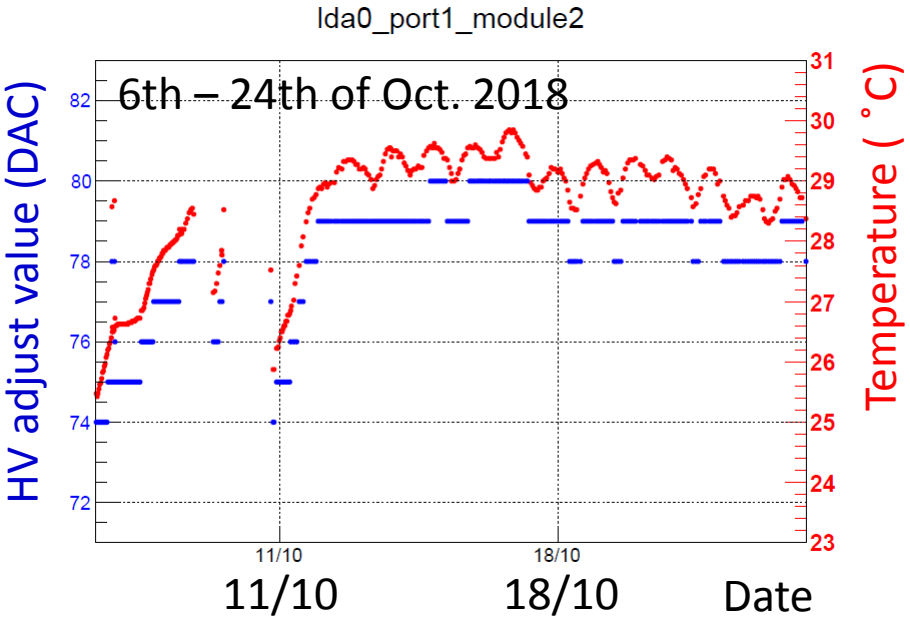


HV Adjustment

HV Adjust Value and Temperature vs Time

- Automatic HV adjustment on power board successfully works for Vop correction against temperature changes.
- Routinely running for TB in 2018

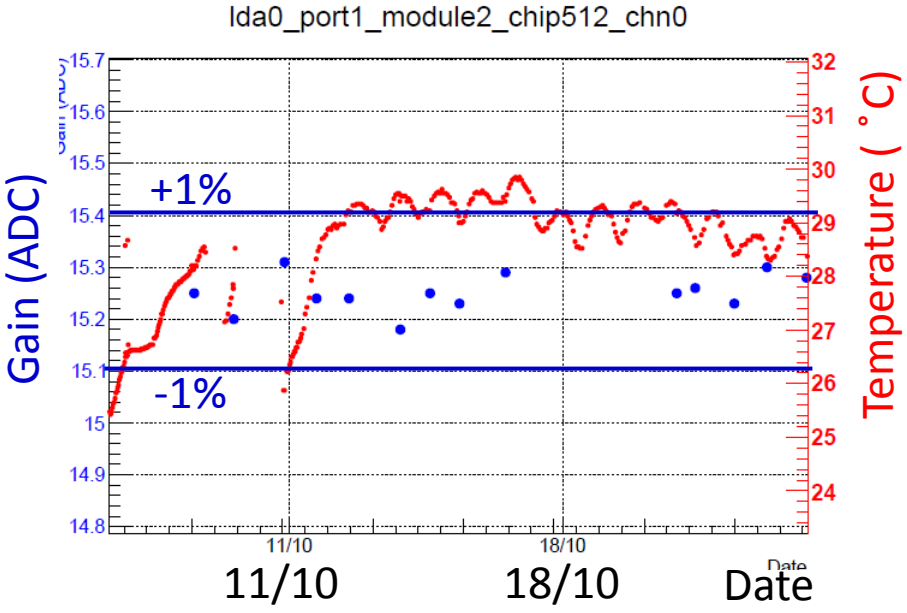


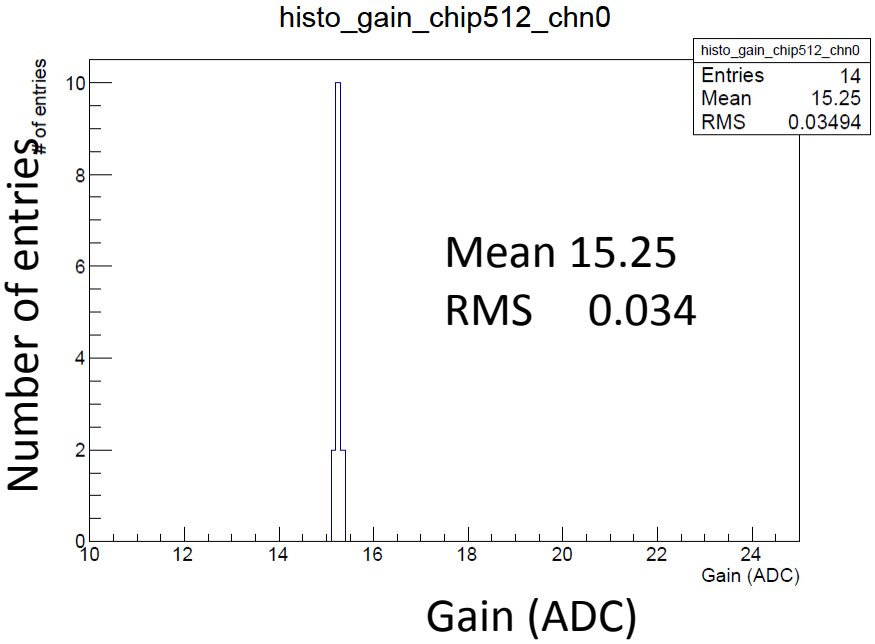


Gain Stability

Gain and Temperature vs Time

- Gain of MPPCs are successfully stabilized by automatic HV adjustment
- Dispersion of gain is within a precision of gain extraction by multi Gaussian fitting (<1%)





Summary

- Calorimeter system with 22000 MPPCs: smooth commissioning and operation
- Low noise and self-triggered operation with 0.3 MIP sensitivity
- Excellent uniformity of MPPCs: operation at common bias and without channel-by-channel adjustment of voltage, gain or threshold
- Automatic adjustment of common bias voltage to compensate for temperature changes → stable gain within less than $\pm$ 1%

backup

dMIP/dV is larger than dGain/dV of MPPC

- dMIP/dV is ~1.1%/DAC

but

- dGain/dV of MPPC is ~ 0.6%/DAC

There is 0.5% gap between dMIP/dV and dGain/dV

- What is considered cause of the gap?

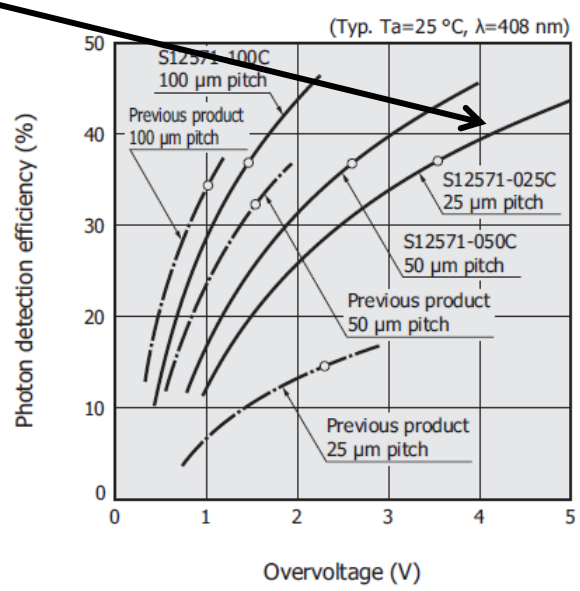
bias voltage dependence on properties of MPPC

- photon detection efficiency
- after pulsing probability
- cross talk probability
- …

$$V_{ov} = V_{bias} - V_{break\ down}$$

ref. e03_handbook_si_apd_mppc.pdf

[Figure 2-8] Photon detection efficiency vs. overvoltage



dMIP/dV is larger than dGain/dV of MPPC

- dMIP/dV is ~1.1%/DAC

but

- dGain/dV of MPPC is ~ 0.6%/DAC

There is 0.5% gap between dMIP/dV and dGain/dV

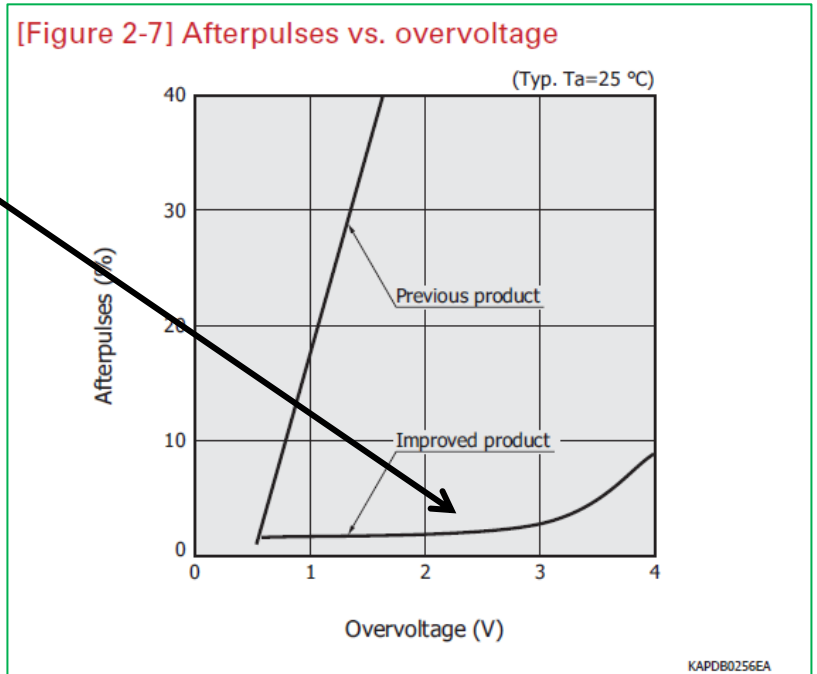
- What is considered cause of the gap?

bias voltage dependence on properties of MPPC

- photon detection efficiency
- after pulsing probability
- cross talk probability
- …

$$V_{ov} = V_{bias} - V_{break\ down}$$

ref. e03_handbook_si_apd_mppc.pdf



dMIP/dV is larger than dGain/dV of MPPC

- dMIP/dV is ~1.1%/DAC

but

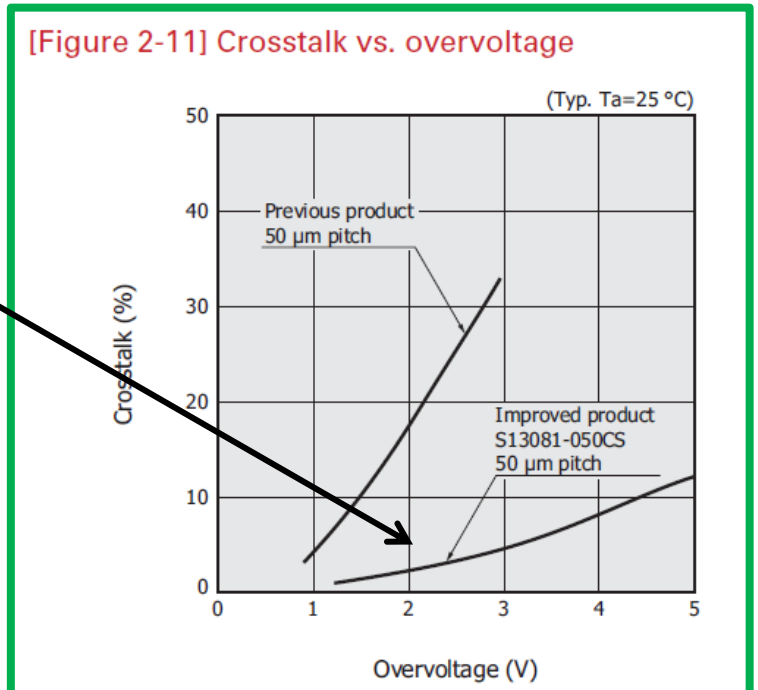
- dGain/dV of MPPC is ~ 0.6%/DAC

There is 0.5% gap between dMIP/dV and dGain/dV

- What is considered cause of the gap?

bias voltage dependence on properties of MPPC

- photon detection efficiency
- after pulsing probability
- cross talk probability
- …

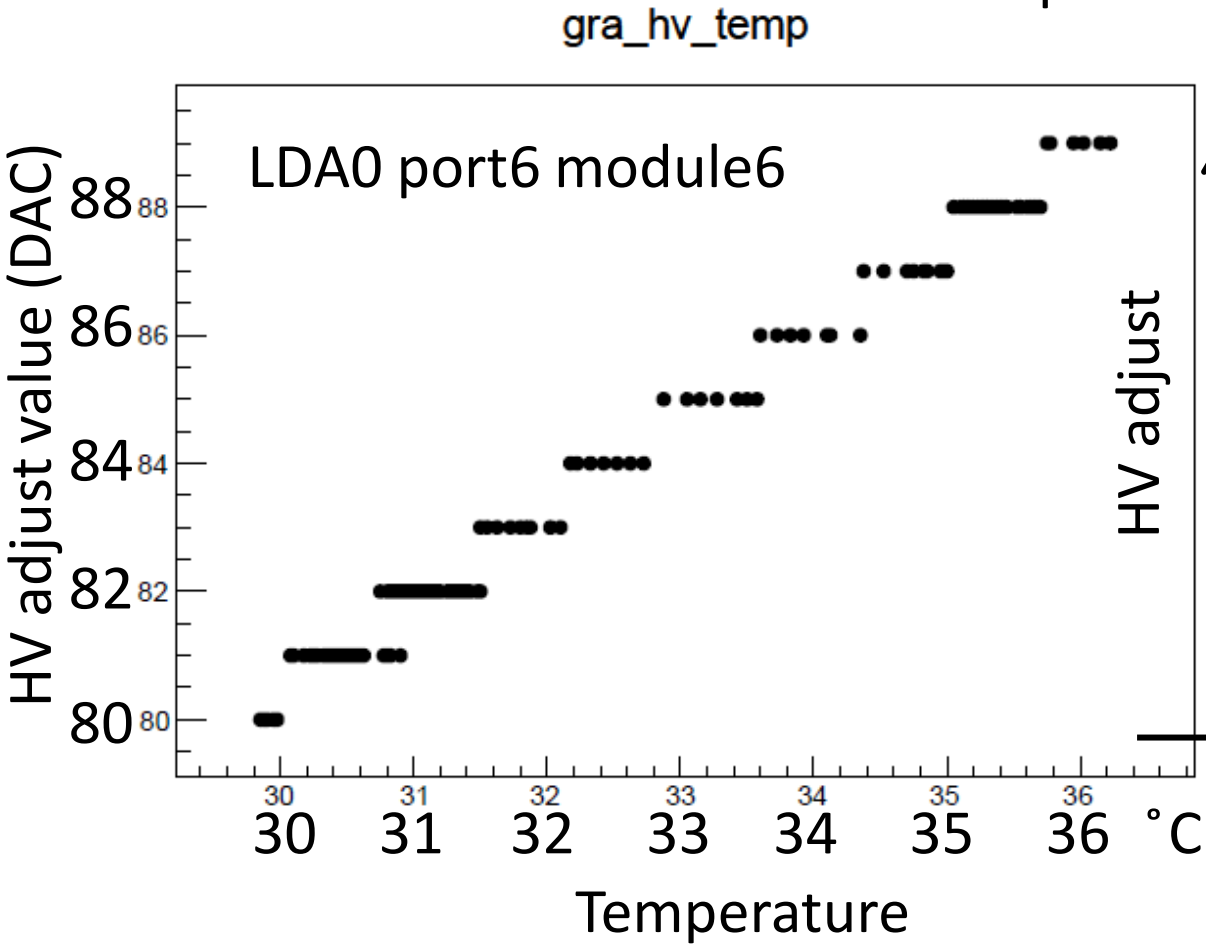


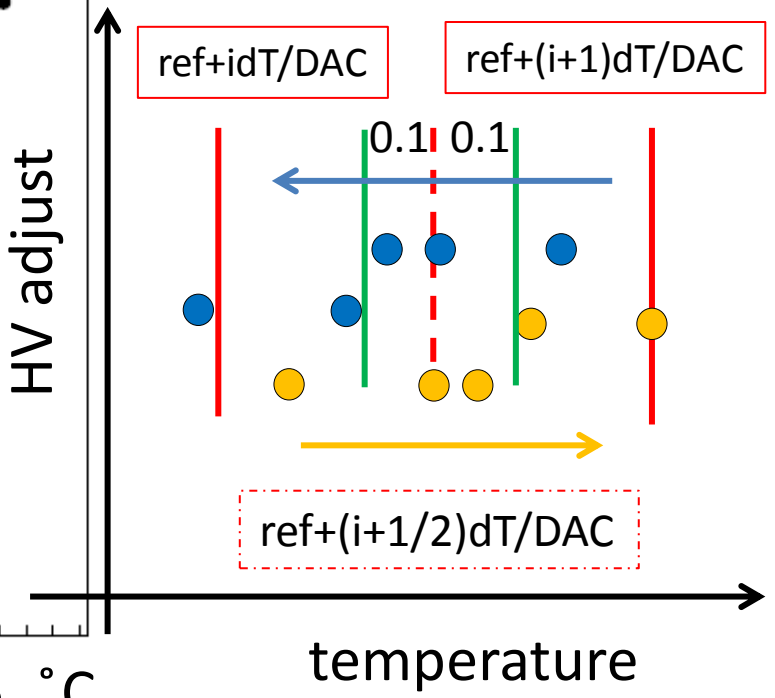
$$V_{ov} = V_{bias} - V_{break\ down}$$

ref. e03_handbook_si_apd_mppc.pdf

HV adjust vs Temperature

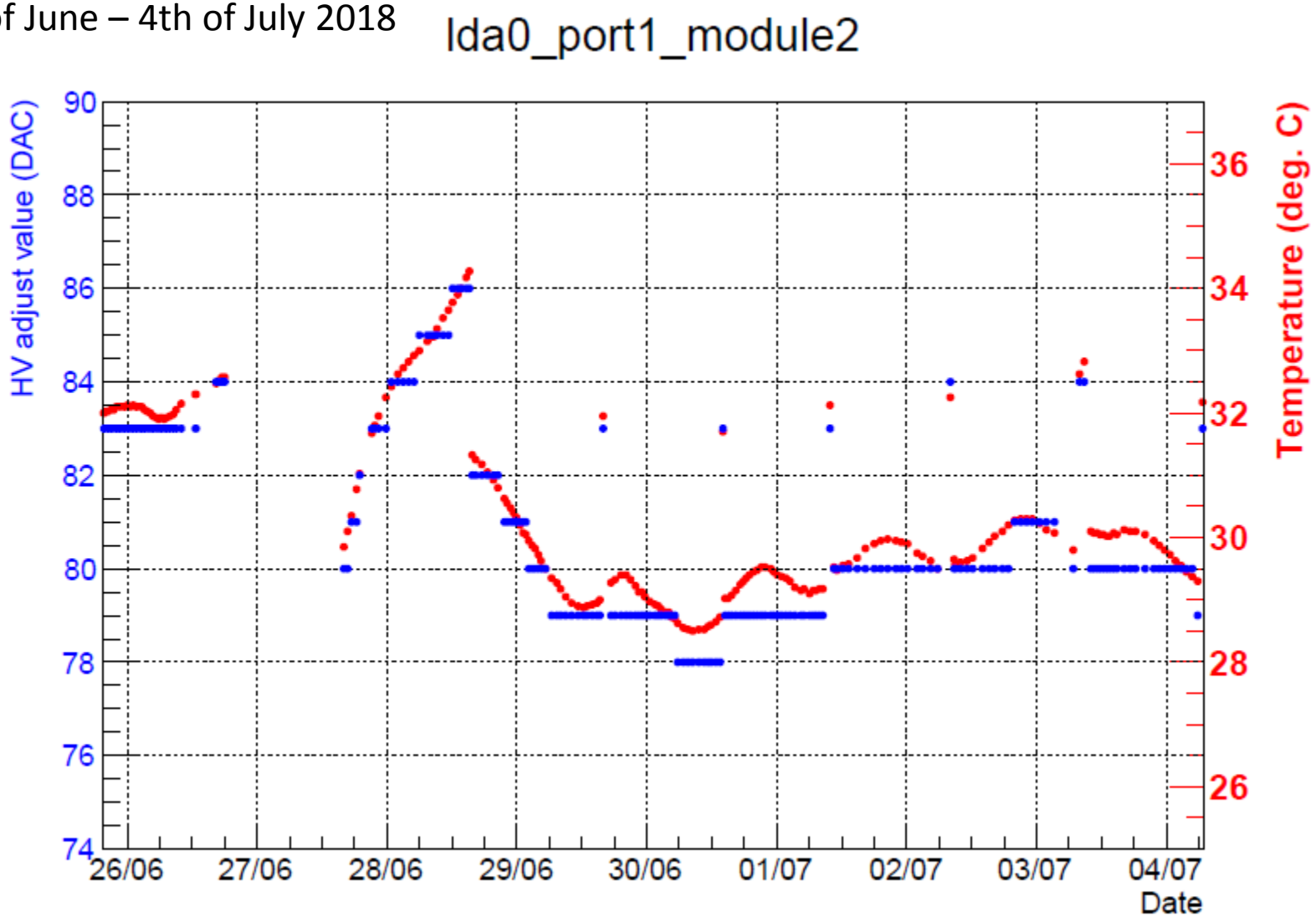
- 28th of June – 4th of July 2018
- There are over-lap of 0.2 degree C due to a hysteresis for stabilization around borders of temperature





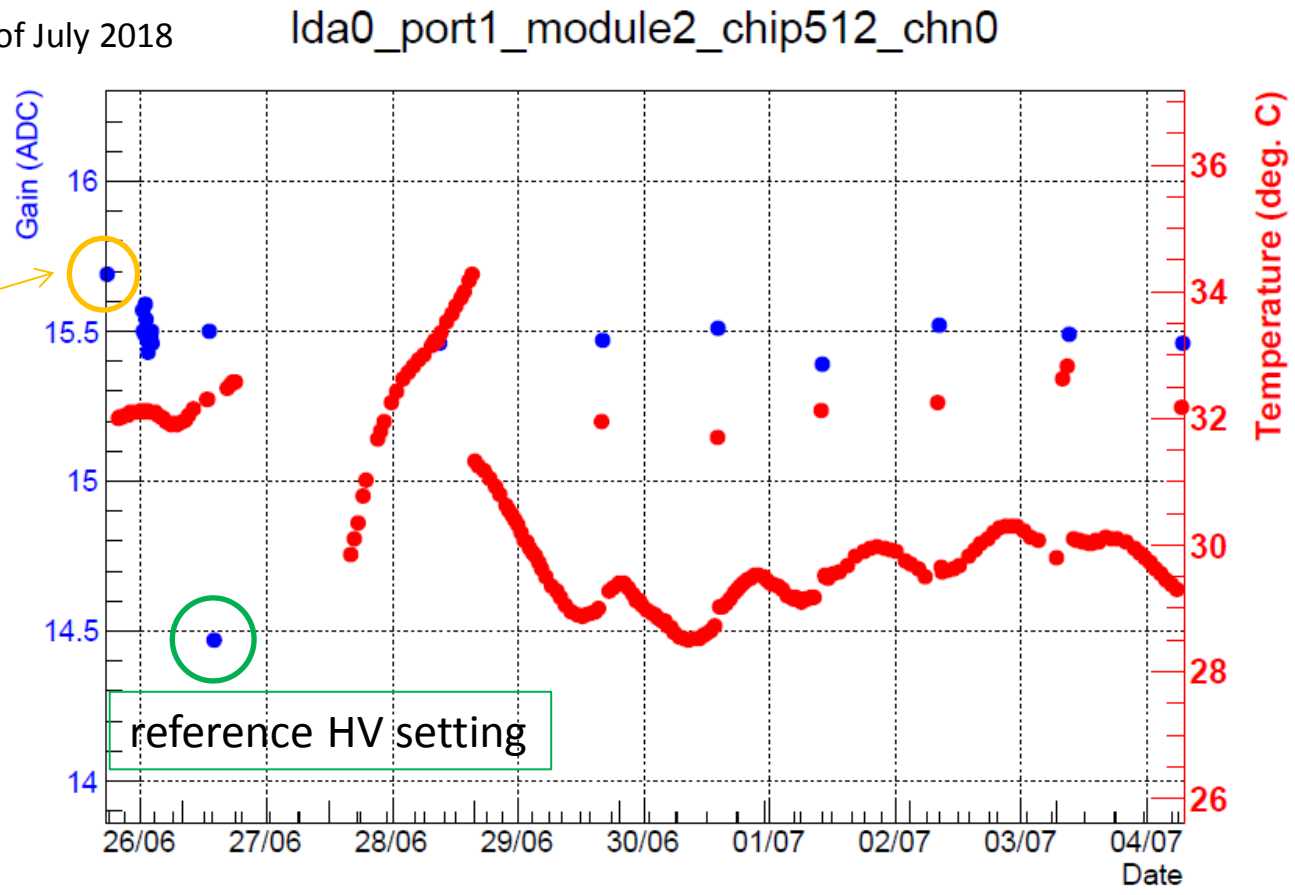
HV adjust value and Temperature vs Time

28th of June – 4th of July 2018



Gain and Temperature vs Time

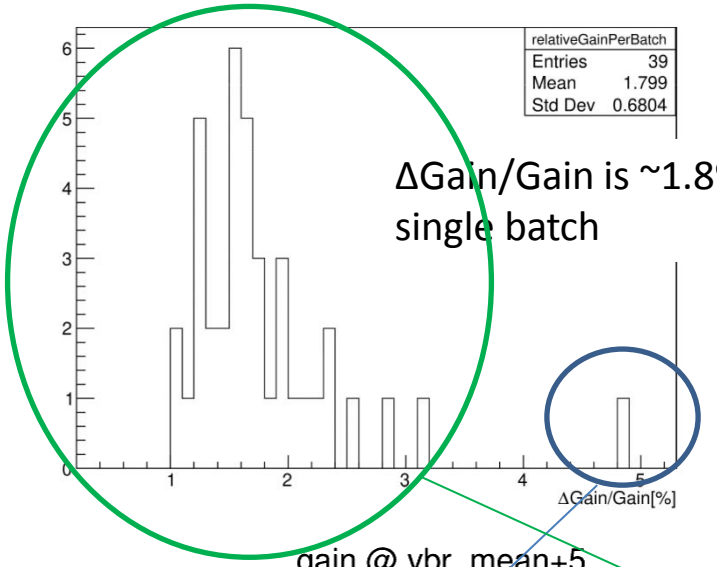
28th of June – 4th of July 2018



no HV adjust (same setting as the last configuration)

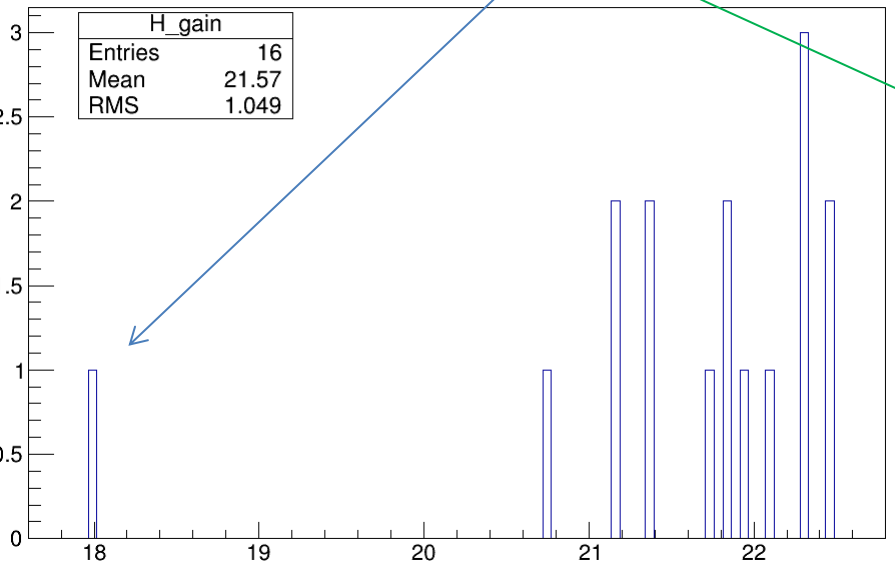
- Automatic HV adjustment on power board successfully works for the temperature compensation.
- Automatic HV adjustment is included in DAQ chain for TB in 2018.

gain measurement at Heidelberg



ΔGain/Gain is ~1.8% for a single batch

gain @ vbr_mean+5



gain @ vbr_mean+5