HK DAQ
recent status

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Amount of raw data ~ site dependence

μ rate drastically changes the raw data rate

→ Data size will be largely reduced if the location is deeper

Data rate after the software trigger

~ real-time data processing ~

1) Trigger rates and data sizes of “real” events

d) How high the nominal dark hit rate will be.

Assume ~ 10kHz

(nominal dark rate for SK-PMT = 3 ~ 5 kHz)

Expected data rates after the software trigger

case 1) 3 compartments (N = 3)

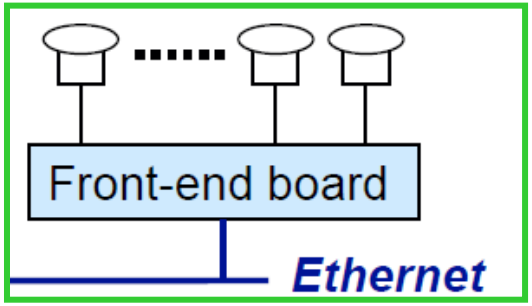
10 kHz dark, 17 k sensors / compartment

μ rate = **35 Hz** (muon rate * area ~ 18 times larger)

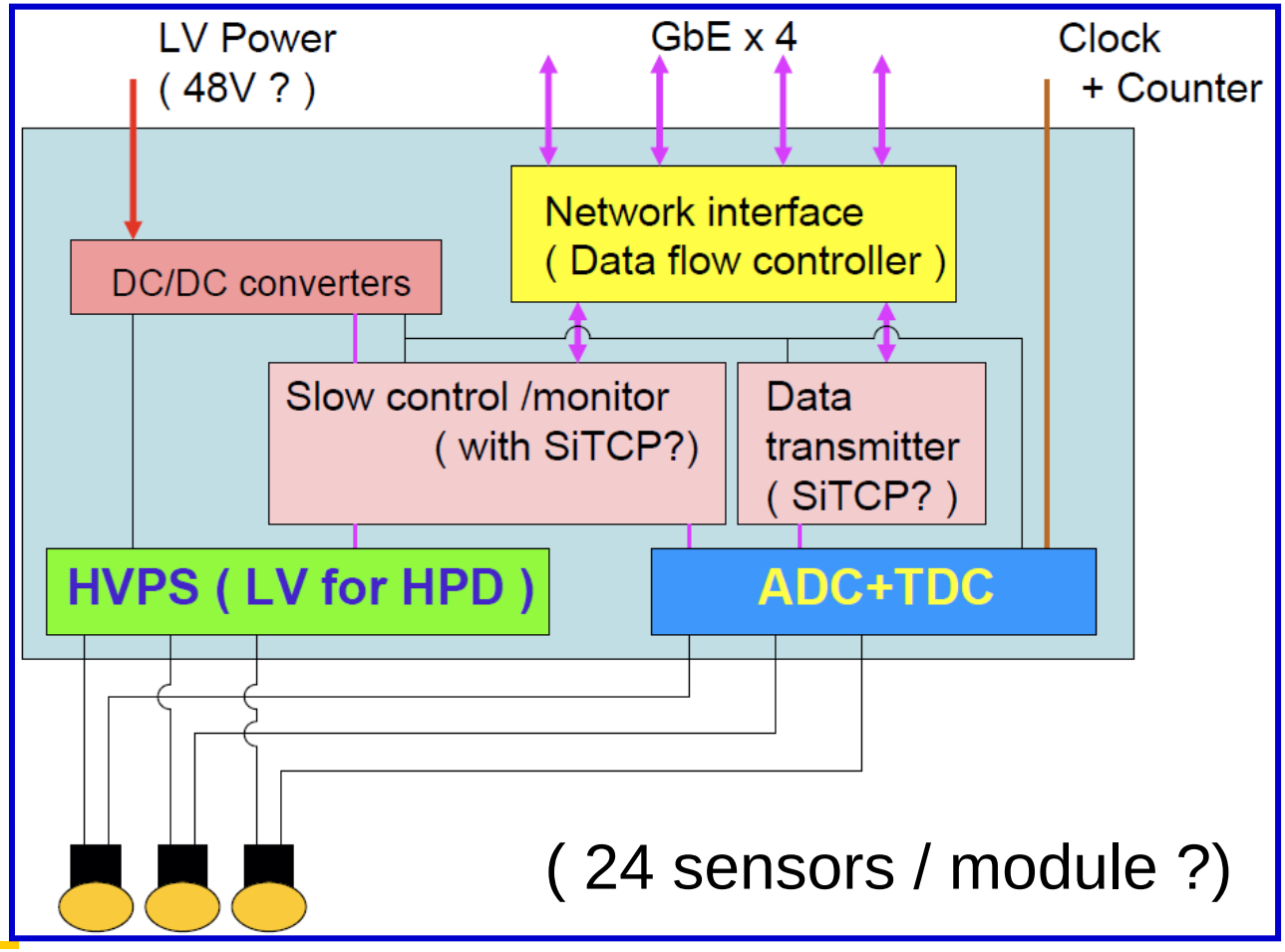
~ 15 MB/sec/compartment

~ 40 % from SLE & 40% from μ

Possible front-end electronics module connections



Schematic diagram of the front-end board



Key components

- Self triggering & dead-time free ADC + TDC
- HV (LV) for photo-sensors
- Intelligent network interfaces

In the last meeting, experts strongly recommend to keep the module DRY (not to in the water).
Detector design group want to reduce the weight of the cables….

Current designing issues ~ front-end electronics

Signals and noise shapes from the new photo-sensor (HPD)
seem to be different from normal PMT (so far.)
Bit noisy (higher dark rate),
Occasional negative (positive) noise hits,
Small dynamic range etc…

*) Current design of pre-amplifier in the HPD
is constrained due to the noises of HVPS in HPD

→ Details of the sensor are expected to be finalized in ~ 2 yrs.

- This year, try to start ***conceptual design of analog part.***
  ~ Basic studies of available QTC/(F)ADC etc.
- Realistic design of the front-end analog circuit
  can be started when the photo-sensor is finalized.

Current designing issues ~ front-end electronics

Stable, low noise compact HVPS is essential to realize HPD solution

Basic requirements for HVPS for HPD

Dimension		: 50 x 30 x 50mm3
Output voltages	: HV	: +250V ~ 10,000V (10kV)
	: LV	: HV - 500 ~ HV - 80V (LV is relative to HV)
		: (HV-LV should not exceed configured value)
Ripple		: TBD (< 10mV)
Line regulation		: 0.2% at 20% fluctuation of the Vin
Load regulation		: 1V at IOUT LV = 1uA
Max out current	:	Total 1uA
Current limit	: HV	: TBD (1 uA ?)
		(some of the special requirements are not shown here)

→ Starting R&D work of HVPS module with photo-sensor group & HPK

Near term goal ~ prototype of the electronics module

Building test detector with O(1000) channels (sensors)
in ~ 5 yrs is seriously considered.

→ Good opportunity to test
new electronics modules & DAQ system for HK

Considering timescale,
it may be difficult to prepare new analog chips
to be used for this test from the beginning.

- There are spare QTC chips for SK
  ~ we can use this for the first round.
- We don't have enough TDC chips for 1000 channels.
  (The TDC chip used in QBEE (AMT3)
  or similar chips have been discontinued.)
  → Need to start R&D of new TDC at first

- It is also important to start conceptual design
  of analog signal handling (QTC / ADC / FADC)

Near term goal ~ prototype of the electronics module

QTC/ADC specification (performance)
(current performance = minimum requirements)

• **Built-in Discriminator**	¼ p.e. (~ 0.3 mV)
• **Processing Speed**	~ 1usec/HIT
• **Charge Resolution**	~ 0.05 p.e. RMS (< 5 p.e.)
• **Charge Dynamic Range**	0.2~2500pC (0.1 ~ 1250 p.e.)
• **Timing Respons**	0.3ns RMS (@ 1p.e.) 0.2ns RMS (> 5p.e.)

TDC specification (performance)

• **Least Time Count**	0.52 ns
• **Time resolution**	250ps
• **Dynamic range**	≥15bits
• **Continuous running mode**	

Near term goal ~ prototype of the electronics module

If we can secure budget to build a test detector,
near term (~ 5yr) work may look like as follows: