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Hyper-K Electronics; FADC and Communication Options

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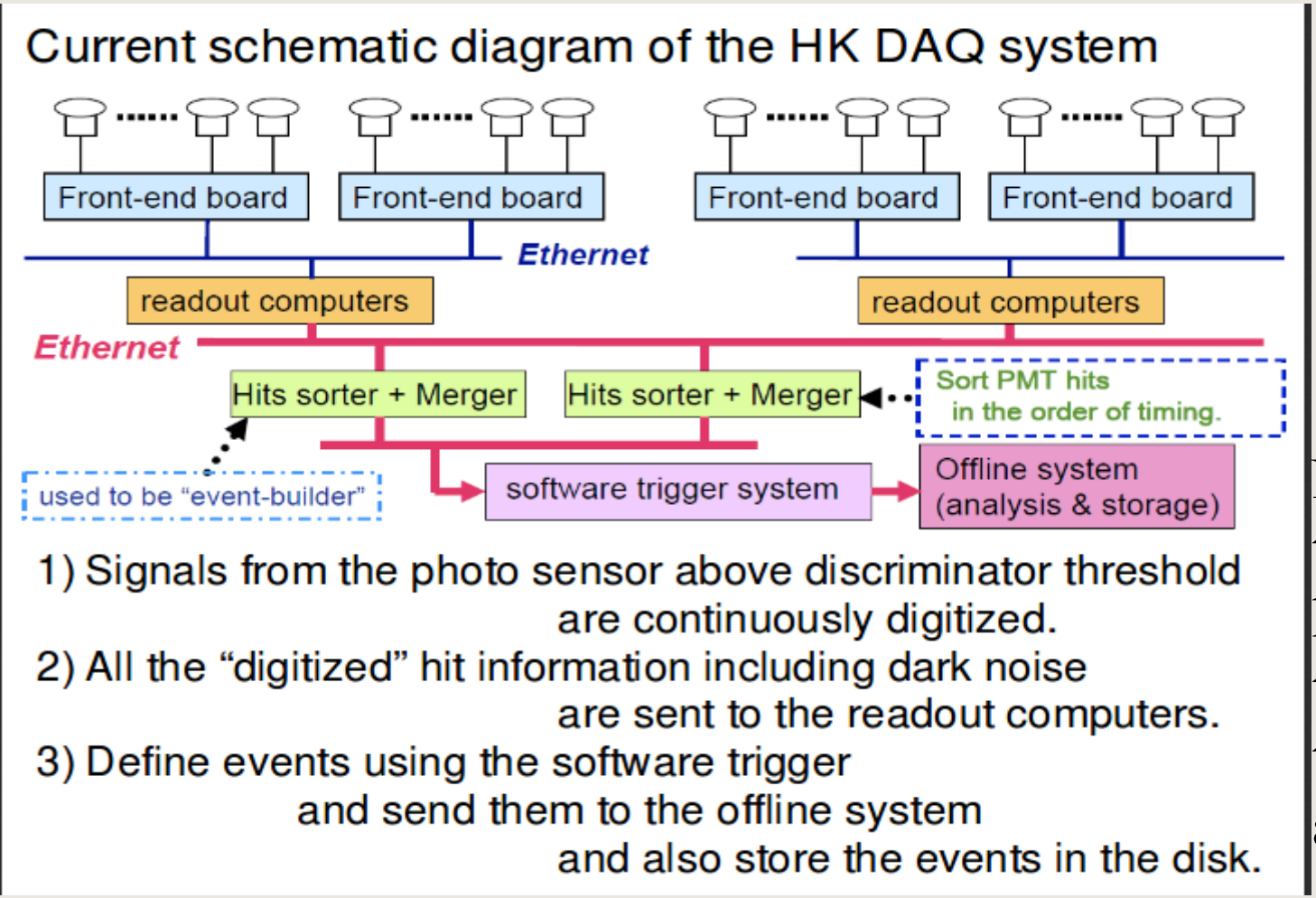
4th HK Open Meeting, Jan 2014

Overview

- Reminder of baseline HK electronics/DAQ plan
- Canadian electronics/DAQ work
  - FADC digitization
  - Communcation
- Plans for HK prototype.

Hyper-K Electronics/DAQ



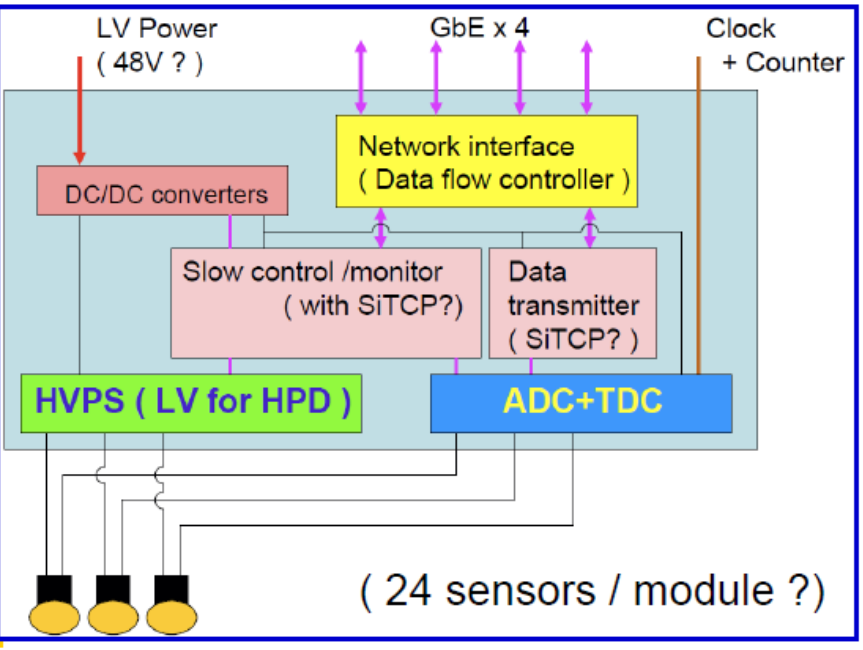
No global hardwar
triggers; all PMT
hits stream up
to PCs where
trigger decisions
are made.

Hayato-san, previous HK meetings

HyperK: Baseline Front-end Digitization

- Baseline signal digitization: TDC + ADC (like SK).
- One potential concern: the TDCs used for SK electronics are no longer available; need to find new ones.
  - Possible chips being investigated.

Schematic diagram of the front-end board



Hayato-san, previous HK meetings

HK Electroni
4th

QTC/ADC specification (performance)
(current performance = minimum requirements)

- **Built-in Discriminator** ¼ p.e. (~ 0.3 mV)
- **Processing Speed** ~ 1usec/HIT
- **Charge Resolution** ~ 0.05 p.e. RMS (< 5 p.e.)
- **Charge Dynamic Range** 0.2~2500pC (0.1 ~ 1250 p.e.)
- **Timing Respons** 0.3ns RMS (@ 1p.e.)
  0.2ns RMS (> 5p.e.)

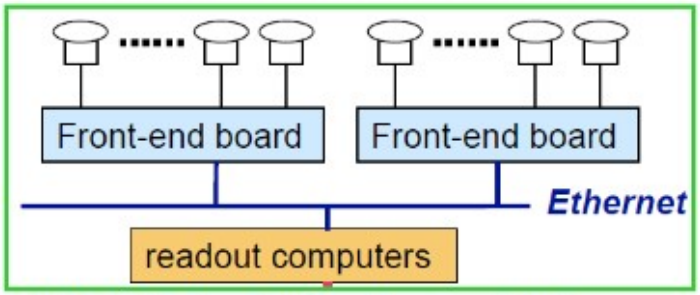
TDC specification (performance)

- **Least Time Count** 0.52 ns
- **Time resolution** 250ps
- **Dynamic range** ≥15bits
- **Continuous running mode**

Hyper-K Communication Scheme

Possible front-end electronics module connections

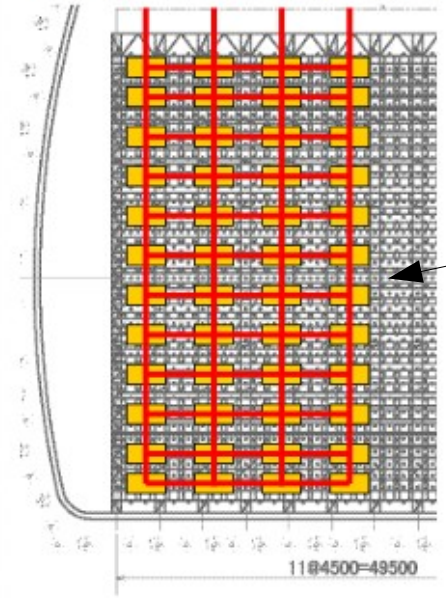
~ Design of the data flow



1) Assuming to use 1GbE

- Robustness
- Power consumption

HK detector Side view



2) Connect neighboring Front-end boards each other

- Reduce total length of the cables
- Avoid single point failure

Usually, data collected by a module are transferred to the upper module (vertically)

If a module failed, transfer data to the other module instead of the failed module (horizontally).

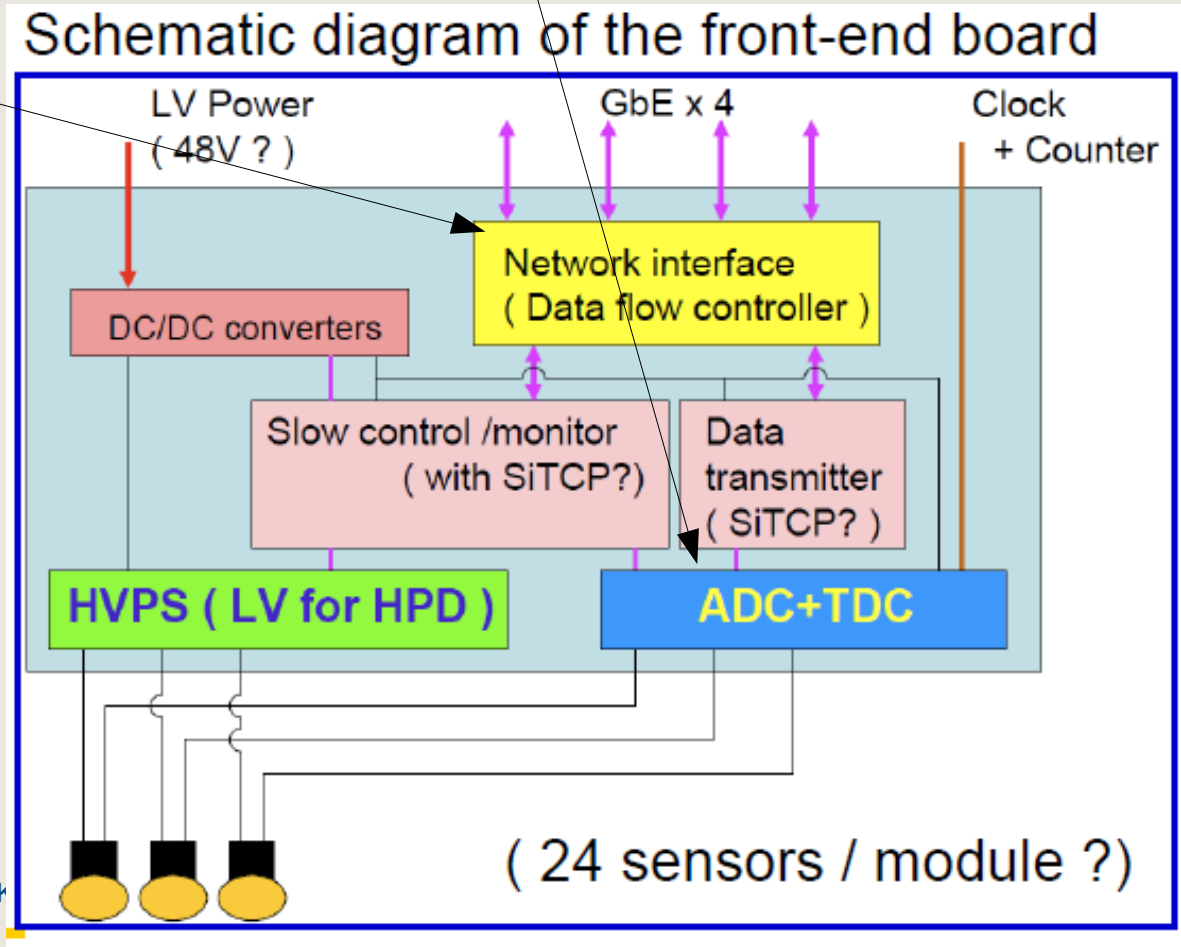
Data rate at the top modules has to be enough smaller than 1Gb/sec.

Electronics sit in water: Redundant communication needed.

Hayato-san, previous HK meetings

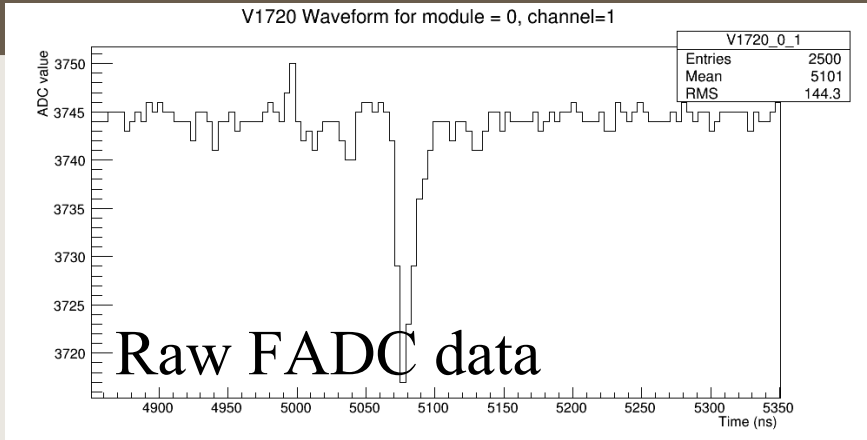
Canadian Front-end Electronics Interests

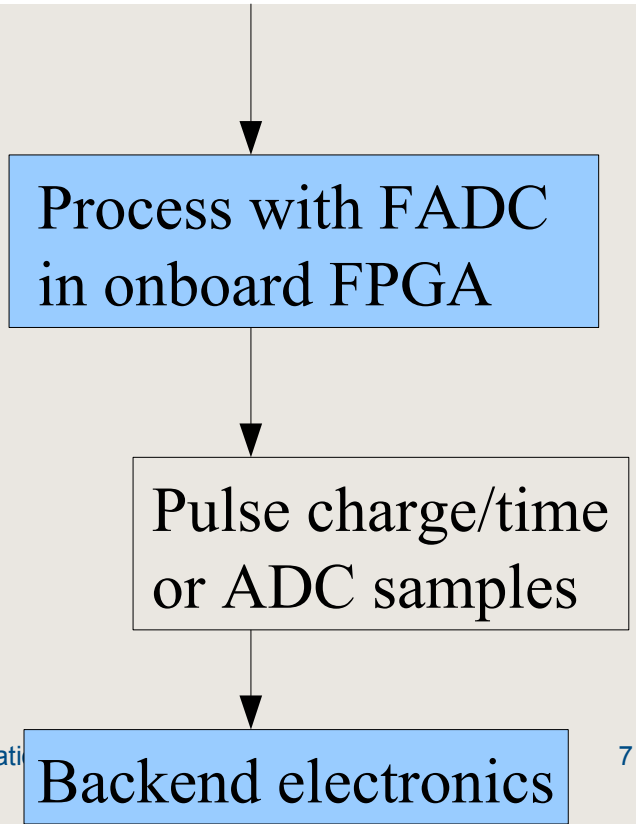
- FADCs instead of TDC/ADC for digitization
- Redundant communication protocol



FADC Option - Overview

- Proposal is to use FADC (Flash ADC) instead of TDC/ADC.
  - Something like 125-500 MHz sampling, 12-16 bit resolution.
- FADC data is continuously processed using FPGA on front-end board; firmware finds hits and only send pulse summary to backend.
  - Pulse summary is either just Q/T (for small pulses) or a set of ADC samples (for large pulses).





FADC Option - Overview

- Have experience at TRIUMF with this digitization from DEAP (dark matter) and GRIFFIN (nuclear physics).
  - Also with FPGA processing for T2K-FGD.

Pros

- More information on charge distribution 1us after first pulse.

Cons:

- Higher power (?) and cost
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

FADC Option - Overview

Current work is focused on these two questions:
1) Can we quantify gains of FADC? What physics does this help?

2) Can we meet timing resolution and dynamic range requirements? (reminder: 0.25ns resolution, 0.05-1250 PE range)

Pros

- More information on charge distribution 1us after first pulse.

Cons:

- Higher power (?) and cost
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

FADC Benefits

What benefits do you get from more detailed/dead-timeless FADC digitization?

1) Improved decay electron and delayed neutron tagging (compared to QBEE electronics).
2) Possible improvements to prompt ring measurements: better PID.
   - Initial tests (turning off indirect light) doesn't show improvement, but will continue tests.

FADC Benefits II

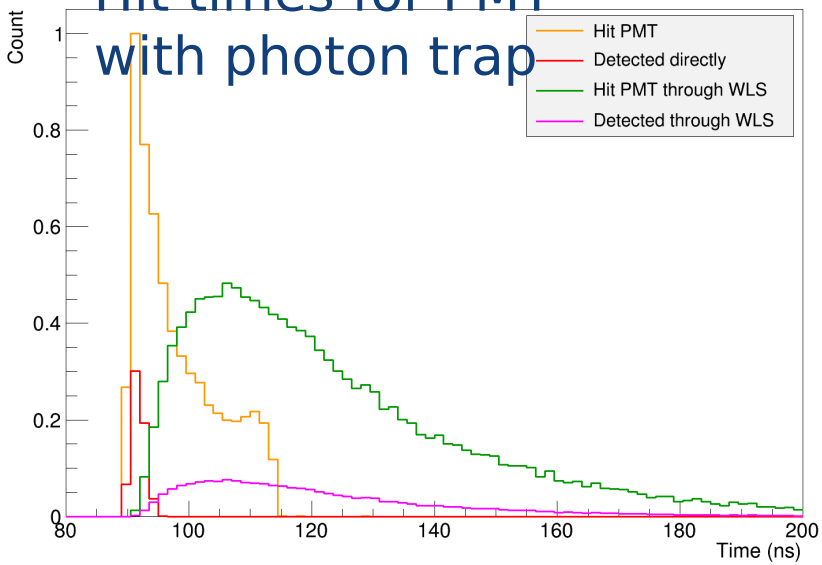
3) Combine FADC with PMT photon trap*: the photon trap provides extra light collection, but WLS photons are delayed.

-> FADC digitization provides a method of measuring the direct photons separately from the WLS photons. Allow reconstruction to treat direct vs WLS photons separately, mitigating possible concerns about including photon trap.

4) If reused for ND, FADC is also good for distinguishing different interactions within a bunch.

-> Also good for water-based scint.

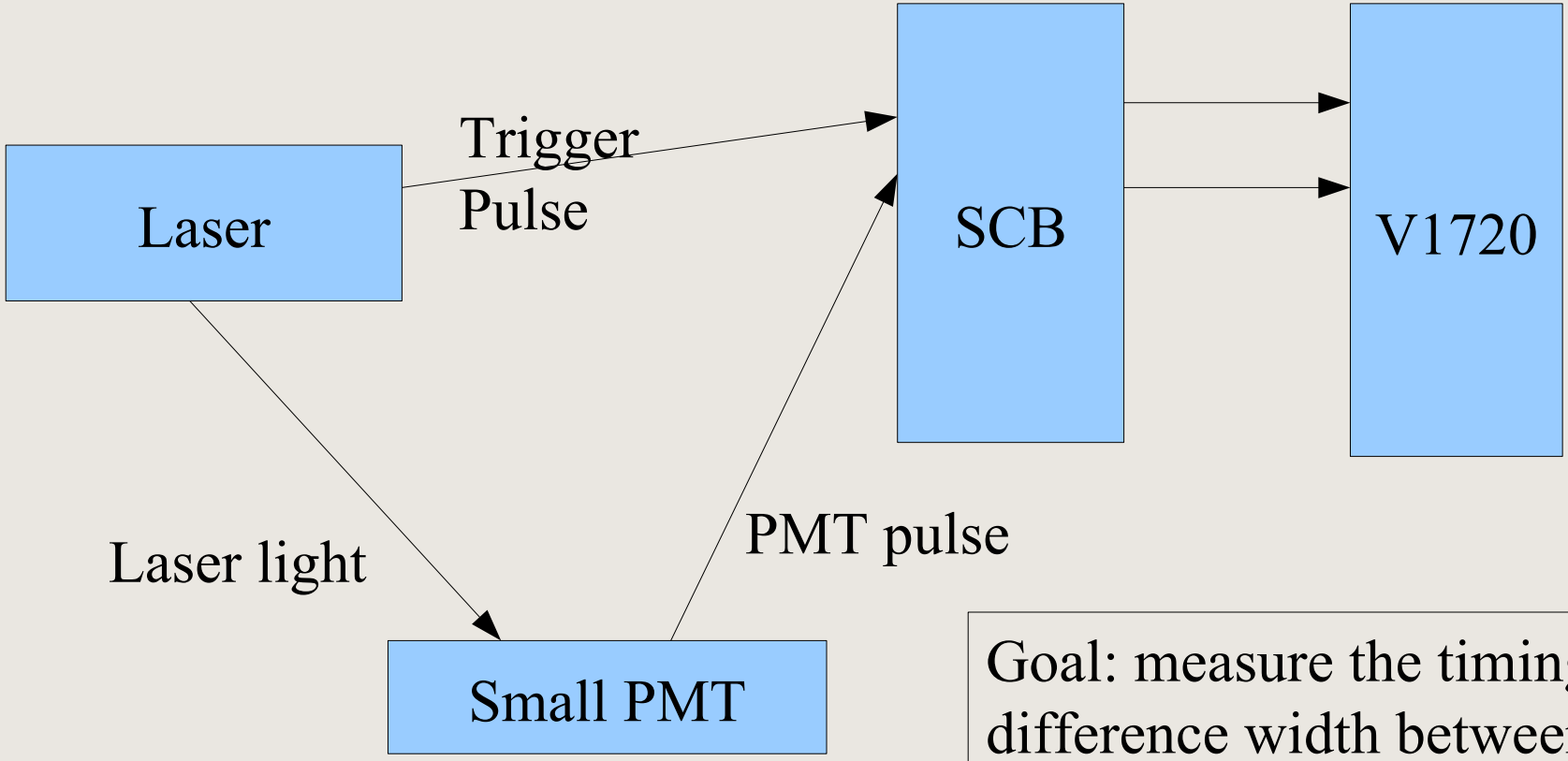
*See Poutissou, Retiere talk.



FADC Test with DEAP Electronics

- Did quick test of FADC timing resolution using DEAP electronics setup at TRIUMF.
- DEAP using CAEN V1720 to digitize PMT signals.
- V1720 is a 12-bit, 250 MHz FADC.
- DEAP PMT signals are put through a custom Signal Conditioning Board (SCB) to shape the pulse V1720.
- Not proposing using this CAEN module for HK, but the technology would be similar.

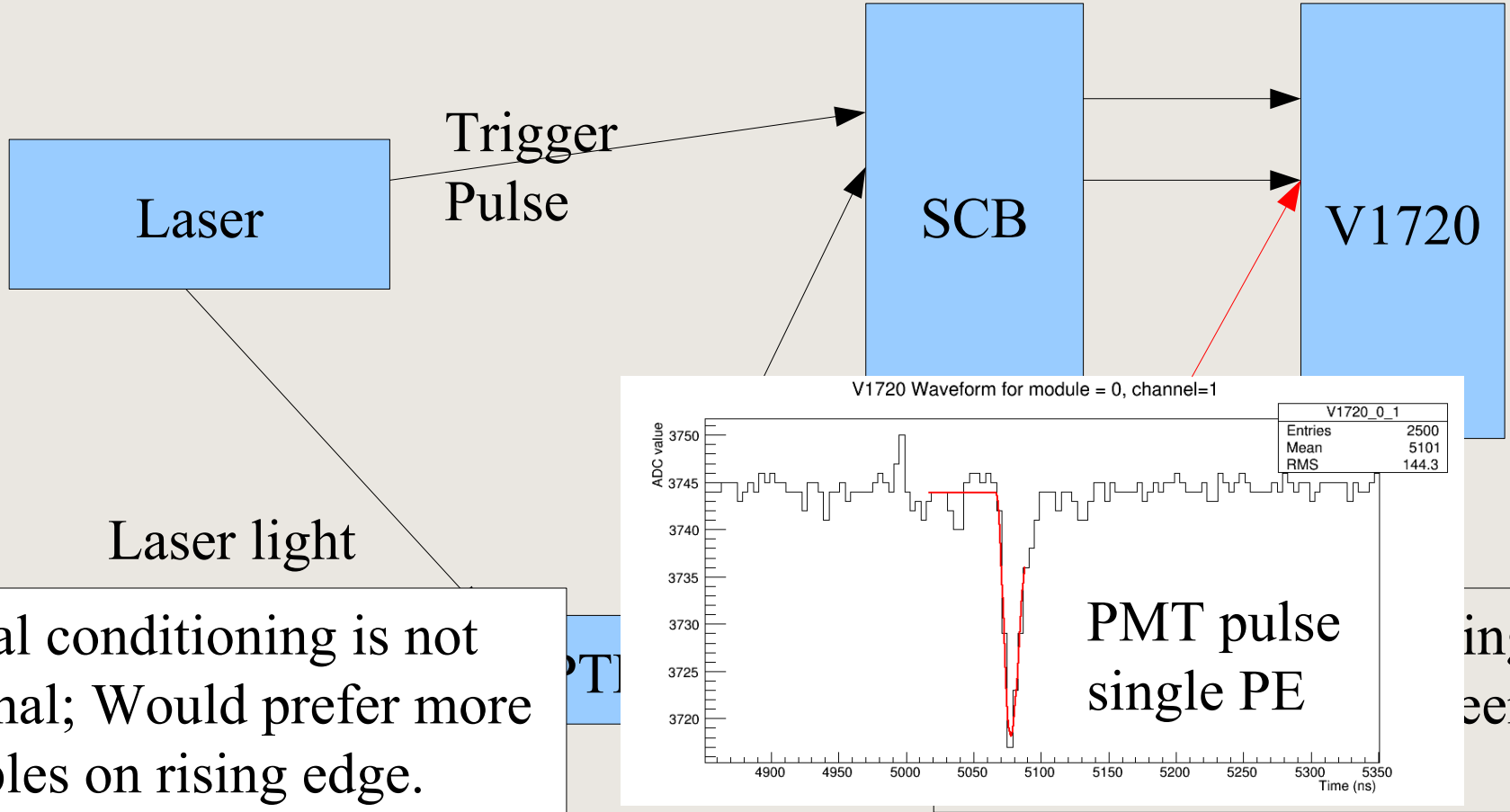
Timing Test Setup



Goal: measure the timing difference width between trigger and PMT pulses.

Hamatsu R9980U 16mm PMT;
small time jitter.

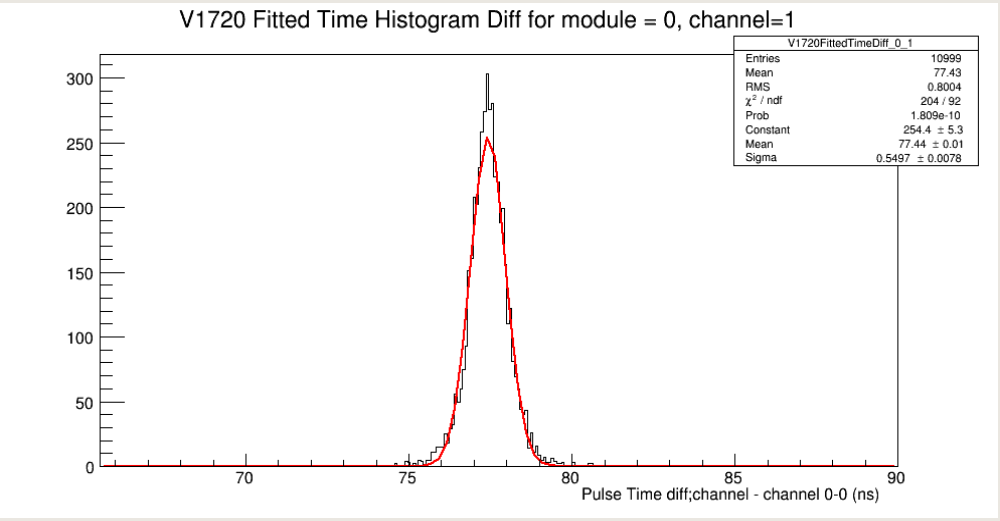
Timing Test Setup

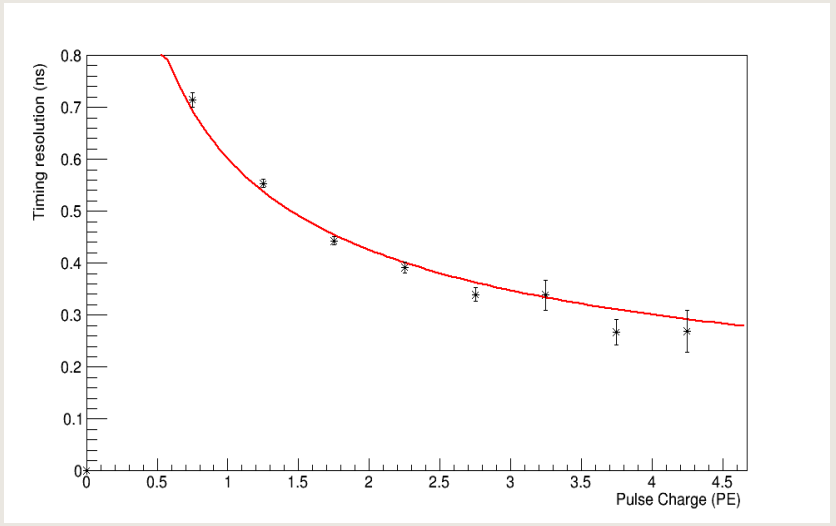


Signal conditioning is not optimal; Would prefer more samples on rising edge.

Timing Resolution

- Histogram the difference between the fitted PMT signal time and reference time.
  - Note: time fits done offline, not in firmware.
- The distribution width is ~0.6ns; even if width is totally from the PMT signal, this is still promising.





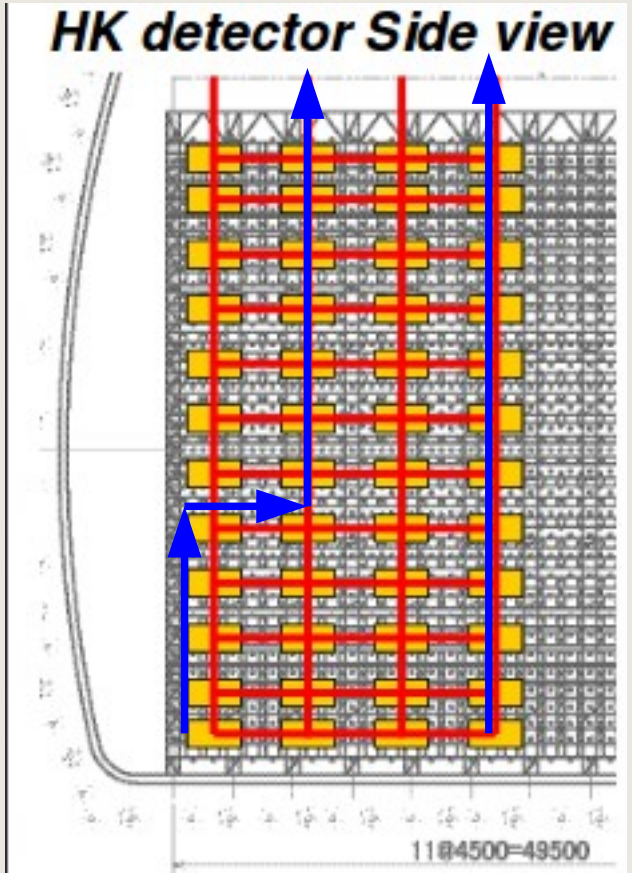
Timing resolution vs pulse charge. Expected 1/sqrt(Q) form.

FADC Timing Test Summary

- Initial results with test are promising; can get reasonable 0.6ns resolution for pulses that are 1 PE.
- Further work:
  - Improve the signal conditioning; stretch the pulse more to get more samples on rising edge.
  - Understand what dynamic range this solution provides; don't think that dynamic range is acceptable (only ~200PE). Consider further options:
    - Attenuate pulse more.
    - Split into high and low gain channels (higher power/cost).
    - Extrapolate charge for saturated pulses.
    - Non-linear amplifiers.
    - Faster (500 MHz) or more precise (14-bit) FADC.

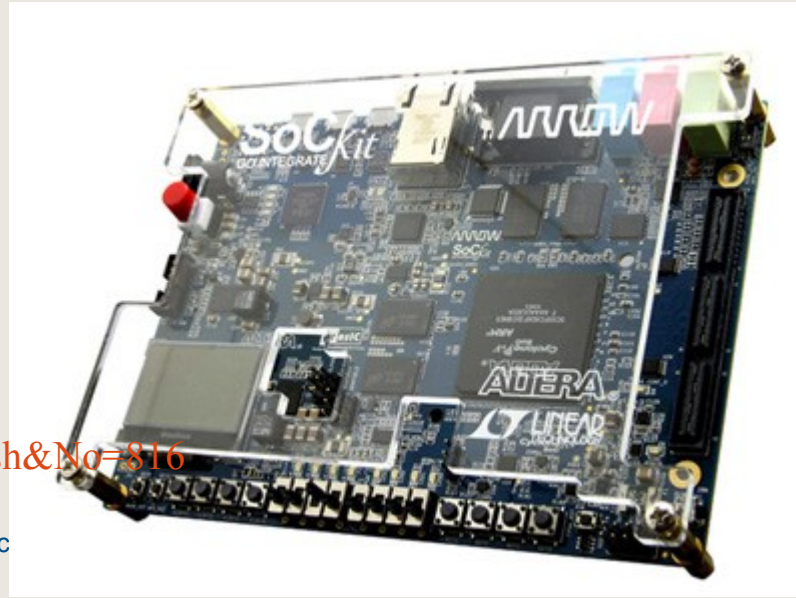
Communication Work

- Have a set of four UBC engineering students who are working on some tests of a possible communication scheme based on RapidIO protocol.
- RapidIO is alternative to ethernet/TCP-IP protocol.
- RapidIO seems interesting because it allows ways of specifying routing of data packets.
- Could use this functionality to route packets for redundant mesh network.



RapidIO Test

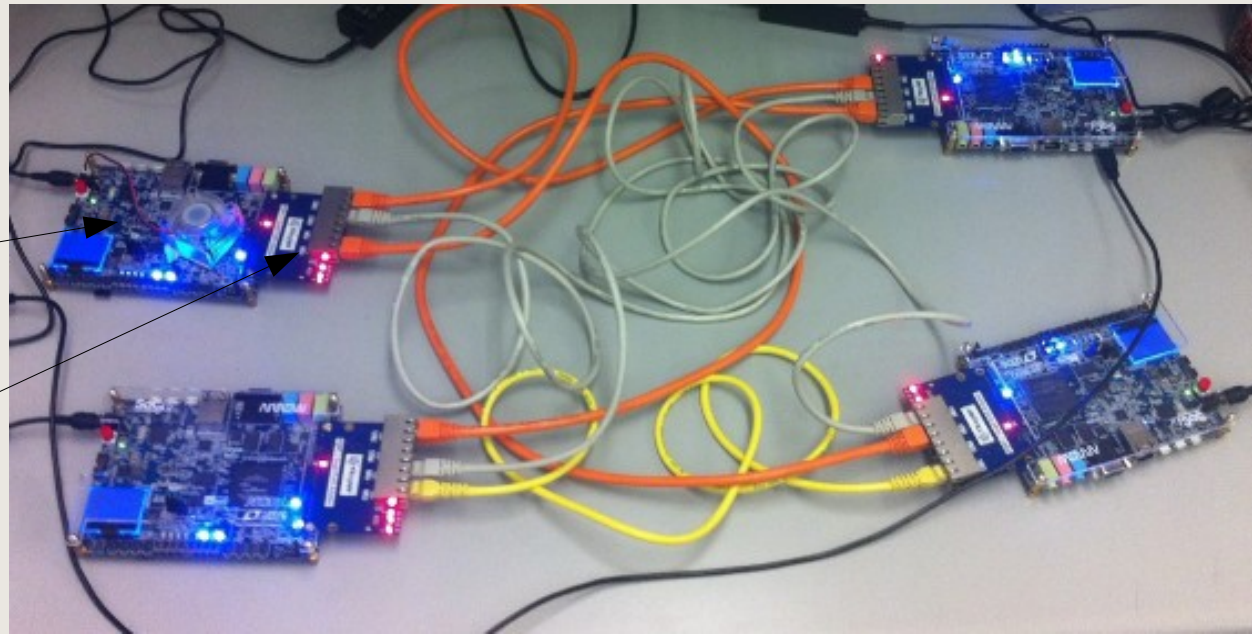
- Plan is to test of the RapidIO communication using a set of ~10 Altera FPGA evaluation boards.
  - Specifically Terasic evaluation board with Altera FPGA (with NIOS CPU) and dual ARM processors.
  - Made custom extension card to allow 5 cat-6 cables to attach to each board.
- Hopefully students will also compare RapidIO to other possible protocols (ie ethernet).



http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=816

RapidIO Test II

- Implemented 4 RapidIO cores in FPGA on each board; each RapidIO core has associated DMA engine.
- Managed to get each of 4 links running at 135MB/s; can also run faster, near 250MB/s, but needs to tweak DMA.
- Starting to work on the routing functionality; did some tests already, checking fail-over when cables are detached.



Plans for HK Prototype

- We hope to test the FADC digitization and communication scheme for some/all of the HK prototype electronics.
  - Making funding request to make this possible.
- Need to understand how the overall electronics will be provided; useless to provide digitization for PMTs that have no HV.
  - Had useful discussions yesterday about division of work.

Conclusions

- We are interested in FADC digitization and communication for HK front-end electronics.
- Focus of FADC work has been on defining benefits of scheme and understanding how to achieve necesary timing resolution.
- Work starting on testing RapidIO as communication protocol.
- We hope to integrate these elements in the HK prototype electronics.

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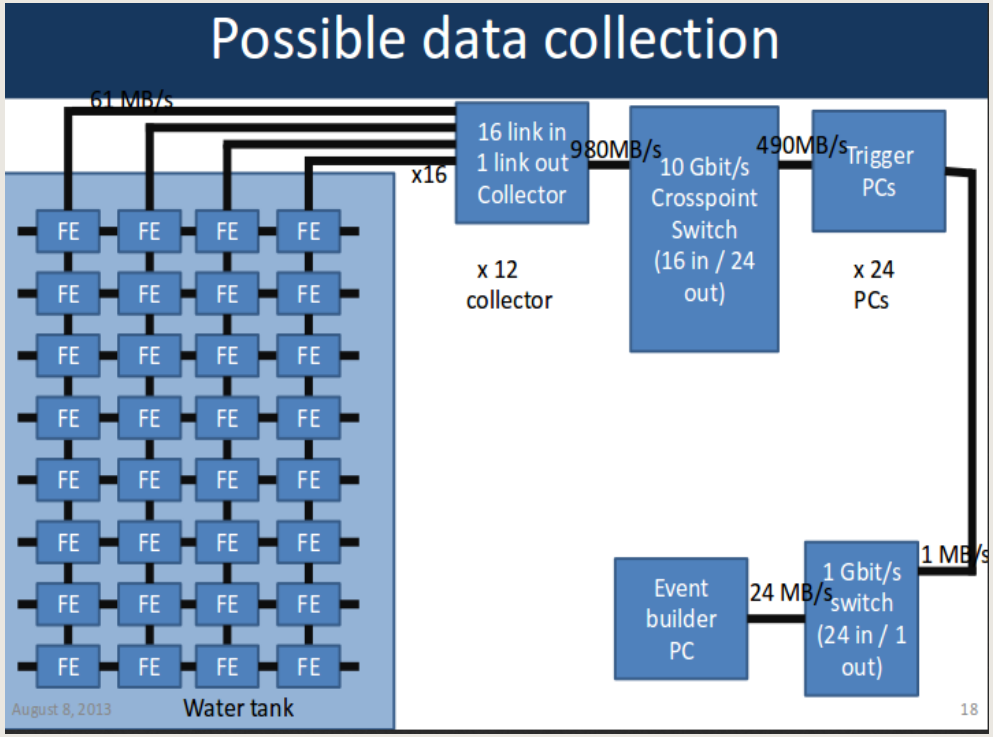
Backups

Back-end Architecture

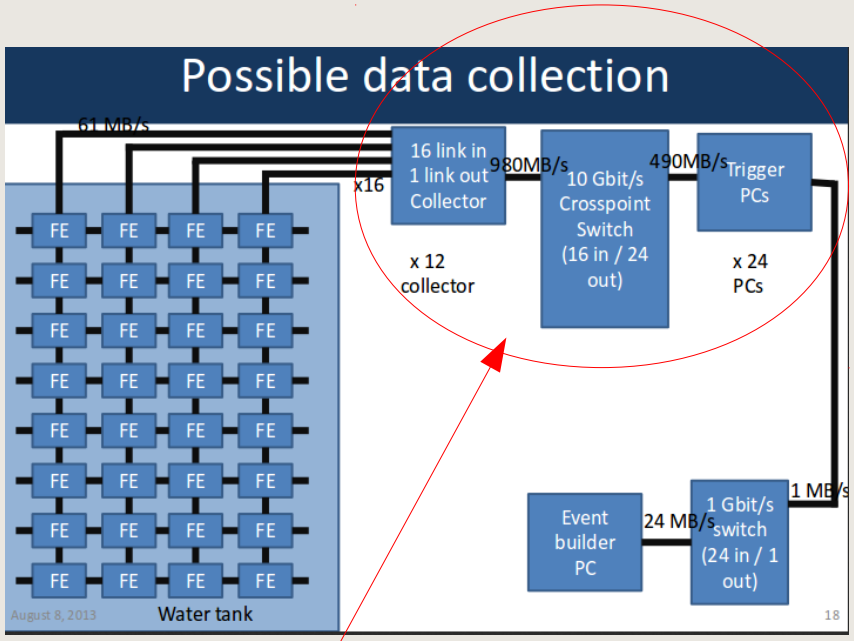
- Fabrice picture for possible back-end architecture.
- Data from front-end electronics get time-sliced and sent to different PCs.
- PCs make trigger decisions and decide if event(s) get logged to disk.



Back-end Data rates

- Maximum 12GB/s for rate.
  - This dominated by the rate for the dark noise:

    10 kHz dark rate * 100k channel * 12 bytes per hit
  - But that is without compartmentilization; rate could be lower, near 1GB/s from a compartment.



- Details of backend architecture depend on these details quite strongly.