

DAQ session
~ introduction ~

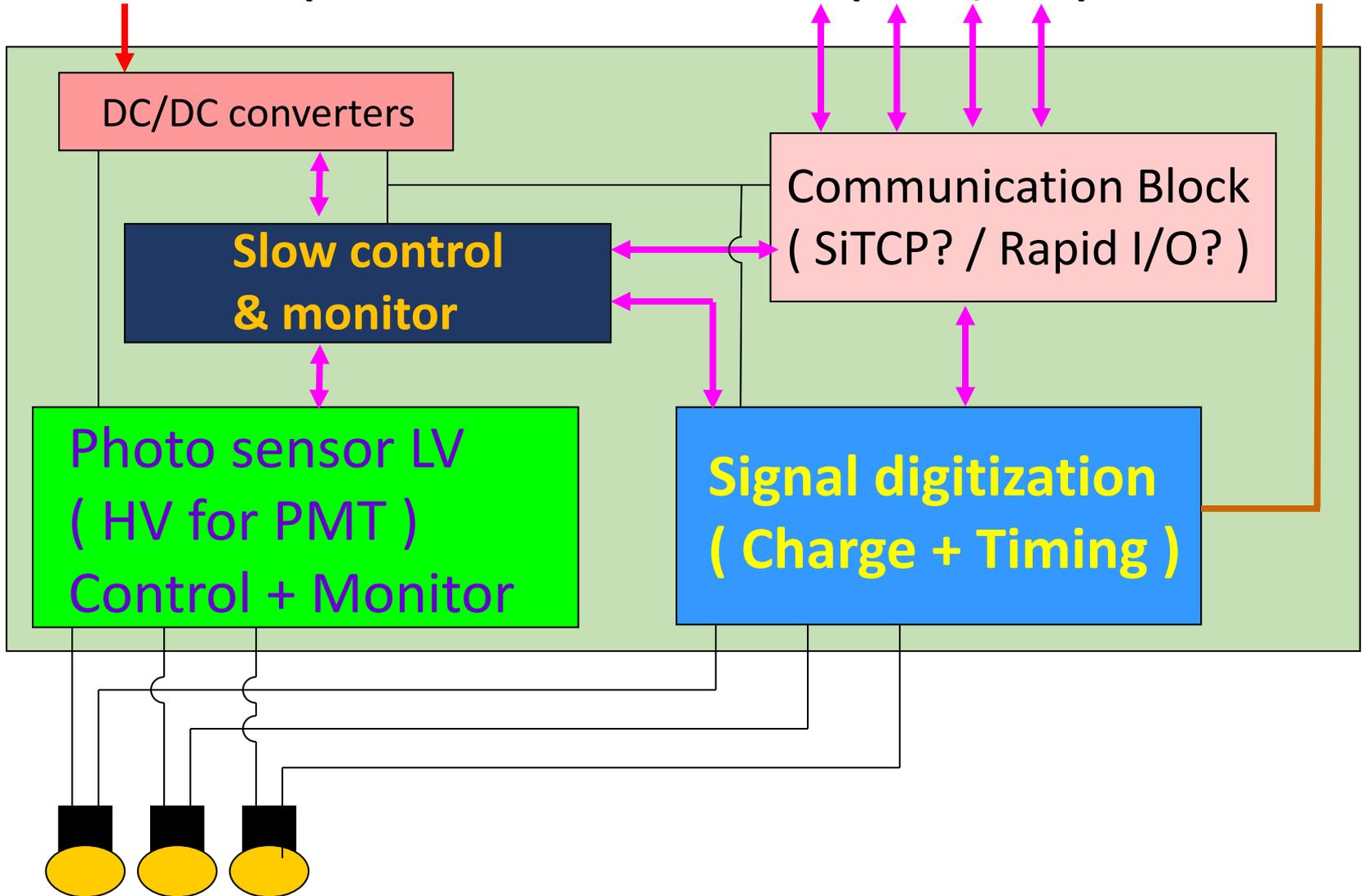
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Schematics ~ Components ~ Work package

Power
(48V ~ 100V ?)

Data + Control lines
(~ Gb/sec)

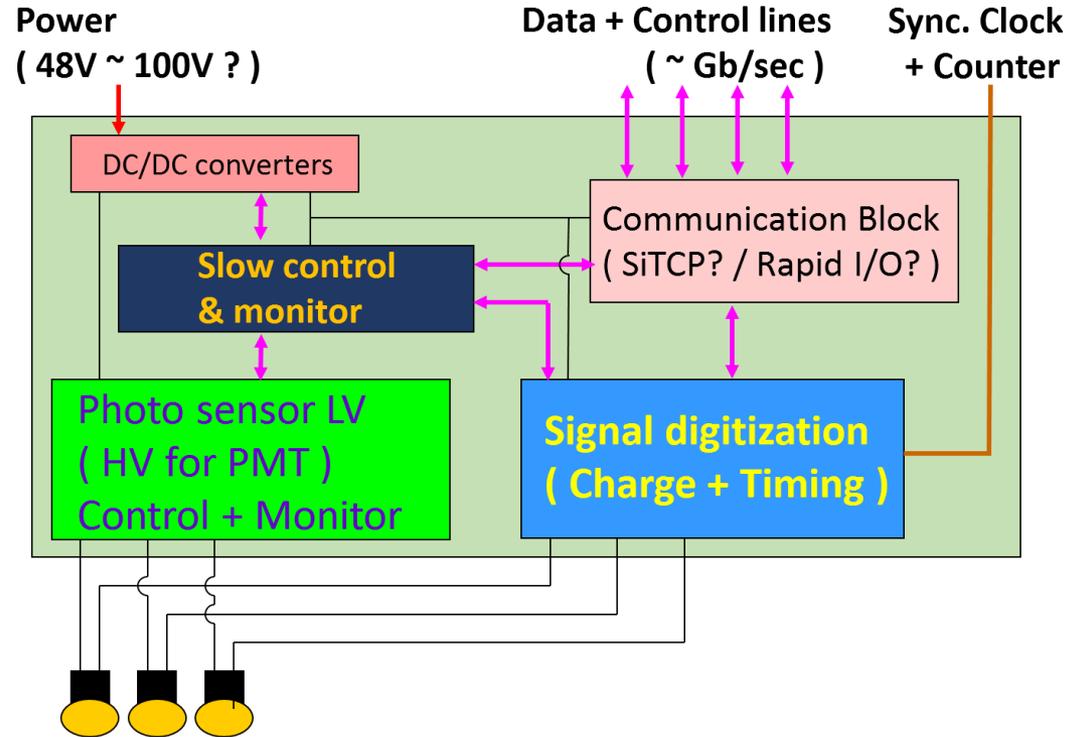
Sync. Clock + Counter



Schematics ~ Components ~ Work package

List of items

- Signal digitization
 - ~ QTC + TDC
 - ~ FADC
- Communication block
 - ~ SiTCP
 - ~ Rapid I/O
 - ~ Rocket I/O
- Slow control & monitor
- Timing (clock) distribution + Synchronization
- Water tight case, connectors and cables



For the prototype-test, having multiple implementations (solutions) would be nice for the feasibility and performance evaluation

However, we need to have a “working” system

coordination : Next thing to do before the next meeting

Recent status

HPD related

Several improvements are expected

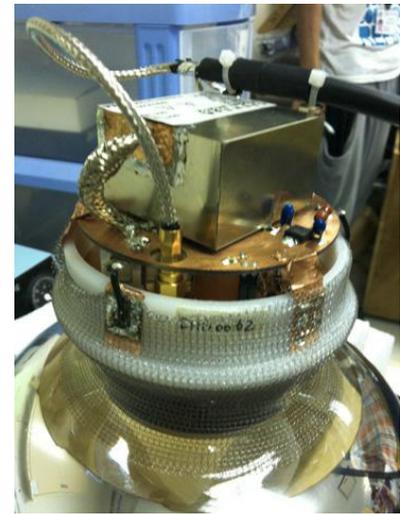
- Noise from the high voltage PS
Noise was much reduced
in the new HV module.

Several other companies are making prototypes.
(independent design)

- Pre-amplifier in HPD

Design of the new pre-amplifier was started.
(Performance of the previous revision was limited
to overcome the external noises.)

Try to maximize the performance of the HPD sensor.
Initial version is expected to be evaluated
by Sept. 2014.



Recent status

DAQ group

Previously, the groups from Japan, Canada, UK and US
have started R&D.

Reports from Canadian and UK groups will follow.

Polish group recently expressed interests in joining.

Activity in Japan

- 1) HPD Pre-amplifier design (as briefly mentioned)
(collaboration with HPD group & HPK)
- 2) HPD High voltage power supply (alternatives)
- 3) Gbit SiTCP (FPGA based TCP stack without CPU core)
Already used in various experiments.
We are also trying to use in the board for SK.

Recent status

Activity in US

TDC R&D

High precision FPGA based TDC R&D in FNAL
(Wave Union TDC by W. JinYuan et al.)

~ To be used in g-2 experiment

Performance

MSB < 20 ps with 400MHz chip
(AMT3 : 520 ps)

Resolution < 30 ps
(AMT3 : 250 ps)

Power < ~30 mW/channel