Next Generation Digital Optical Modules (DOMs)

Perry Sandstrom

For WIPAC Hardware Group

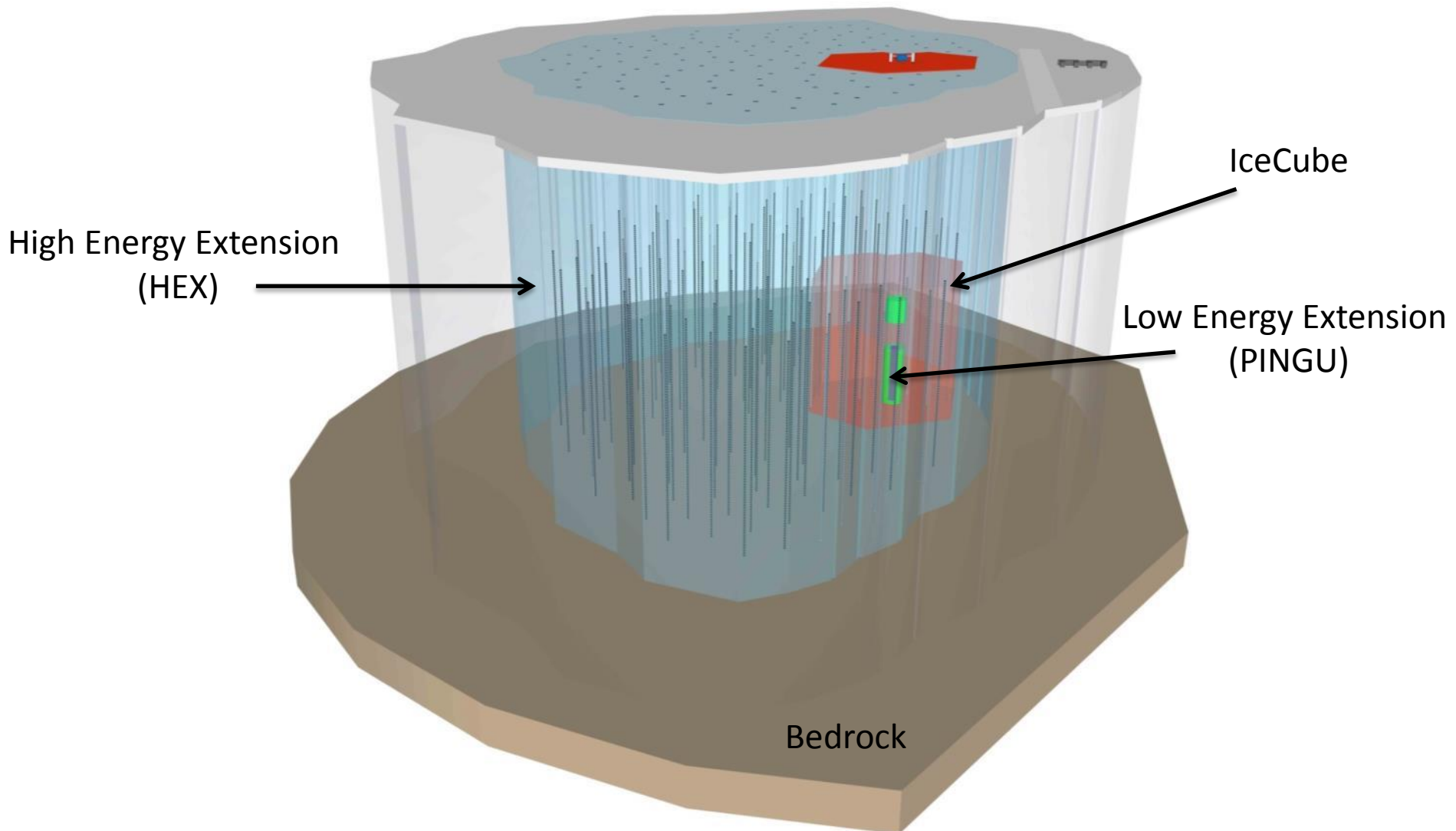7/21/14

WISCONSIN
UNIVERSITY OF WISCONSIN–MADISON

WIPAC

NSF

DOM Deployment

The IceCube Neutrino Observatory

IceCube laboratory building (ICL)

IceTop cosmic ray surface array

50m

- Volume= ~1km^3 of polar ice
- 5160 DOMs on 86 strings
- 17m DOM-DOM spacing
- 125m string-string spacing
- Completed in December 2010

1450m

Instrumented region

Eiffel Tower (324m) for scale

2450m

Bedrock
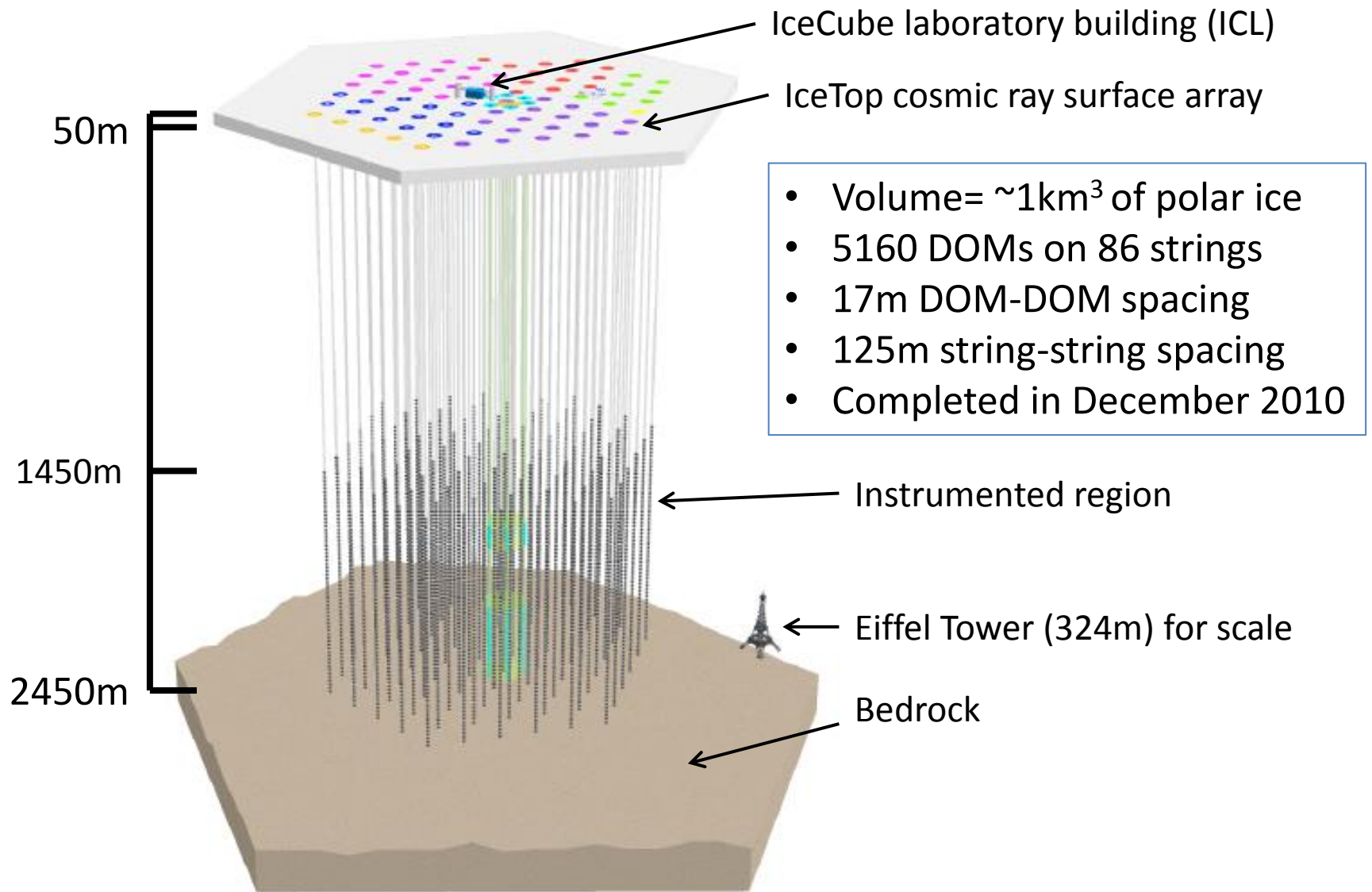
Possible Extensions to IceCube

IceCube

High Energy Extension
(HEX)

Low Energy Extension
(PINGU)

Bedrock

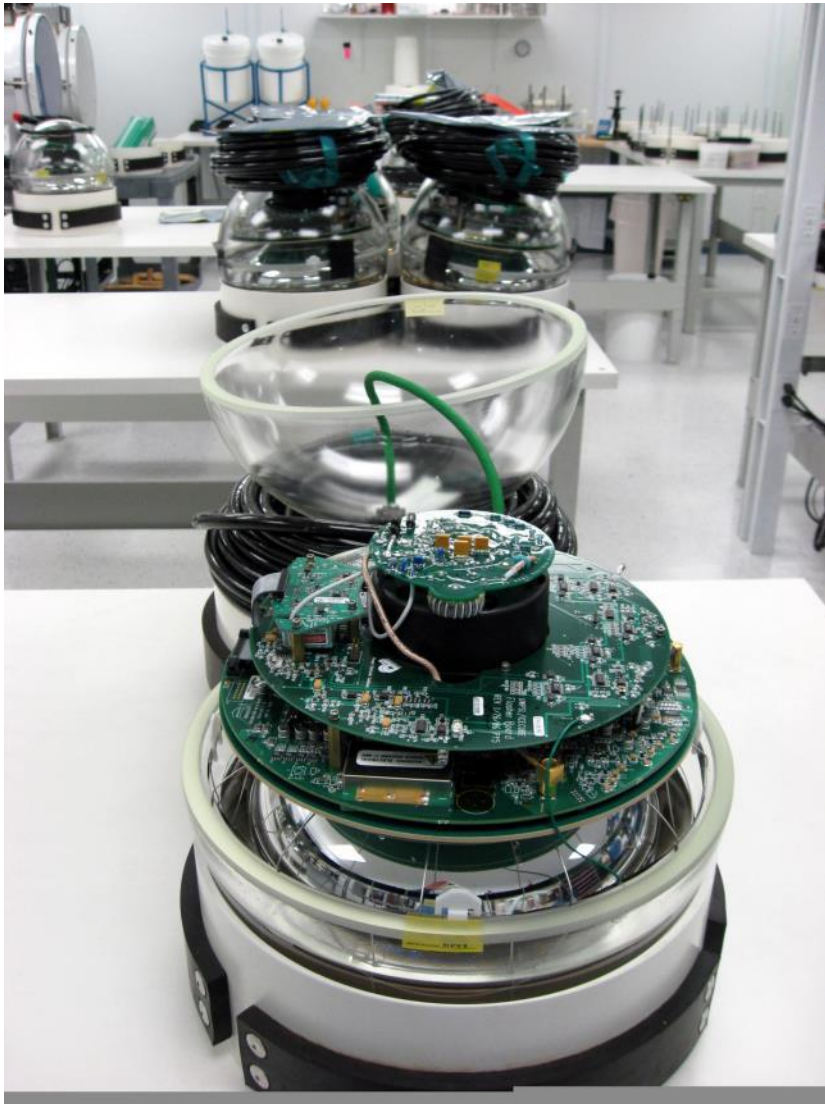"PINGU" = **P**recision **I**ceCube **N**ext **G**eneration **U**pgrade

4

Total of 5160 DOMs now frozen into the icecap

> 99% Survived Deployment

IceCube DOM Fabrication (3-sites)

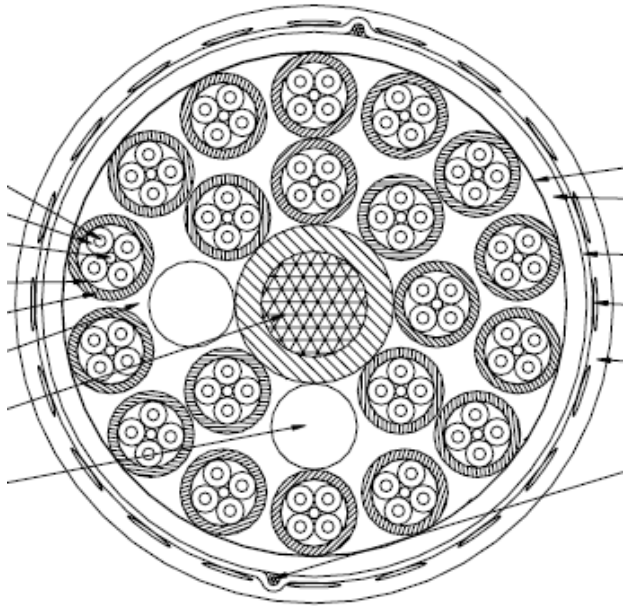## Quality of this design was a major key to IceCube's success

- Records PMT Waveform of every "hit"
- Timing synchronization between all DOMs <2ns
- Data/Timing/power over 3.3 km copper pair
- Power consumption ~3W
- Withstand > 8000 PSI freeze-in pressure
- Survive shock-vibration; ships, planes, sleds
- Built-in gel cushioning for PMT & electronics
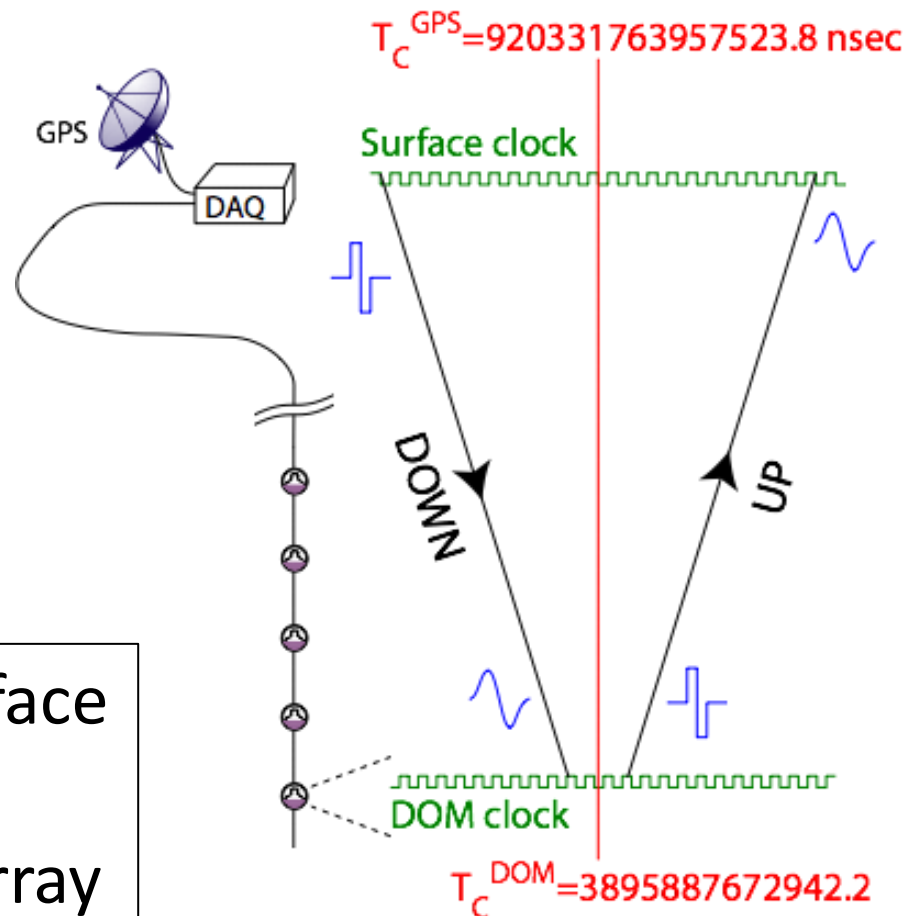- ESD proof
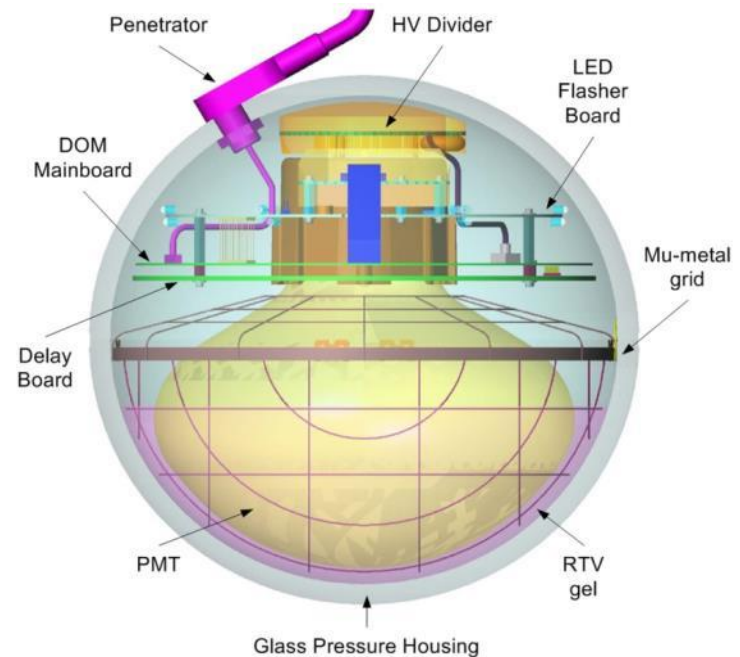
Remote Power, Communications and Timing

Everything happens over *3km long* AWG#19 copper pairs

**46mm Diameter
Downhole Cable**

**RAPCAL
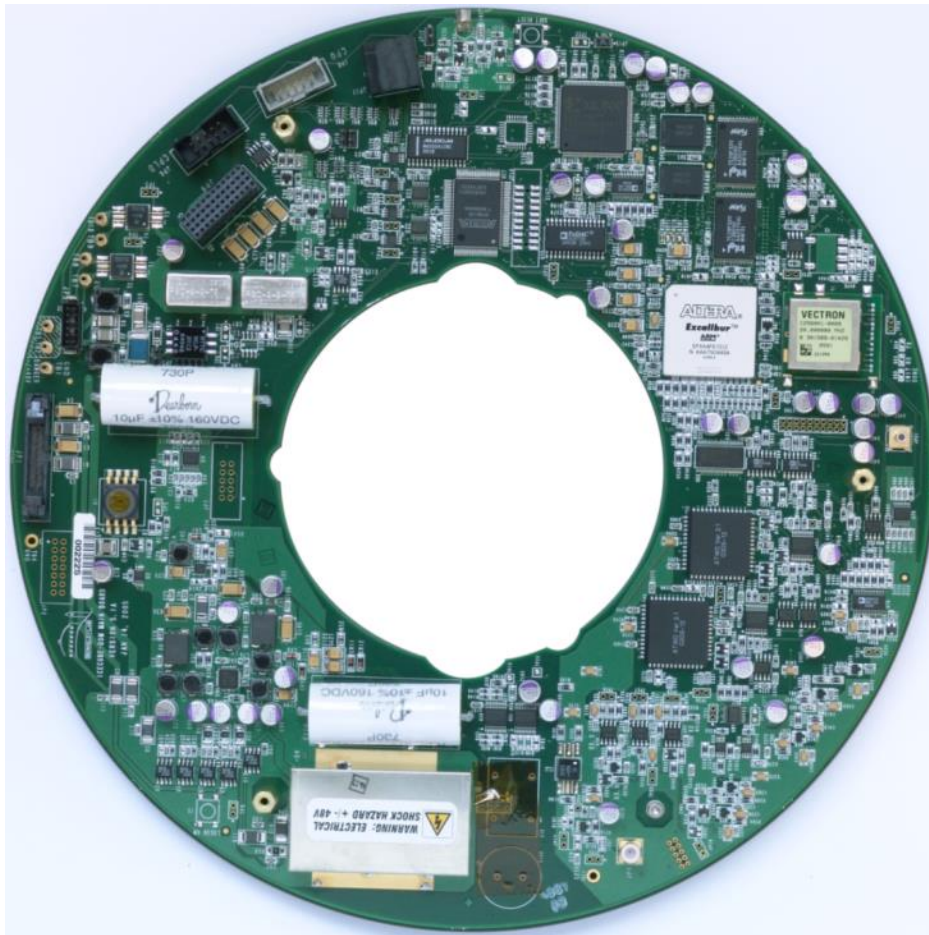Reciprocal Active Pulse CALibration**

$T_C^{GPS} = 9203317763957523.8$ nsec

Surface clock

GPS

DAQ

DOWN

UP

DOM clock

$T_C^{DOM} = 3895887672942.2$

Power: 100V supplied at surface
Comms: 1Mb/s, half duplex
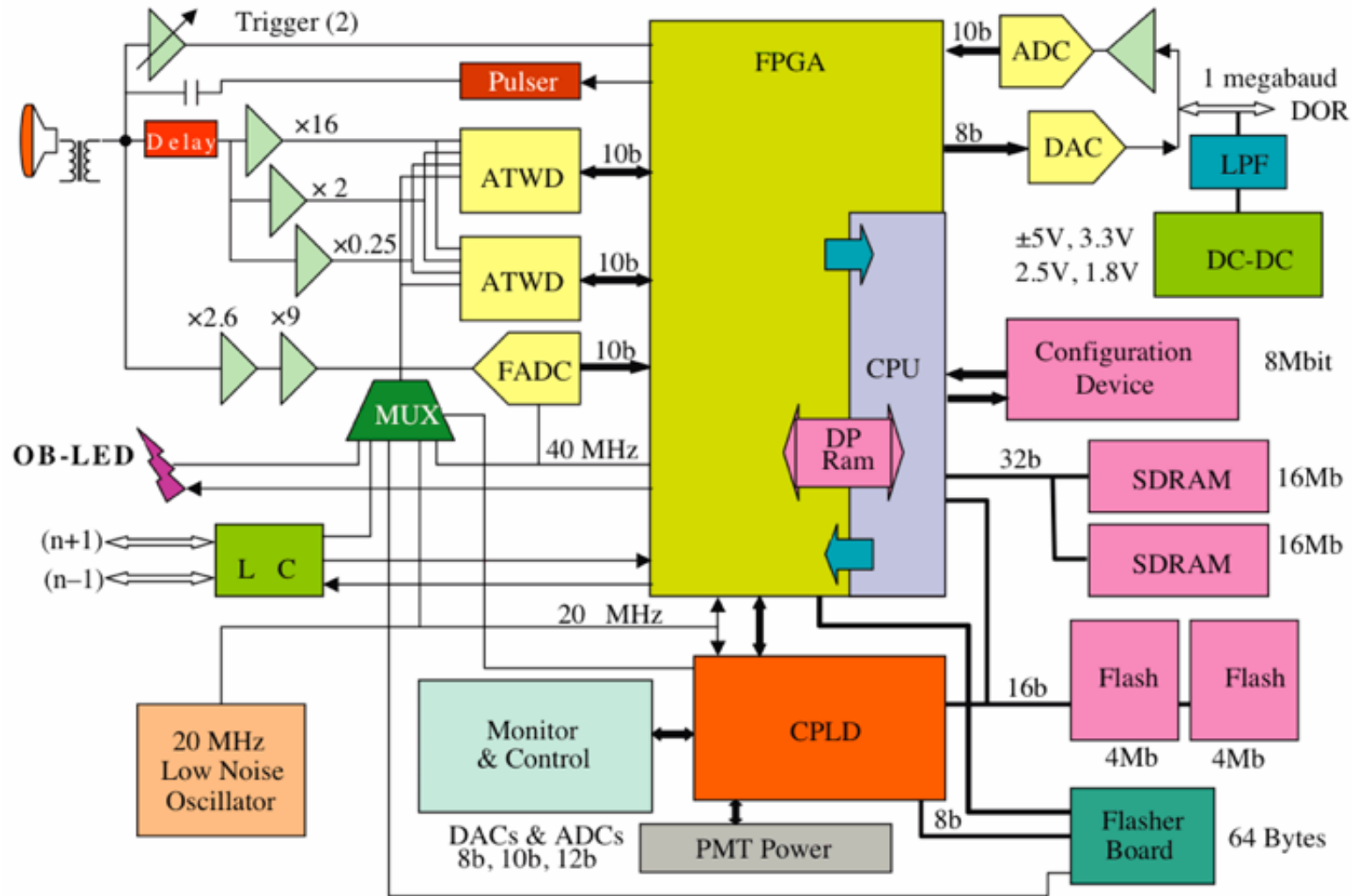Timing: <2ns across whole array

IceCube DOM Main board (LBNL)

- High Reliability Components
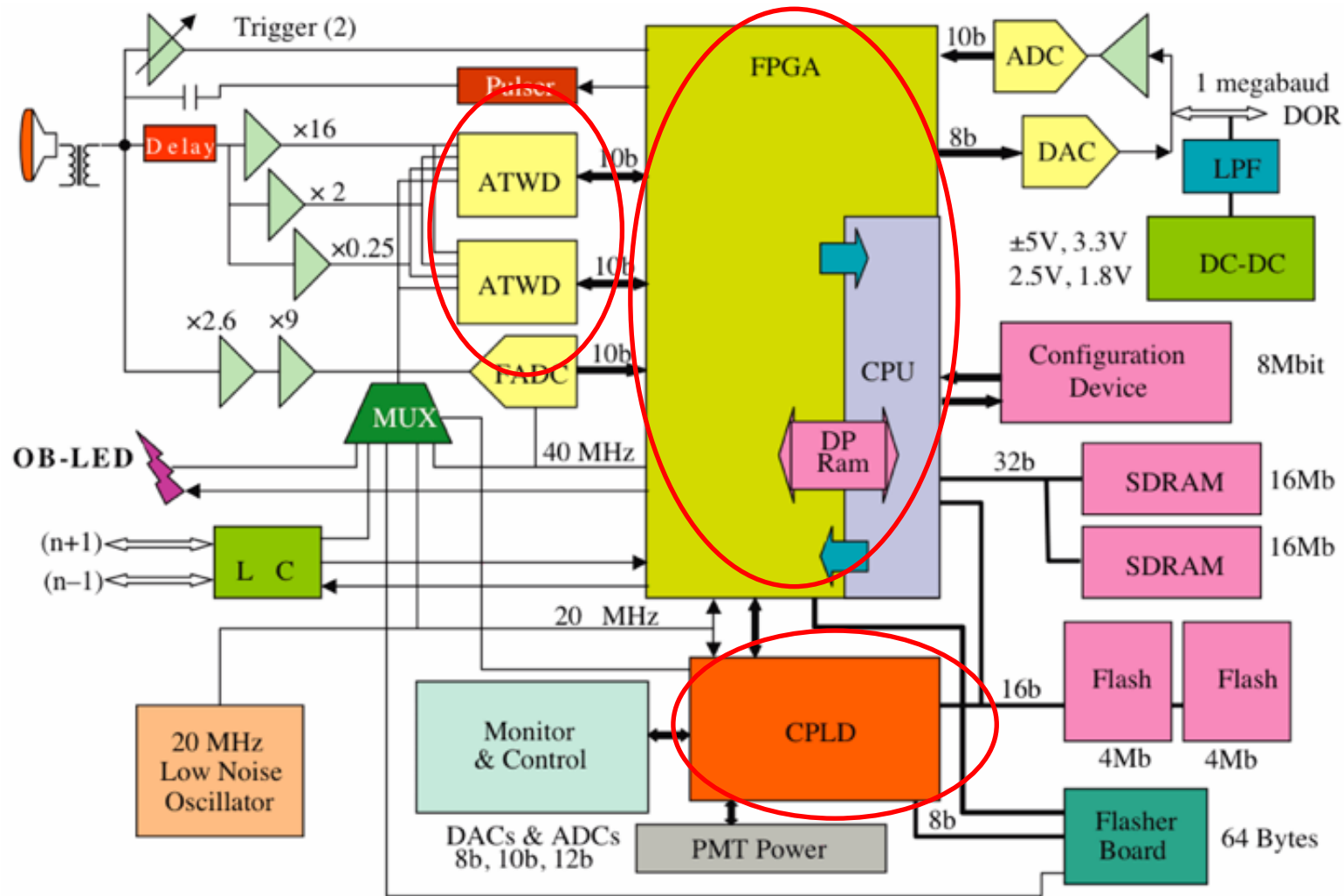- Thorough design verification
- ~5 (early) revisions then FROZEN
- DFM- Design for Manufacture
- Good vendor for PCB assembly
- IPC610 Class2 on Class3 line
- PCB: IPC Class3 w/no rework
- HASS screening (Temp & Vibration)
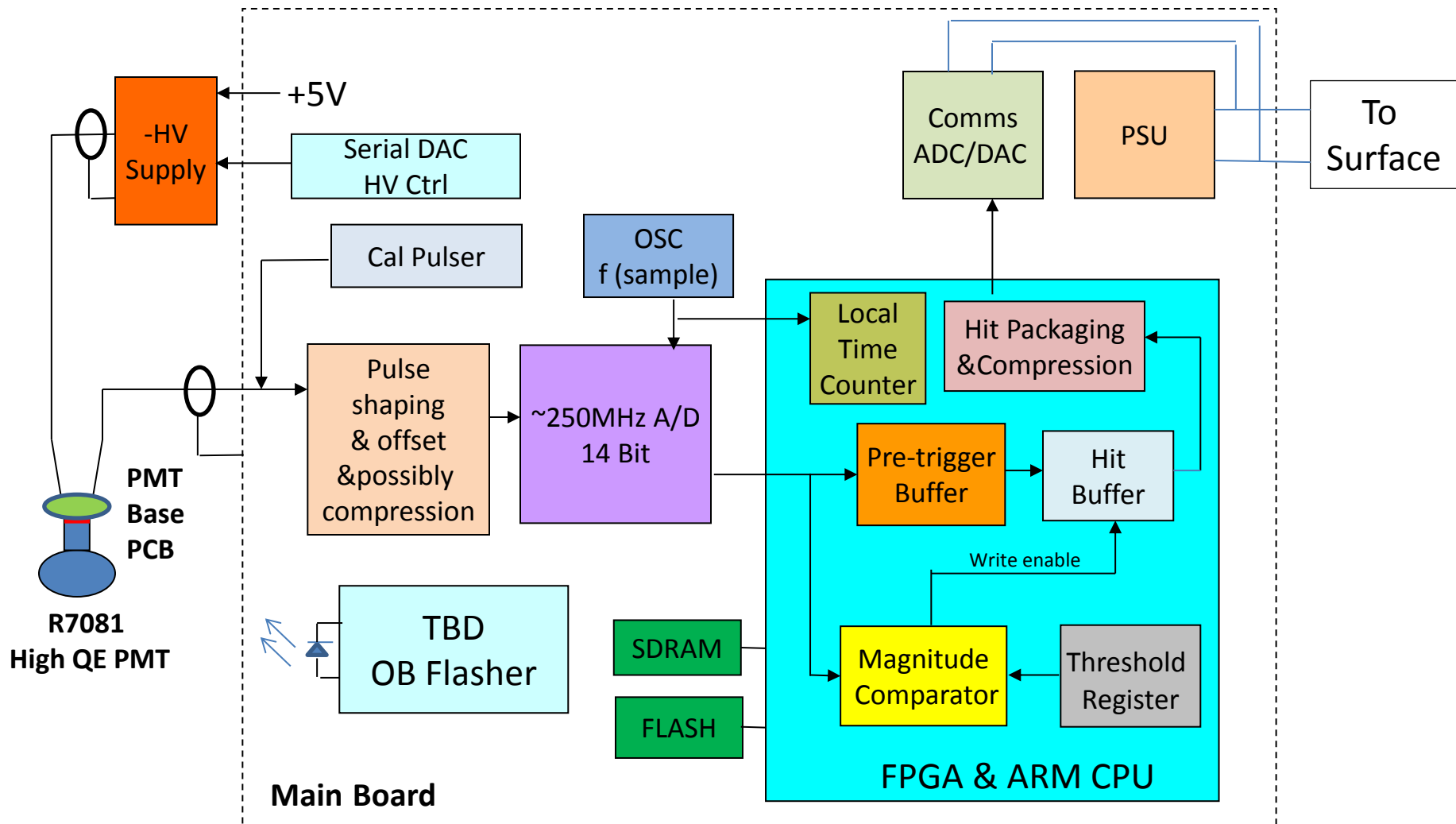- Built in Self-Test

IceCube DOM Block Diagram

IceCube DOM Block Diagram

Obsolete or unavailable in quantity

Next Generation DOM Block Diagram

Next-Generation Design Upgrades

Change:	IceCube	Upgrade	Rationale
PMT digitizer	triggered record	continuous	new technology allows high speed, low power ADC
Waveform format	fixed length	variable length	digital discriminator detects waveform duration
Local coincidence	hardwired	none	better hit compression; simpler cabling & electronics
DOMs per wire-pair	1 "U" + 1 "T" types	4 identical	easier PDOM manufacture; smaller cables
DOM spacing	17 meters	~5 meters	science requirement of lower ν energy threshold
DOM deployment	grips on cable	wire-rope links	shorter spacing allows easier, faster deployment

Next Generation DOM Design

Penetrator

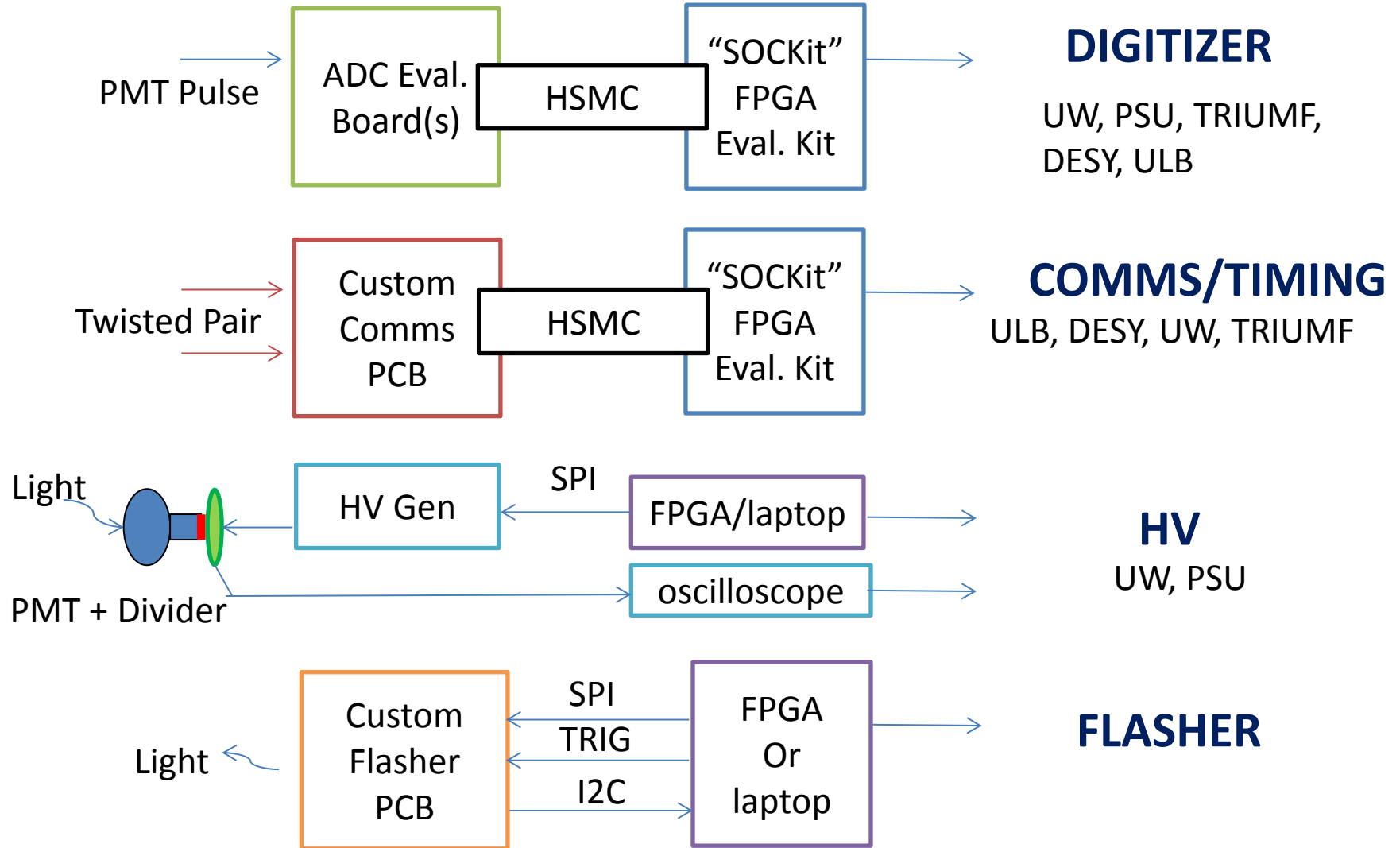PMT Base

HV Supply

LED Flasher

Main Board

Delay Board

Waist Band

Pressure Sphere

Mu-metal cage

Silicone Gel

PMT Photocathode
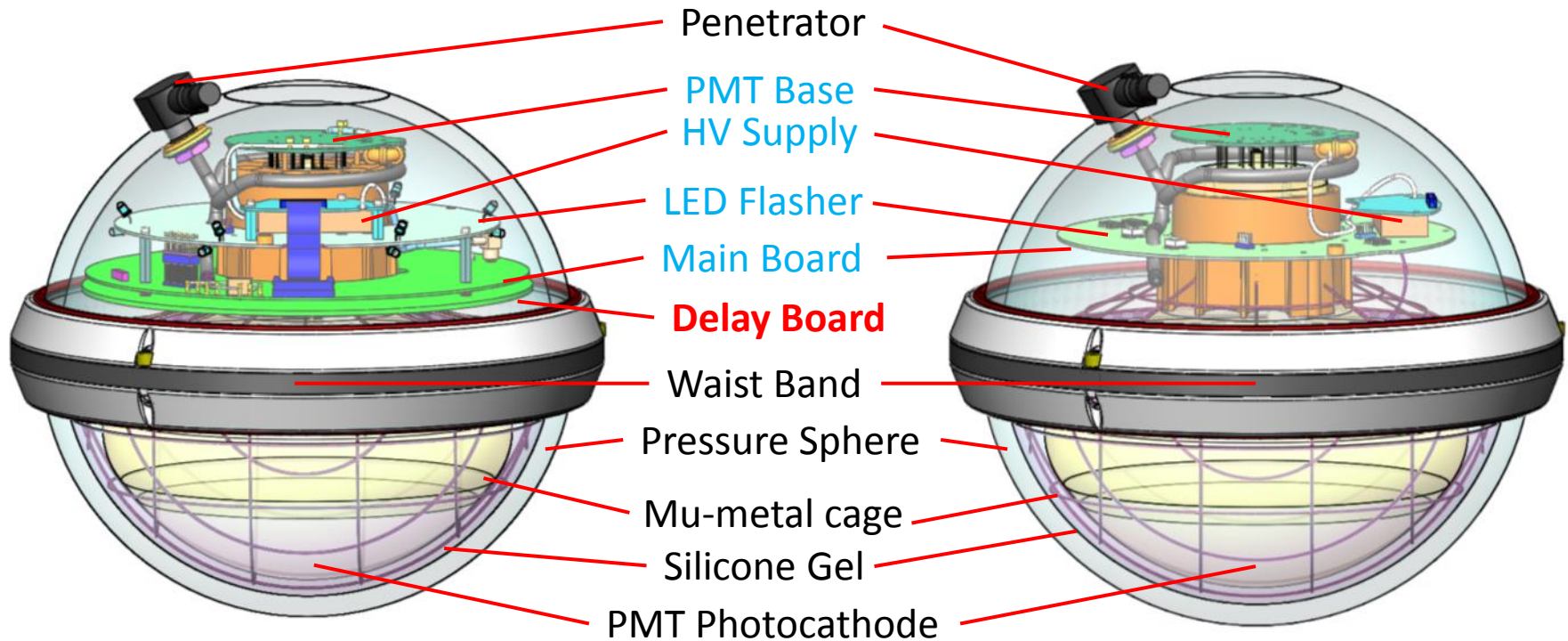
IceCube
DOM

Next Gen.
DOM

KEY:
Component identical
Component eliminated
Component re-designed

Main Prototyping Sections

PMT Pulse → **ADC Eval. Board(s)** — HSMC — **"SOCKit" FPGA Eval. Kit** →

DIGITIZER

UW, PSU, TRIUMF, DESY, ULB

Twisted Pair → **Custom Comms PCB** — HSMC — **"SOCKit" FPGA Eval. Kit** →

COMMS/TIMING
ULB, DESY, UW, TRIUMF

Light

PMT + Divider → **HV Gen** ← SPI ← **FPGA/laptop** →

oscilloscope →

HV
UW, PSU

Custom Flasher PCB ← SPI ← / TRIG ← / I2C → **FPGA Or laptop** →

Light ←

FLASHER

HSMC = High Speed Mezzanine Connector

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PMT Signal Path

8KHz-130MHz
Band-pass

~40MHz
Low Pass
Single Pole

~110MHz
Low Pass
5-7 Pole

HV
− +

K   A

**HV Isolation
Toroid**

**Pulse
Shaping**

**Anti-
Alias**

+

**14 bit ADC
250MSPS ADC**

R7081 PMT
& Divider

10

100

10

Possible
Passive
Compressor
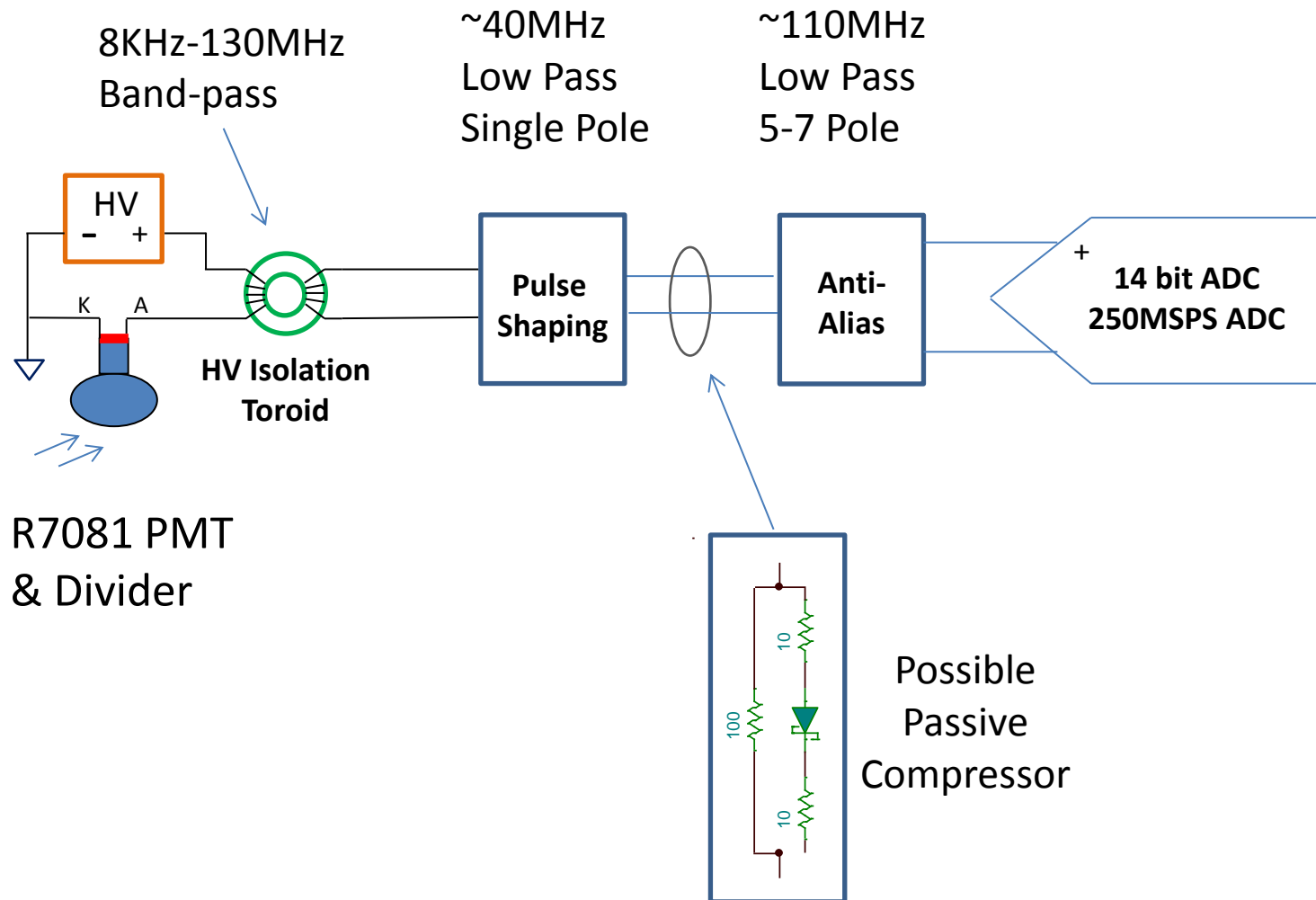
Digitizer Prototyping Sequence
(DDC=Digitizer Daughter Card)

PMT → **Commercial ADC Eval. Board** — **HSMC** — **FPGA Eval Kit** → USB

Q3/2013 - Q4/2013

Verify concept: Continuous Digitizer
Establish: Interface, FW, noise, Pdiss

PMT → **DDC 1 ADC Eval. Board** — **HSMC** — **FPGA Eval Kit** → USB

Q4/2013 - Q2/2014

Verify functionality: 300MHz ADC
Establish: Digital Interface, SOC FW,
Study noise, power, layout

PMT → **DDC 2 ADC Eval. Board** — **HSMC** — **FPGA Eval Kit** → USB

Q2/2014 - Q3/2014

Verify performance: Speed, Noise, etc.
Establish: AFE and PSU circuitry, layout

PMT → **REV0** → USB, Comms

Q2/2015 - Q3/2015

Verify performance: Speed, Noise, etc.
Establish: Specific components, layout

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Digitizer Readout Firmware
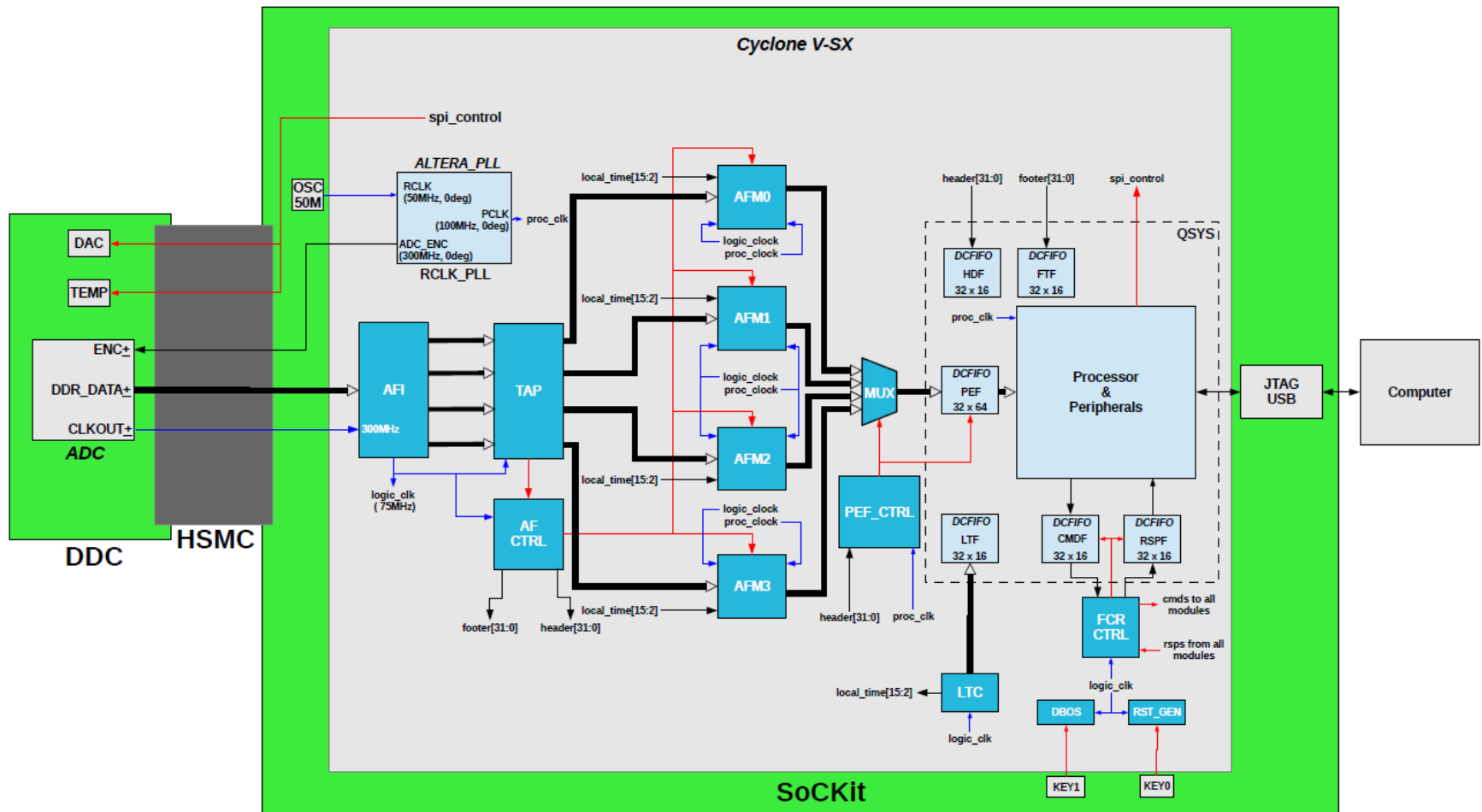
Study: ADC noise, feature extraction, power dissipation, processing requirements

T. Anderson, J. Groh (PSU)

DDC 1 Bench Testing
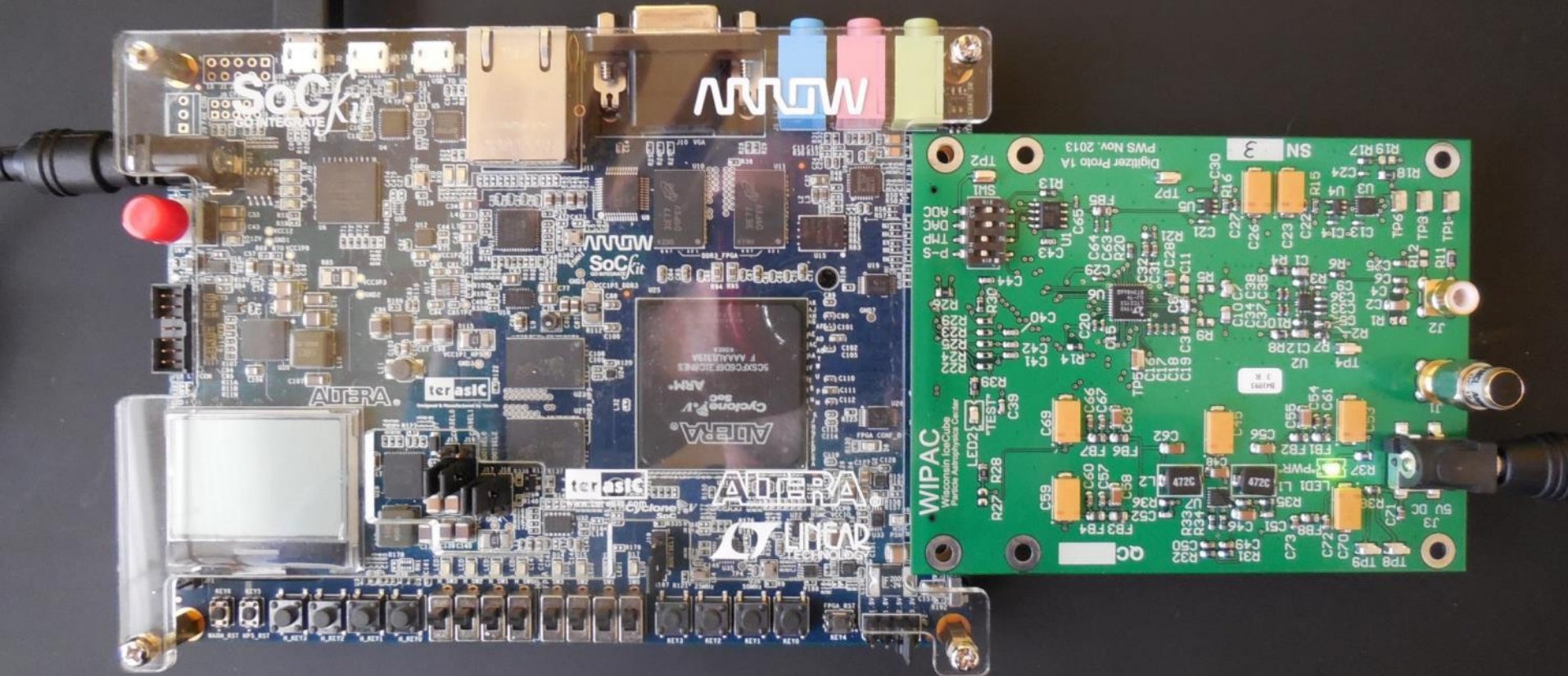
FPGA Evaluation "SOCKit"

Digitizer Daughter Card "DDC-1"

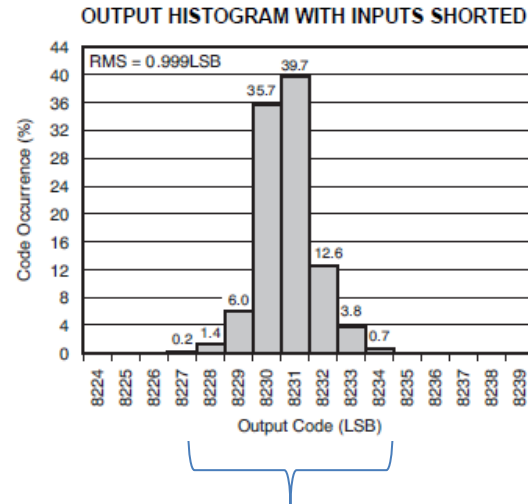# Noise Comparison Between Candidate ADCs

**LTC2153-14
(300 MSPS)**

**ADS4149
(250MSPS)**

LTC2153-14: Shorted Input Histogram

OUTPUT HISTOGRAM WITH INPUTS SHORTED
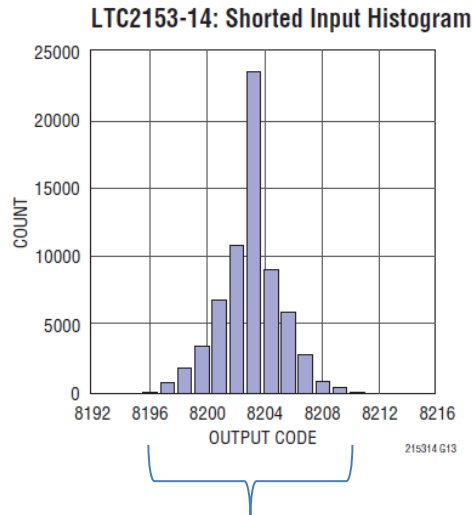
"Noise band":   13 LSB   8 LSB   Ratio = 1.625

"Transition Noise":   2.11 LSB RMS   .999 LSB RMS   Ratio = 2.1

SNR@70MHz in: 68.4 dBFS (310MSPS)   71.4 dBFS (250MSPS)

ENOB: 11.07 LSB   11.3 LSB
              (70MHz input @310MSPS)   (70MHz input @250MSPS)

DDC2 Front End

INPUT

Single-Differential and Pulse Shaping

COMPRESSOR
(Optional)

ADC Input and
DC Bias

Anti-Alias
5-Pole, 100MHz
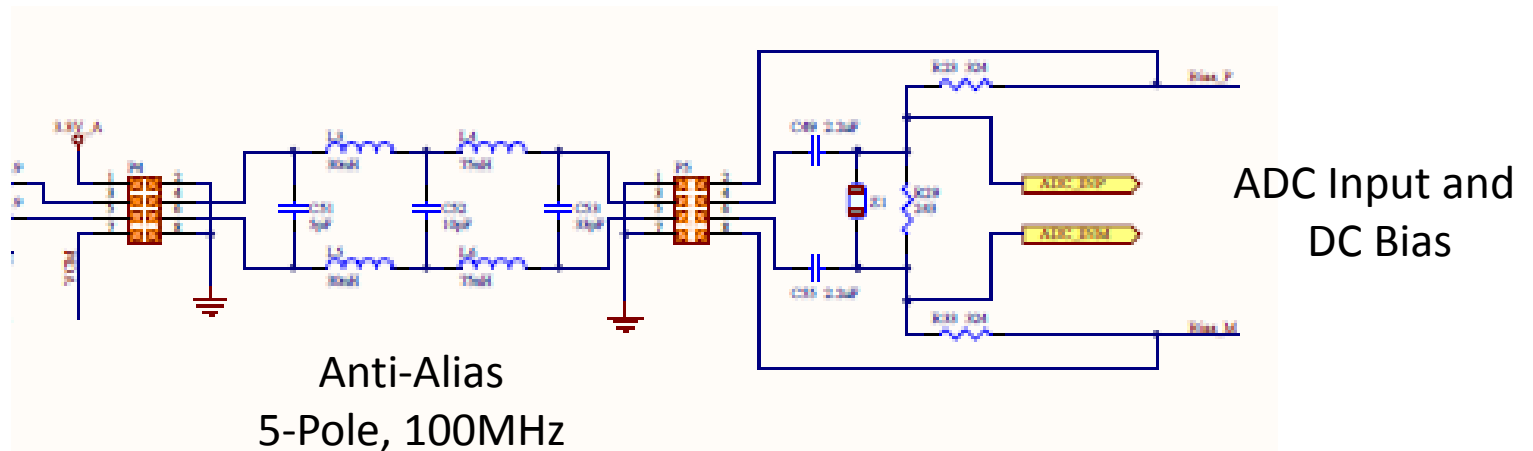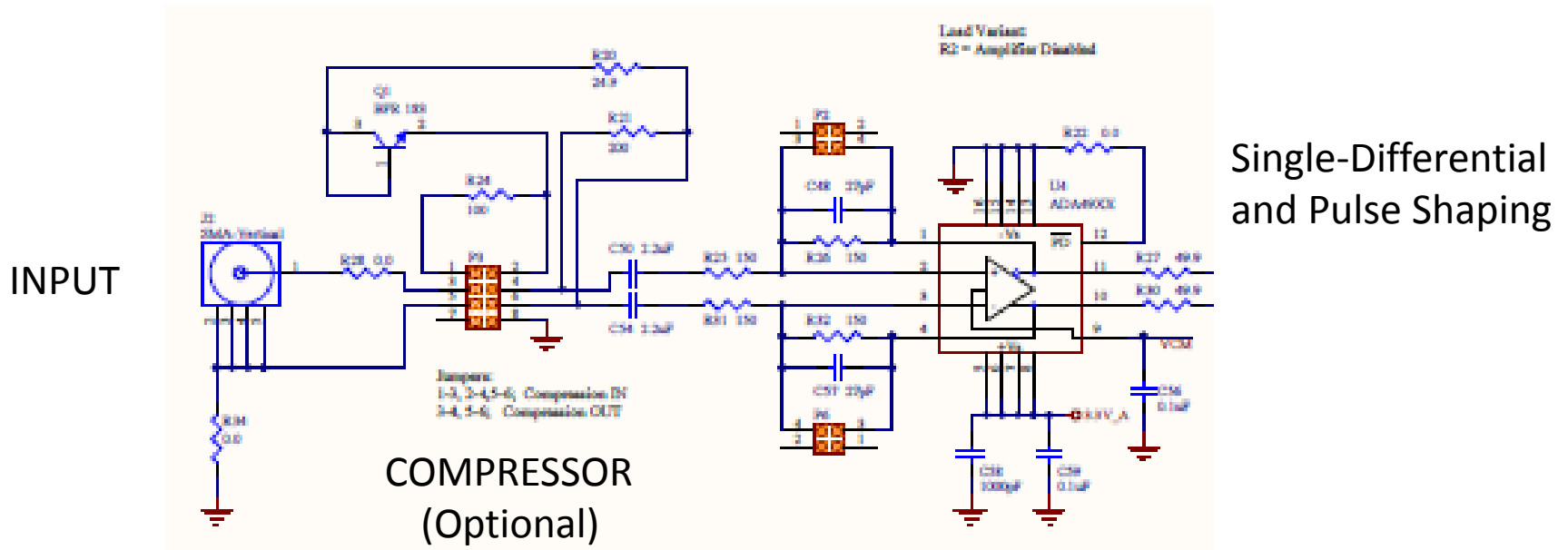
Thank You!

SUPPLEMENTAL SLIDES

PINGU String Architecture

Cable Grip

Adjustable Link Chain

MainCable

To "T" DOM

Cable Breakout

"U" DOM

Cable Grip

Lifting Ring
1.5m Harness

1.75 m Link

Lifting Ring

1.75 m Link

Lifting Ring
1.5m Harness

5m PDOM Spacing Shown

Wire Rope Link

Main Cable

Lifting Ring

Breakout Cable Assembly (BCA)

PDOM Harness

PDOM Connector (0-3)

To Quad Breakout
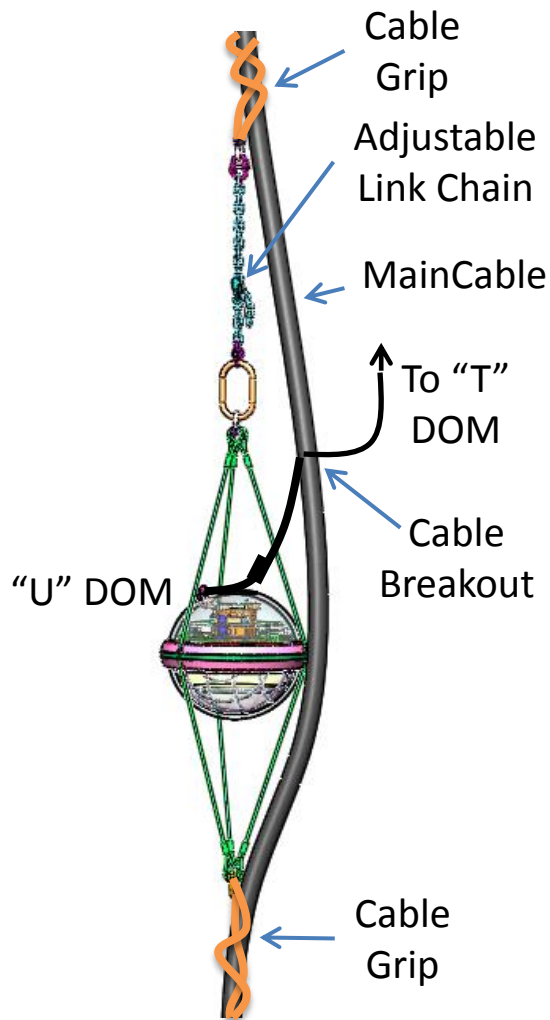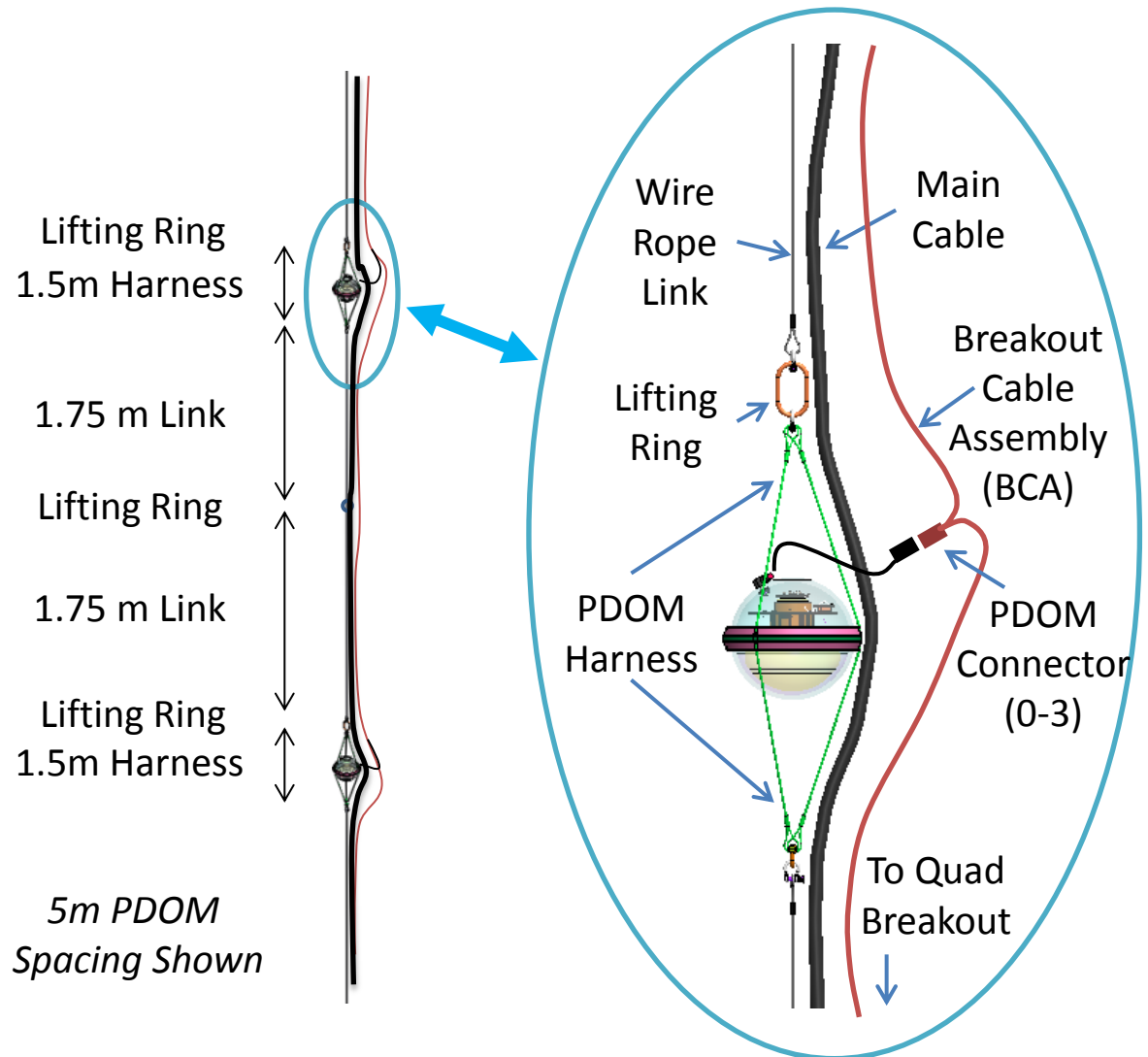
IceCube Detail   **PINGU String**   **PINGU Detail**

General System Requirements

| Requirement	IceCube	PINGU	HEX
Timing	<3ns	Same as IC	Same as IC
LSB	~0.13mv	~0.08mv	~0.08mv
Range (bits)	16	14 compressed?	14 compressed?
Calibration Circuitry	IC flasher	Better Flasher	~Brighter Flasher
Production Calibration	Minimal	Maybe Every Unit	Maybe Sampled
Hole Ice quality	Bubbles	Clearer than IC	Clearer than IC
Sensors-String/quad	60/4	60/8	80/8
PMT	Standard	Hi QE	Hi QE? (double$)
Wired Coincidence	Yes	No	No
Hole Spacing	125m	~30m	~300m
Vertical Spacing	17m	5m	17m
Hub	ICL	ICL	Top of hole
Drill Design	SES-based	Transitional	Modular

DDC1; LTC2153-14 w/ input shorted
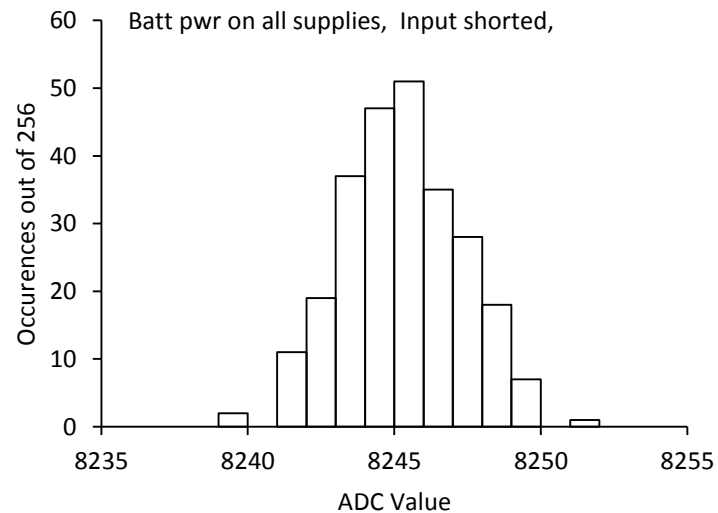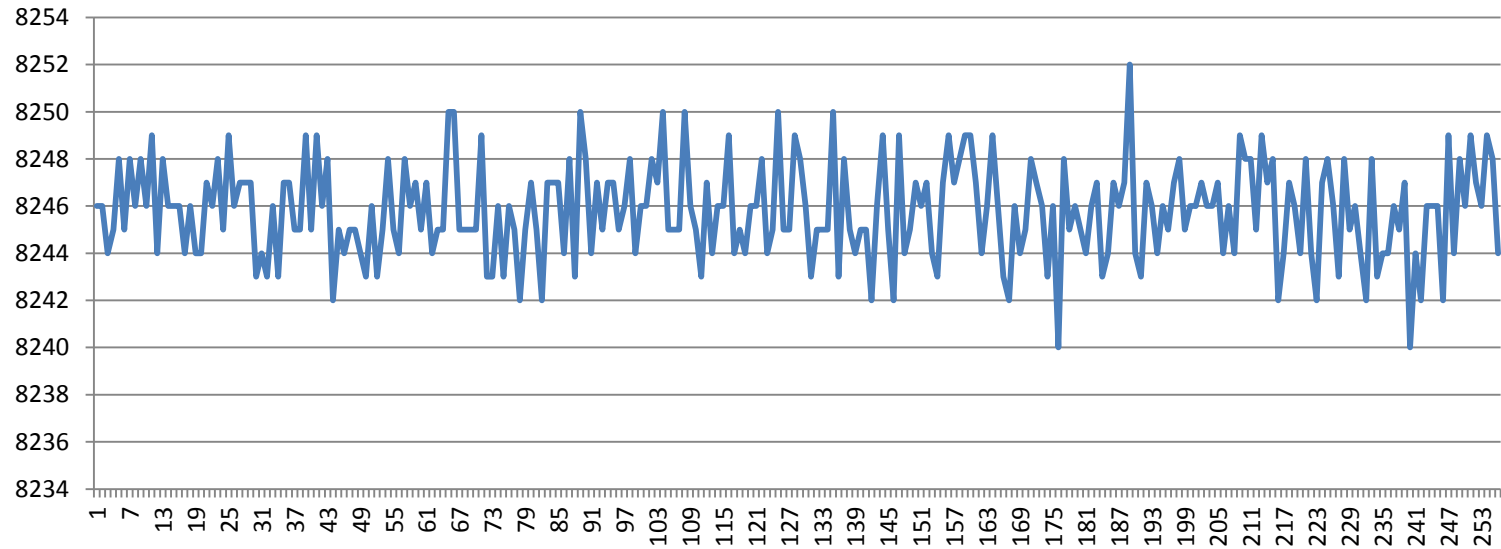
Electronic Subsystems

1) Digitizer
2) Front End (offset & shaping)
3) Communications/Rapcal
4) Oscillator
5) Logic & Processor
6) LV Supply
7) HV Supply (maybe on MB)
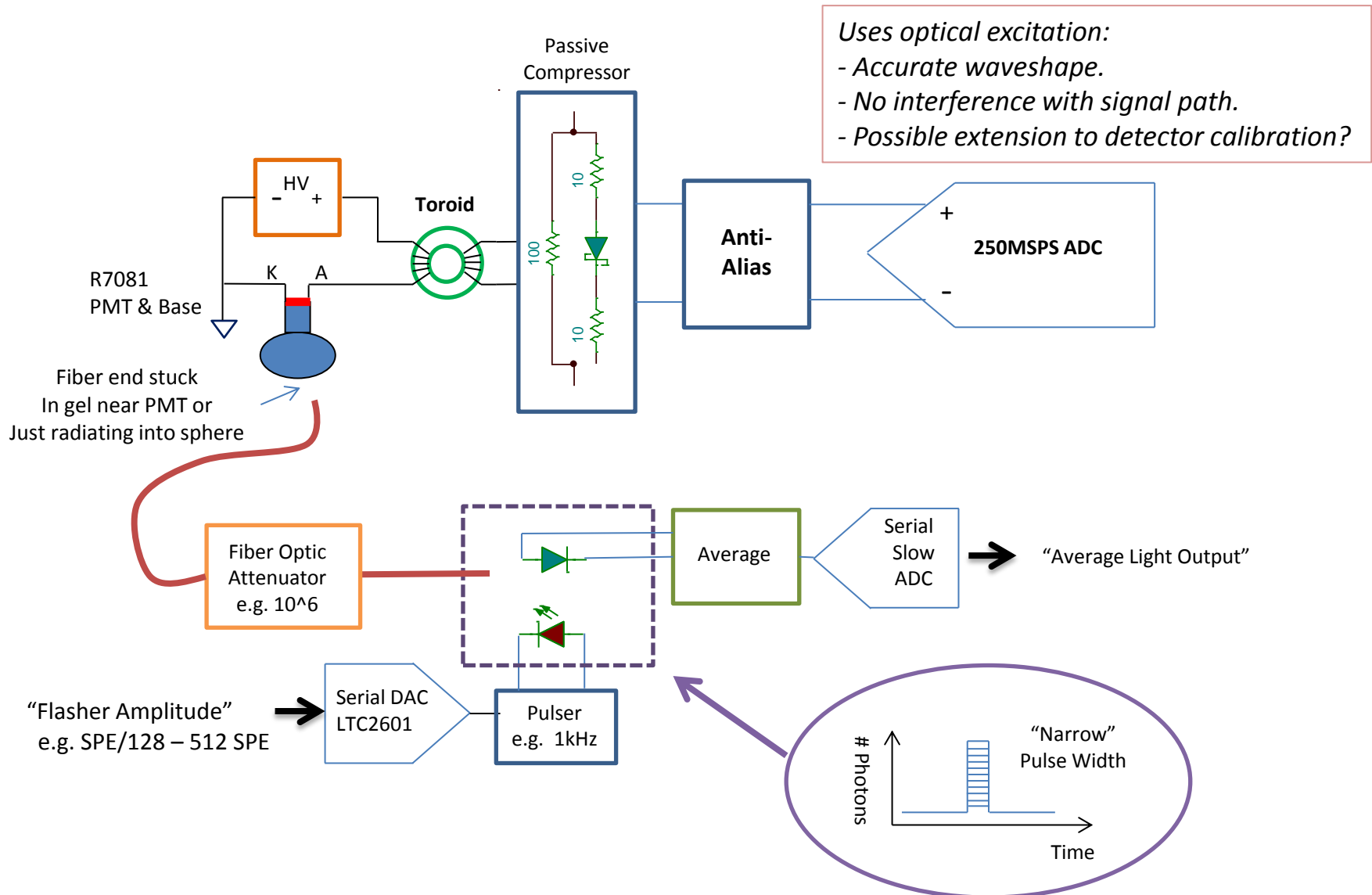8) PMT Divider
9) Flasher
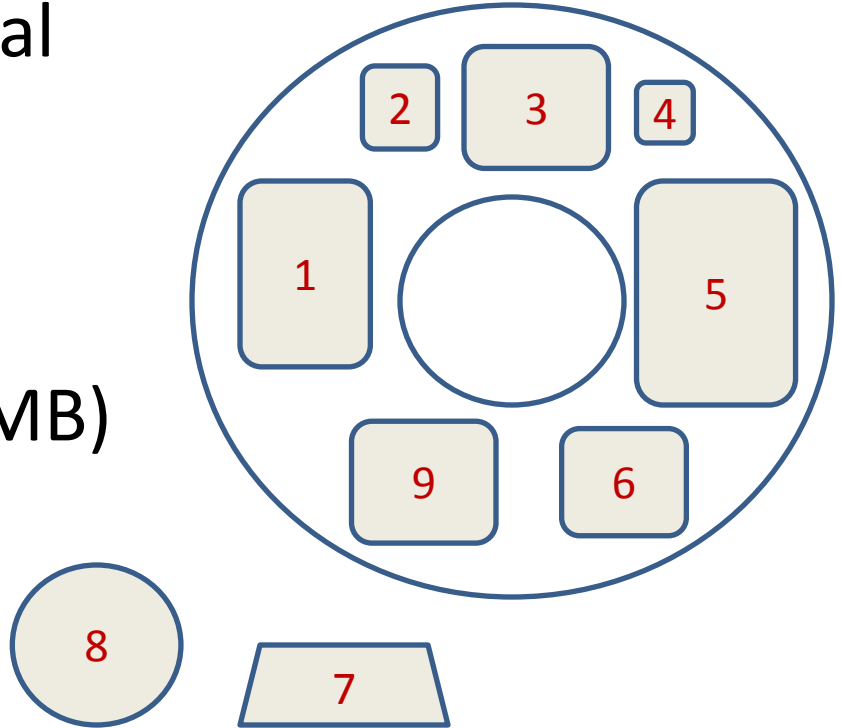
Digitizer Firmware Simplified Block Diagram
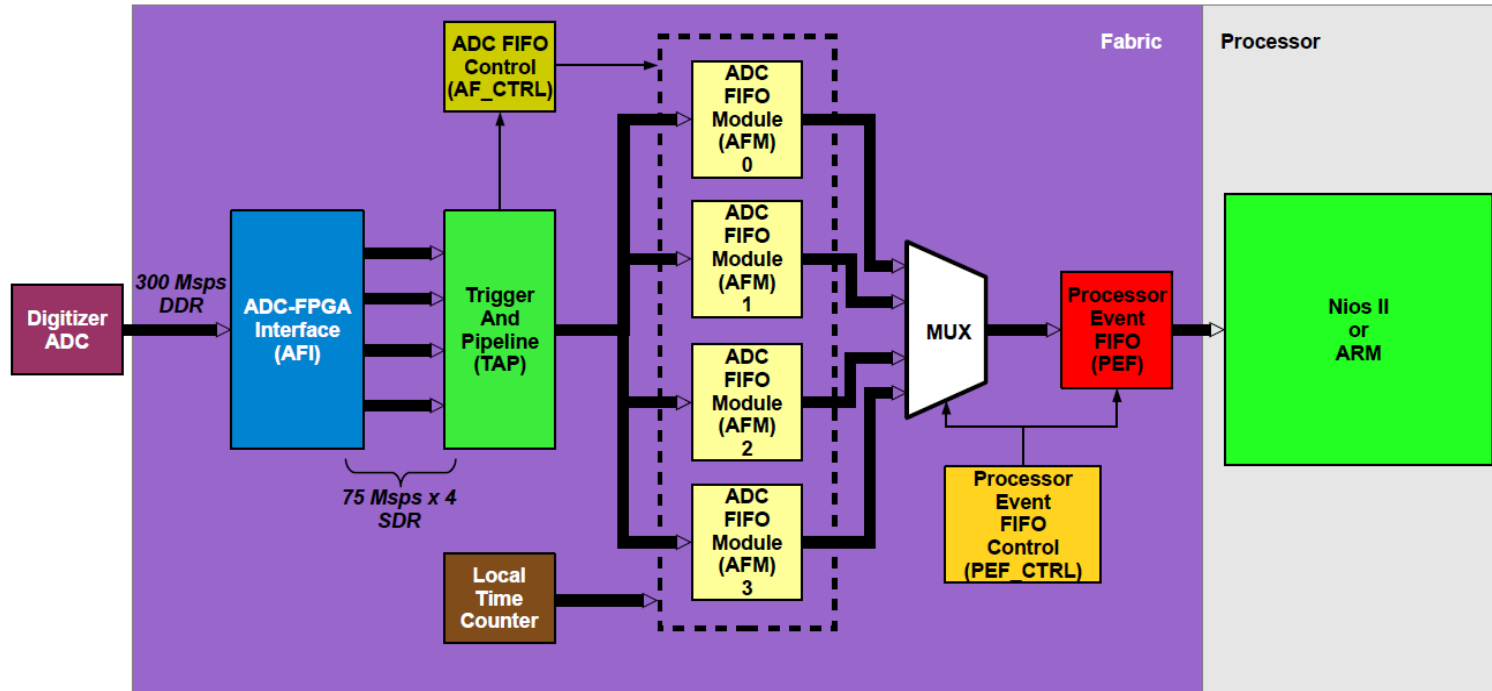
- AFI converts 300 Msps DDR from ADC sampler to 75 Msps x 4 SDR.
- TAP generates trigger flags and pipelines data.
- AF_CTRL controls writing to AFM's internal pretrigger and waveform FIFOs.
- PEF_CTRL orders data in PEF.
- Final waveform contains adjustable amount of pre-trigger and post-trigger data.

T. Anderson and J. Groh (PSU)

Strawman Compression Calibration

Passive Compressor

Uses optical excitation:
- *Accurate waveshape.*
- *No interference with signal path.*
- *Possible extension to detector calibration?*

HV
−   +

Toroid

100   10   10

Anti-Alias

250MSPS ADC
+
−

R7081
PMT & Base

K   A

Fiber end stuck
In gel near PMT or
Just radiating into sphere

Fiber Optic
Attenuator
e.g. 10^6

Average

Serial
Slow
ADC

"Average Light Output"

"Flasher Amplitude"
e.g. SPE/128 – 512 SPE

Serial DAC
LTC2601

Pulser
e.g. 1kHz

"Narrow"
Pulse Width

\# Photons

Time

Seven Year Seasonal Construction

Strings Deployed:

Season	Strings	Total
2004-05	1	1
2005-06	8	9
2006-07	13	22
2007-08	18	40
2008-09	19	59
2009-10	20	79
2010-11	7	86

Ski-way

IceCube Lab Building

South Pole Station

IceCube Outline
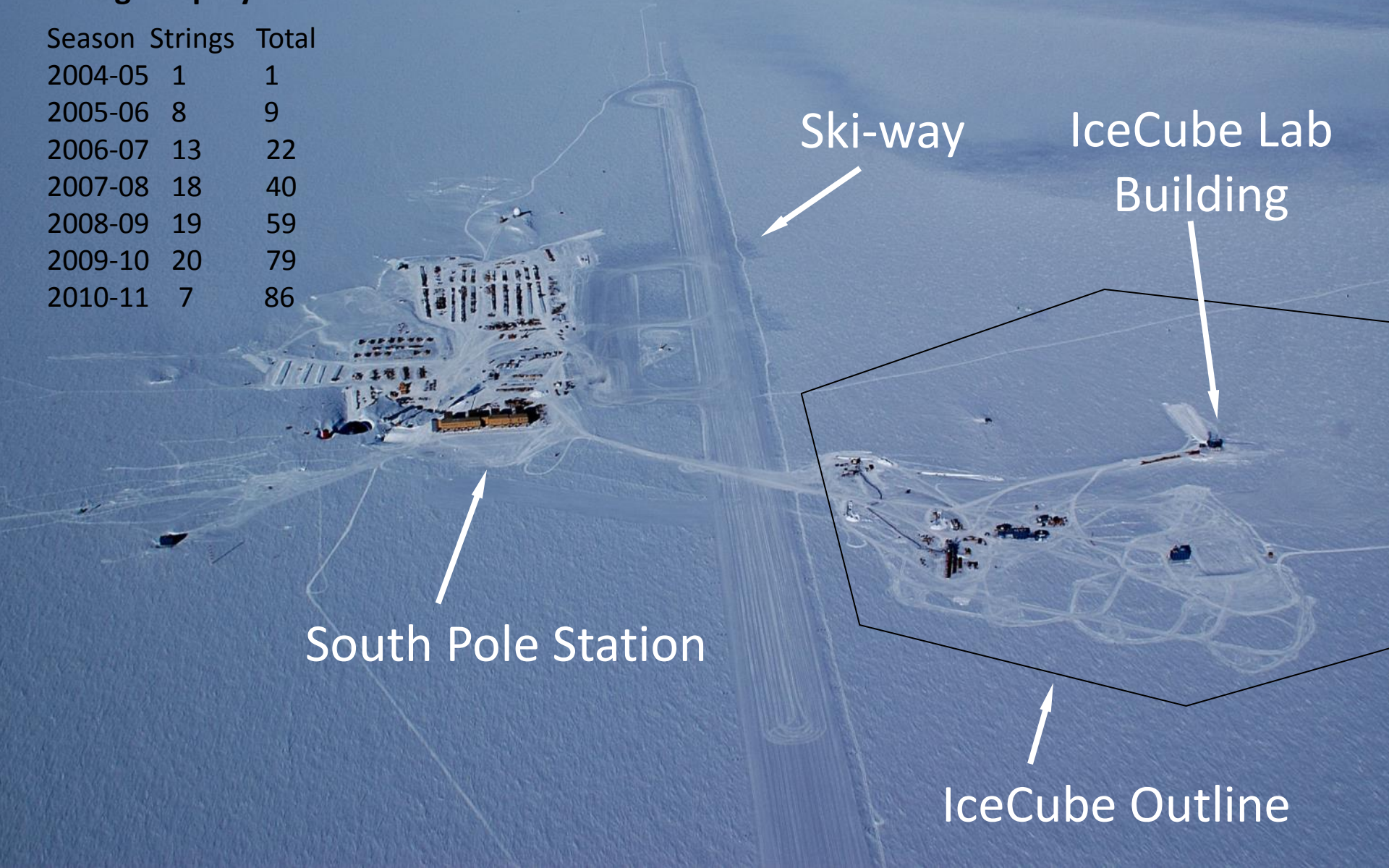
Drilling and Deployment Leap-Frog
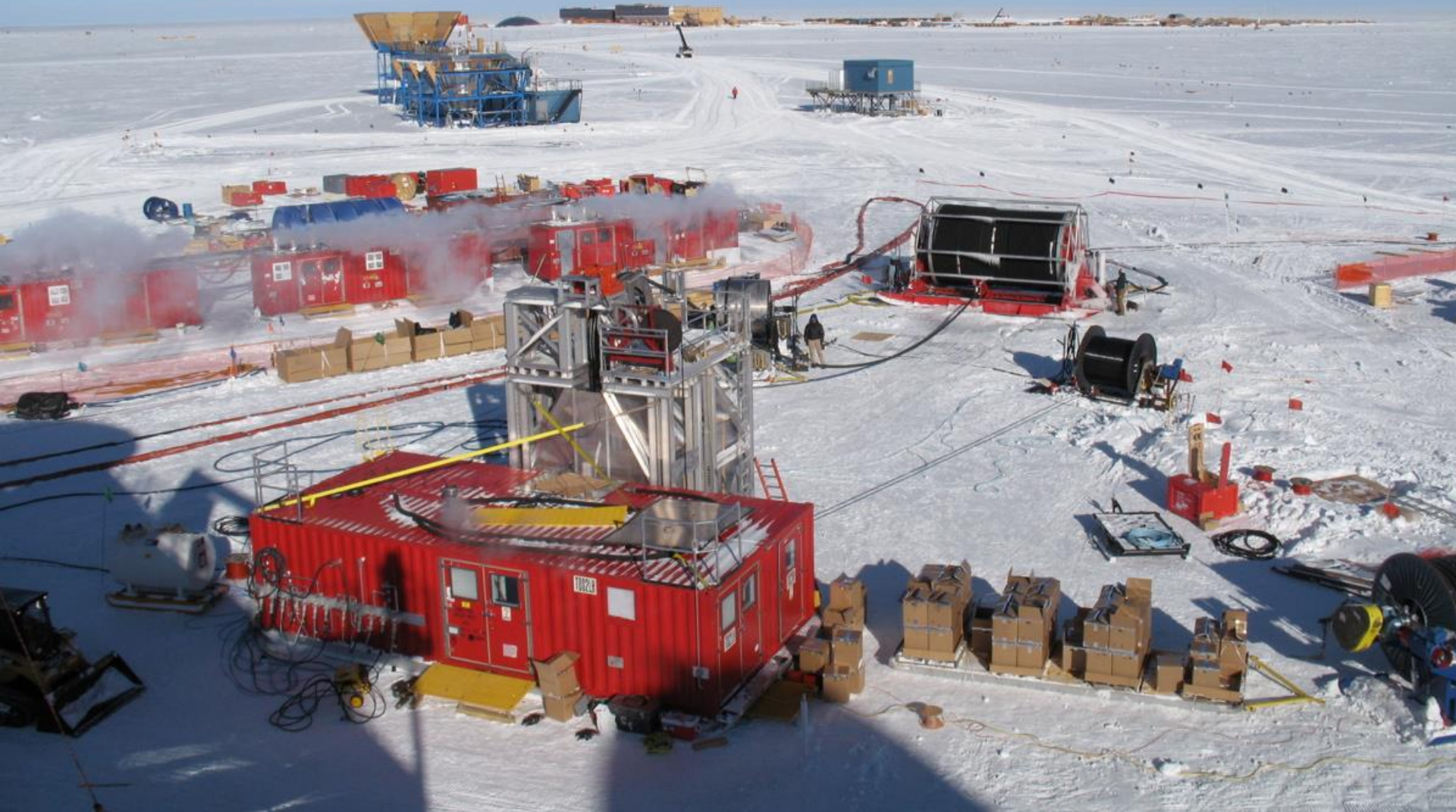
IceCube Digital Optical Modules (DOMS)

Surface Cables into ICL