DAQ plan

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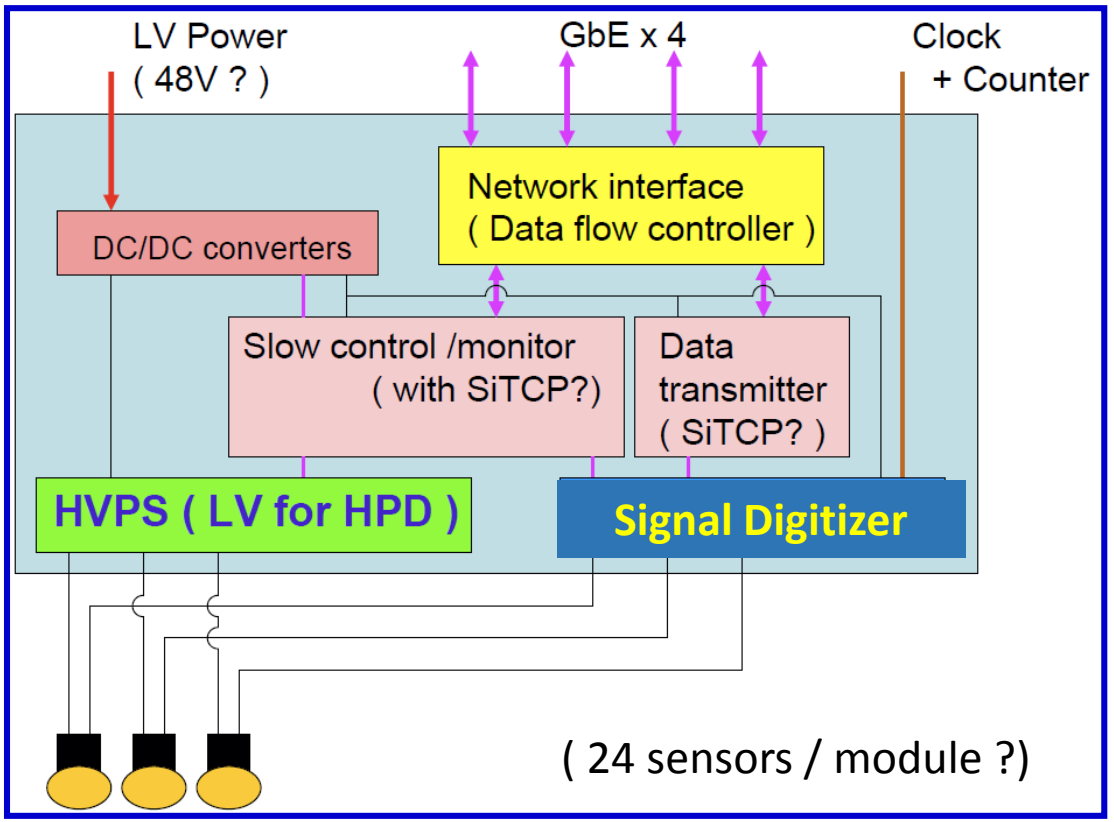
DAQ baseline design

Hardware trigger less DAQ system ~ record all the hits ~

Digitize all the photo sensor signals above threshold
(~ ¼ photo electrons) and read out by a computer.

Key components

- Self triggering
  & dead-time free
  signal digitizers
- HV (LV)
  for photo-sensors
- Intelligent
  network interfaces
- Front-end module
  in the water



DAQ baseline design

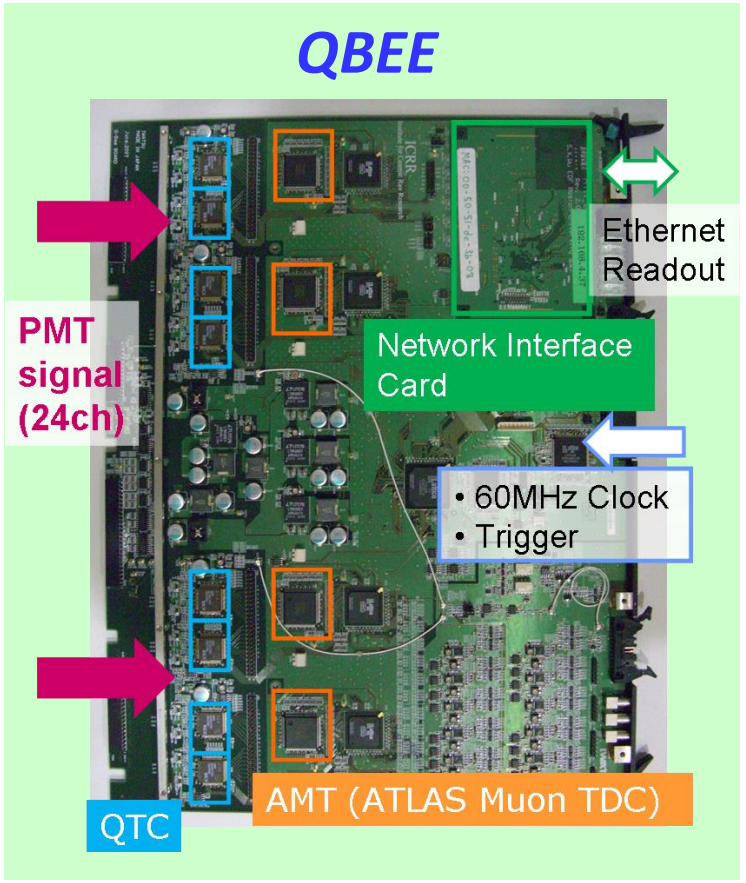
Hardware trigger less DAQ system ~ record all the hits ~

Digitize all the photo sensor signals above threshold
(~ ¼ photo electrons) and read out by a computer.

Possible configurations
of the signal digitization

- QTC (ADC) + TDC
  Similar to QBEE for SK4
- FADC
  Proposed by the Canadian group

In Japan, we started R&D
to develop a test module
with QTC & FPGA based TDC.



Recent updates of the DAQ R&D

R&D of the new front end module

1) Use spare QTC chips for SK

(We don't have many but sufficient for the tests.)

2) Use new FPGA based TDC developed in FNAL by Jinyuan-san.

AMT3 chip (used in QBEE) has been discontinued.
The first buffer of AMT3 was not sufficient
and ringing of the PMT signal may fill up the buffer.
Data bus throughput is not sufficient
to read out all the hits at maximum rate.
This TDC is now under development
for muon experiment in FNAL.

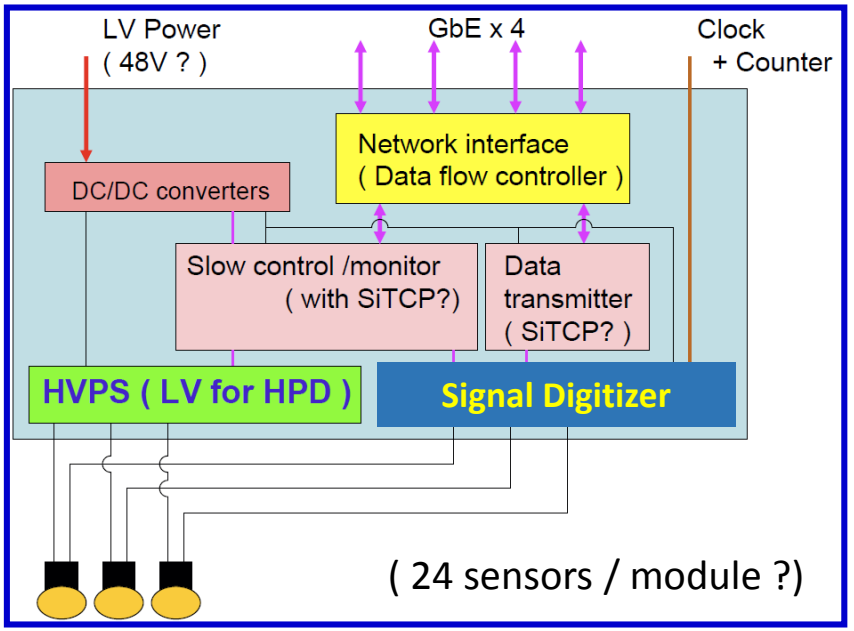
From this summer, evaluation of this TDC will be started.
Once this TDC is confirmed to be feasible,
we will start working on the analog part.

We need to develop new QTC for the real detector.

(We are planning to contact "Iwatsu", for possible collaboration.)

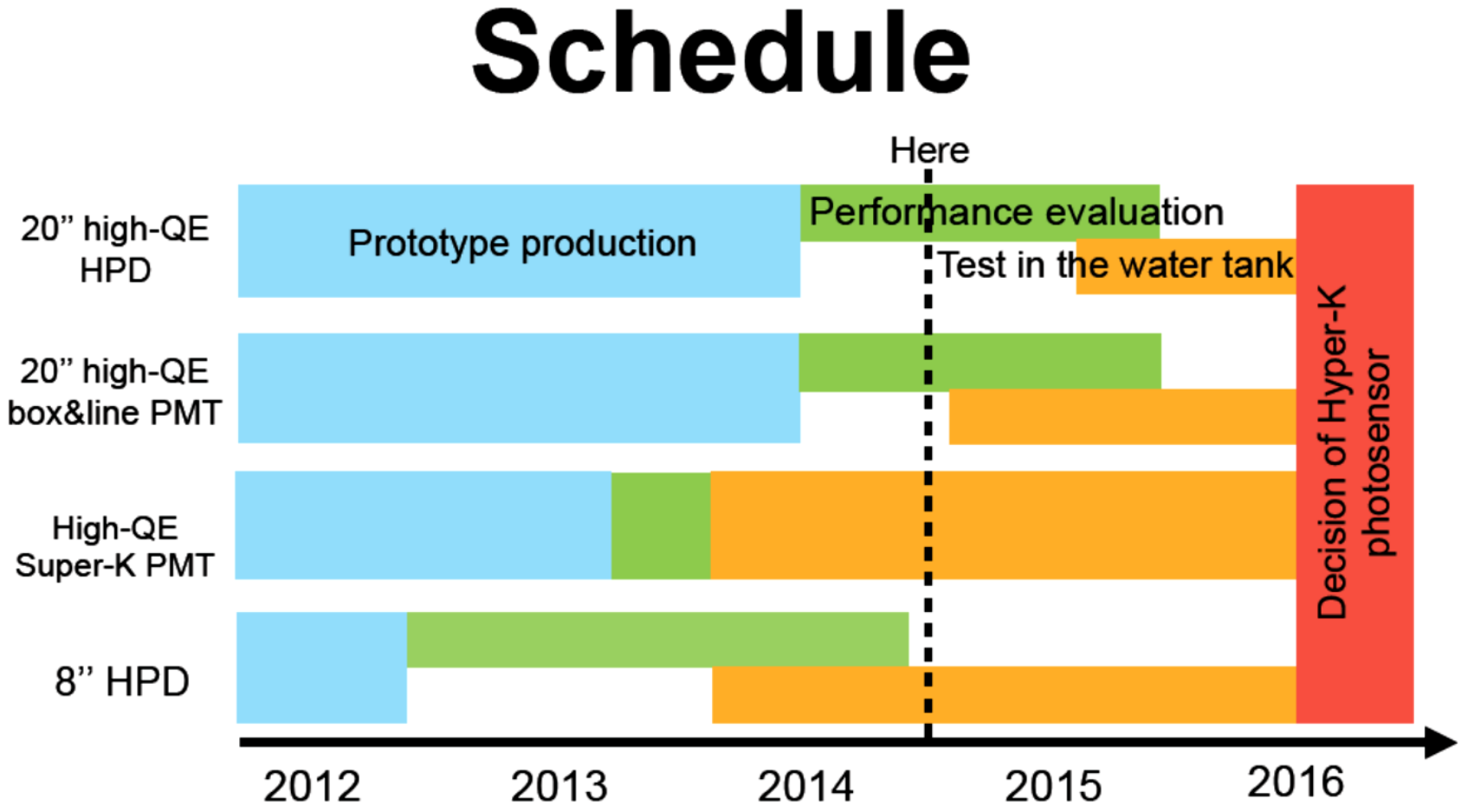
What we are going to do with the test detector

- ***Proof of the concept and performance evaluations***
  - Clocking scheme
    - timing synchronization
      - stability and jitter
  - Signal digitization
    - Methods : FADC , QTC+TDC
    - Noise level
    - Charge & timing resolution
    - Dynamic range and linearity
  - Data transfer system
  - Slow monitor
  - Water proof
    - chassis, connectors and cables



- ***Stability & durability***
- ***Feasibility***

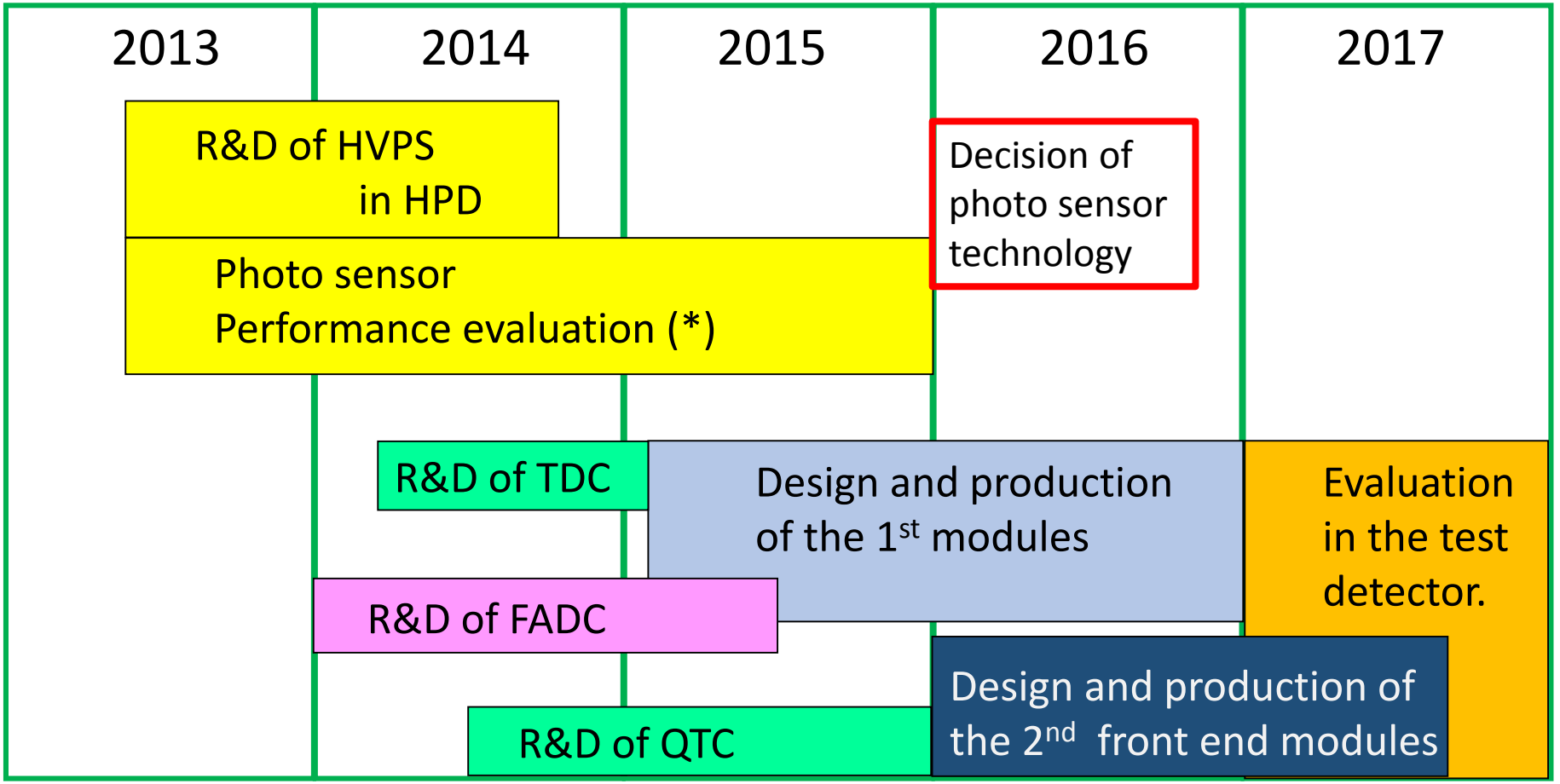
Current plan of the photo sensor R&D



- Development of 20" HPD is still ongoing
  - Preamplifier for large AD size, Low capacitance AD
- In this summer, 20" high-QE box&line PMT will be installed in the tank

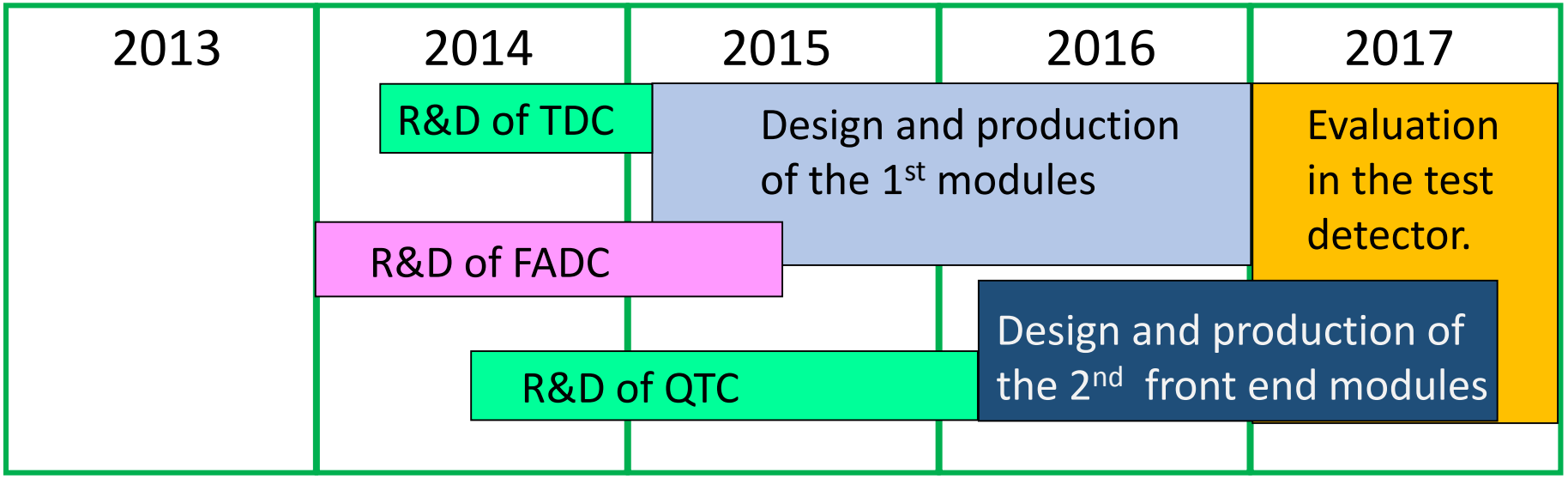
Taken from the presentation at TIPP 2014 by Suda-san.

Rough timeline of the DAQ system R&D



*) We have started tests of the new photo sensors
in the EGADS detector in collaboration of the EGADS group.

Rough timeline of the DAQ system R&D



1) 1st prototype may not contain power supply for the photo sensor
   Check the basic functionalities, performance and feasibility, together with the new sensors.

2) 2nd prototype hopefully has all the functionalities including power supply for the photo sensors
   Check the performance of the signal digitization and the other peripheral functionalities.

Items to be designed in the R&D

Front end board core components

TDC	FPGA-based
QTC	Successor of QTC for QBEE?
FADC	
LV for HPD (?)	Finalize when the sensor is choosen
HV for PMT (?)	Finalize when the sensor is choosen
Clock receiver / transmitter	Low skew (<< 100 ps)
System control	
Network I/F	Successor of SiTCP
	Rapid I/O

Items to be designed in the R&D

Clock module ~ synchronization

Clock module	Accurate 10 ~ 100 MHz clock generator
Clock distributor	Low skew (<< 100 ps)
Clodk distribution cable	Combined with network cable (?)

Data transfer line (from the FEBs to the readout computers)

Data Concentrator	Prefer to connect usual PC directly.

Items to be designed in the R&D

Water tight front-end board chassis and related

Signal connector	from photo sensor to FEB
3kV HV connector	for PMT
10kV HV cable	If HV is located in the FEB box
10kV HV connector	If HV is located in the FEB box
Network cable	
Network connector	
Power supply connector	
Chasis	

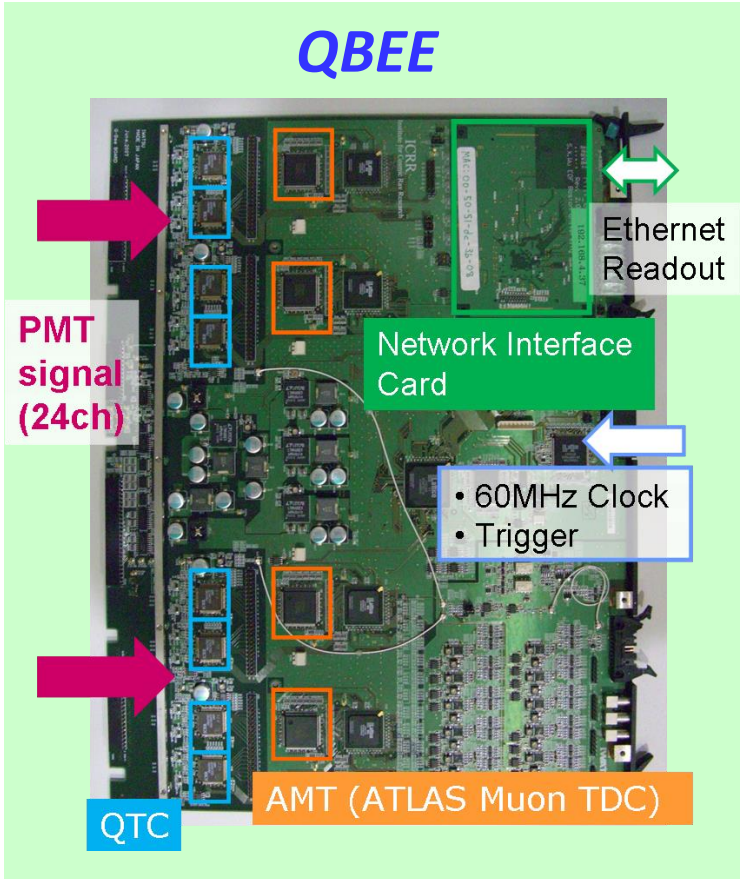
6. Recent updates of the DAQ R&D

Basic requirements of the front-end module

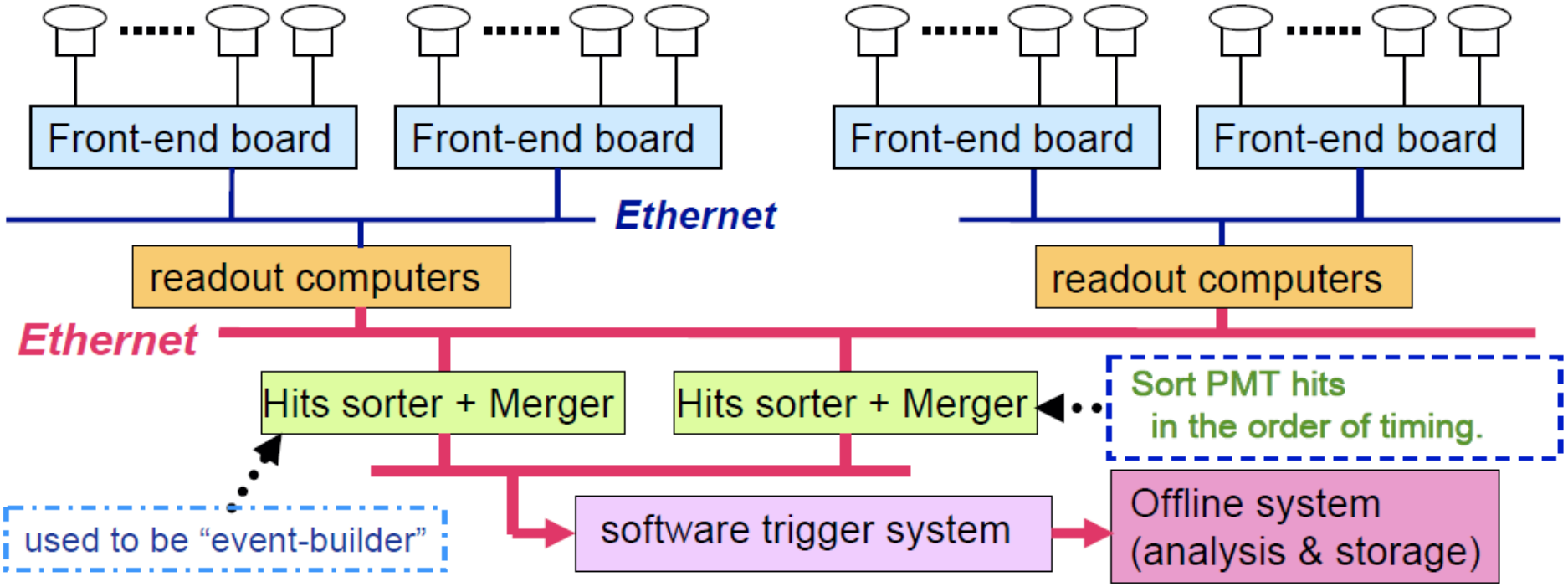
- **Built-in Discriminator**
  ¼ p.e. (~ 0.3 mV)
- **Charge integration gate**
  ~ 400 ns
- **Processing Speed**
  ~1 usec / hit
- **High Sensitivity for single p.e.**
- **Charge Response**
  Resolution: ~ 0.05p.e. (<25p.e.)
- **Wide Charge Dynamic Range** (*)
  0.1 ~ 1250p.e. (0.2~2500pC)
- **Timing Response**
  0.3ns (1p.e.⇔ -3mV) (RMS)
  0.2ns (>5p.e.)

(*) QTC has 3 charge ranges
to cover wide dynamic range
(1 : 7 : 49)

- **TDC lowest bit**
  0.52 ns
- **Low power consumption**
  ~< 1W / channel

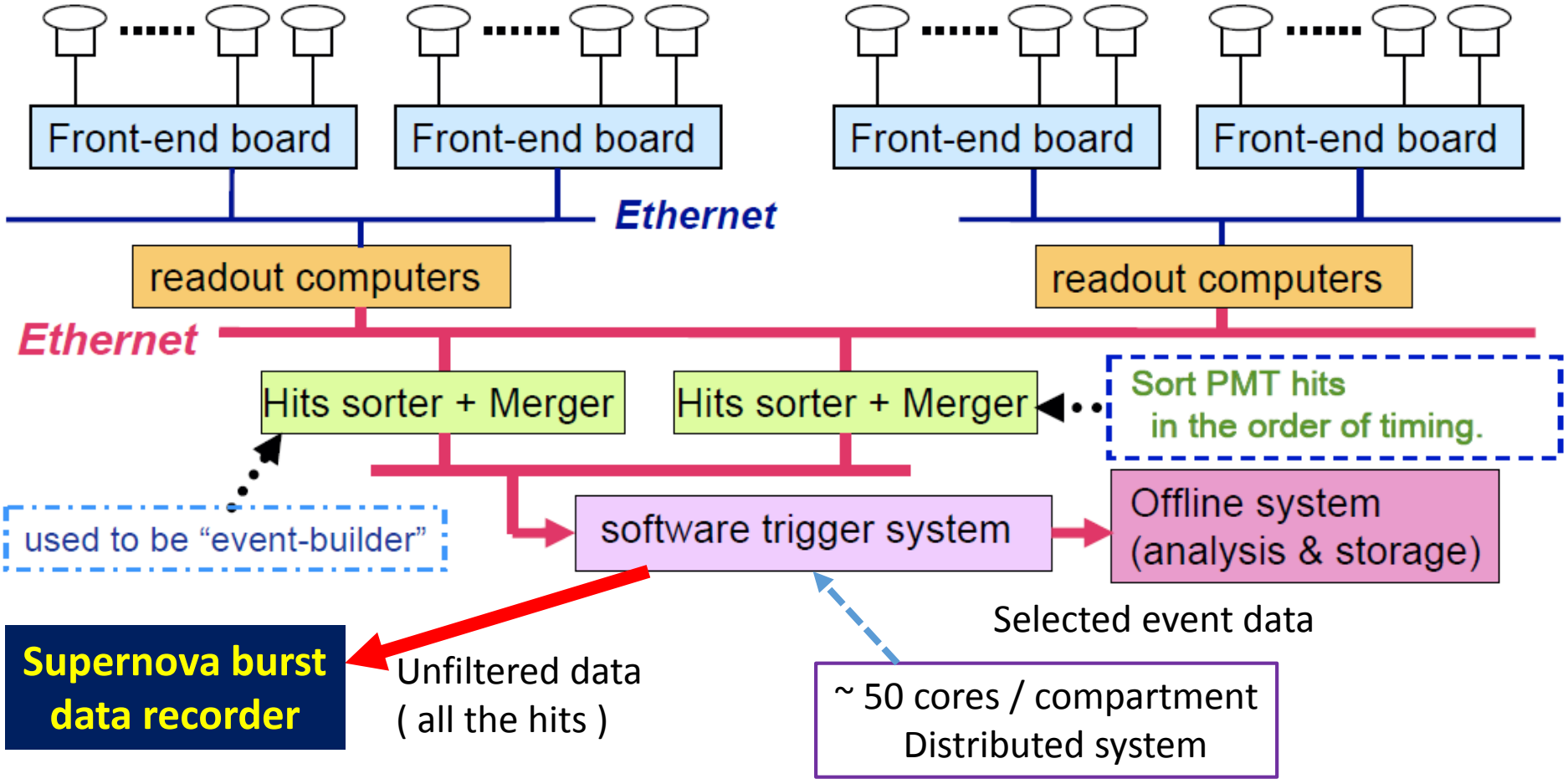


6. Recent updates of the DAQ R&D



1) Digitize all the signal (timing and charge) above ~ 1/4 p.e.
2) Read out timing and charge with the computers.
3) Define events with software and store the event data.
   Sort the hits in the order of timing and
   a) search for the timing cluster, and
   b) apply reconstruction program for low E_ν
   (recent work / improvements in SK)

6. Recent updates of the DAQ R&D



Record all the hit data before and after the supernova for ~ 60 sec.

Transfer all the data to single computer and keep them in the main memory for ~ 60 seconds.
Once supernova burst candidate is identified, dump the data to the disk.

This also implemented in SK and now under the test.