DAQ (i.e electronics) R&D status in Canada

F.Retiere, T.Lindner, C. Rethmeier (undergrad. Student), P-A. Amaudruz, D. Bishop and 4 UBC eng. students

TRIUMF

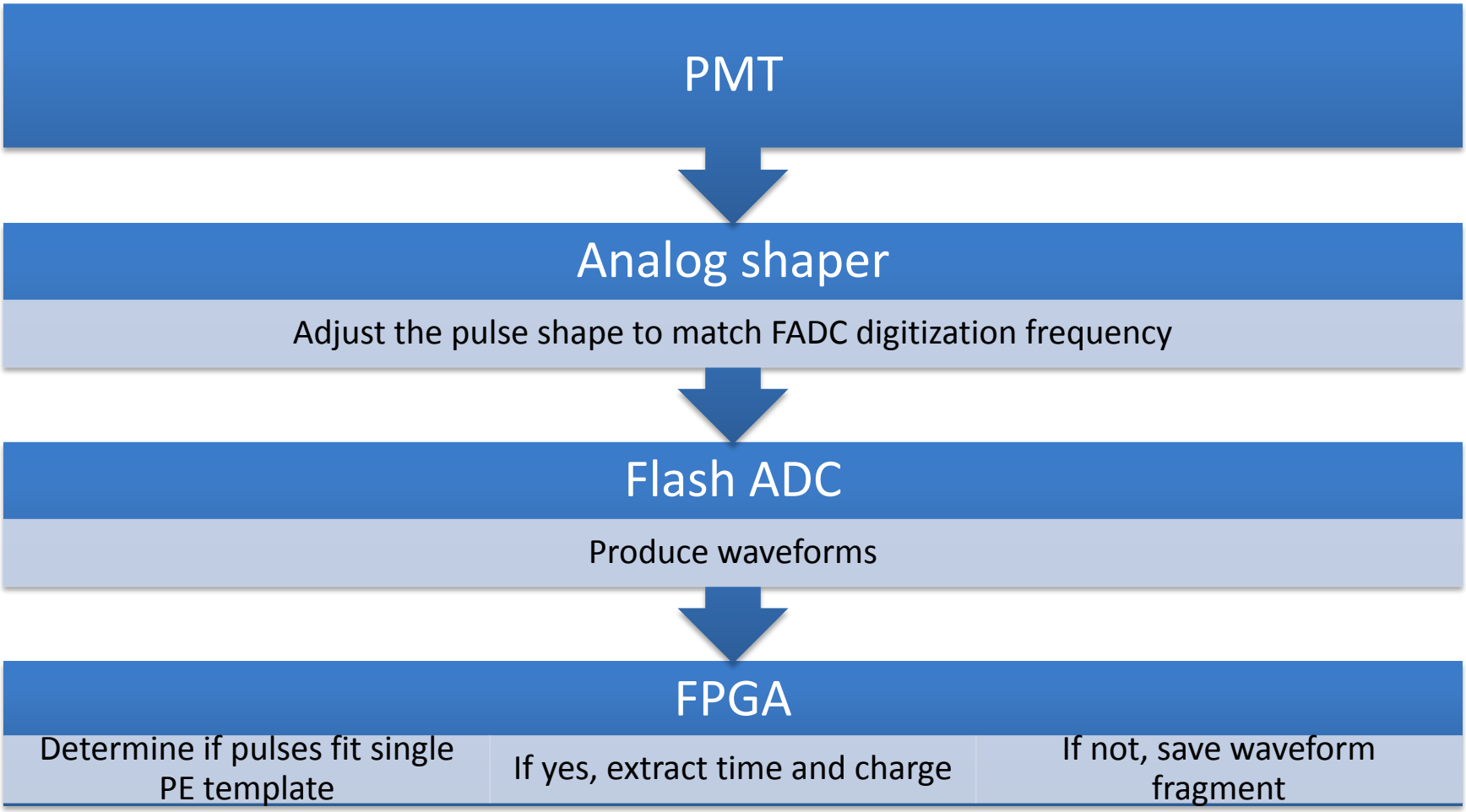
Outline

- Explore flash ADC solution
  - Requirement
  - Strategy
  - Test setup
  - Test results
- Front end electronics communication protocol
  - Investigate using rapidIO protocol

Electronics requirement recap

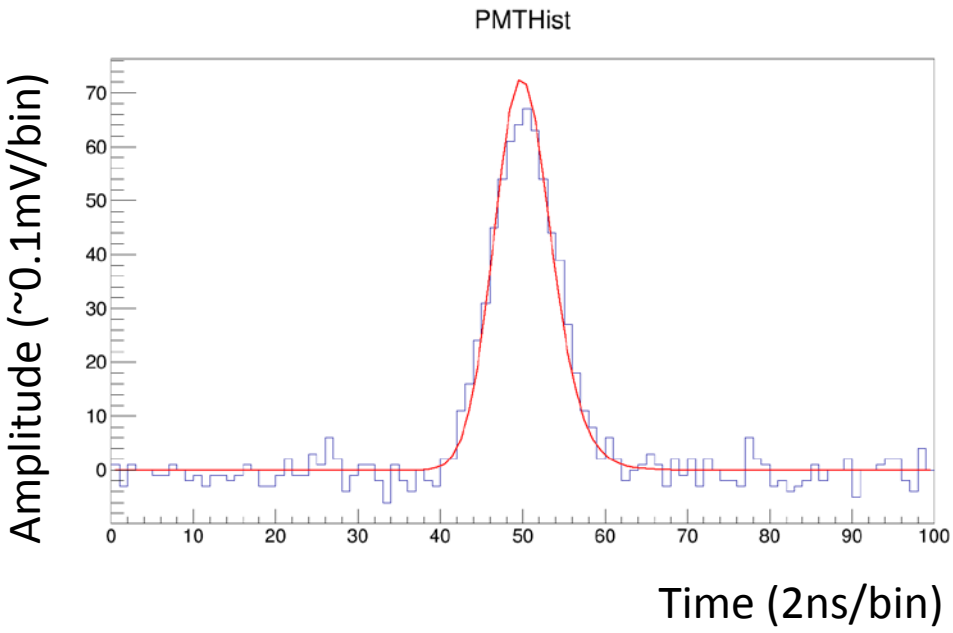
- Timing resolution $\sigma \leq 0.5$ns for 1 photo-electron
- Noise ≤0.1PE
- Dynamic range
  - 1,000 PE over 1ms
    - What is it over 50ns, 250?
  - Maintain PMT linearity, i.e. use low gain?
- Power dissipation ~1W/channel
- Readout scheme
  - Dark noise dominated ~5kHz/PMT
    - Only send time (~TDC) and charge (~QDC) for single PE
    - Could send more data for >1PE pulses
  - Trigger less front end. Send information to backend for all pulses
    - Data suppression occur in backend
  - Daisy-chained in-water front end boards
    - Need fail-safe communication system
- Desirable features:
  - Deadtime-less
  - Ability to identify and time stamp every photo-electrons

Our digitization strategy



Measuring time

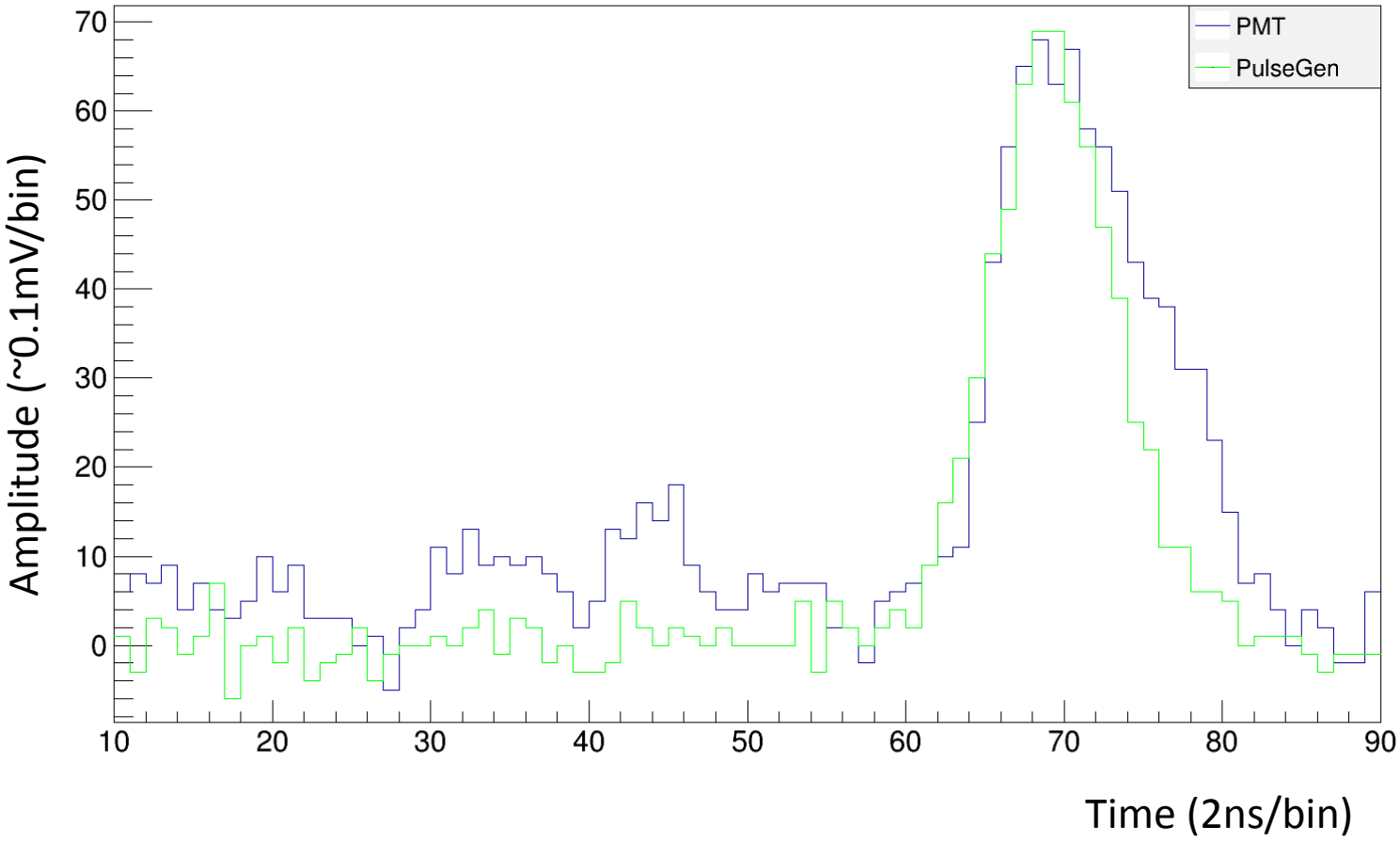
- FPGA based (eventually)
  - Digital CFD
  - Template matching
  - Some smart interpolation
- Analysis offline for now
  - Use fit function
- Performance expectation
  - Resolution scales by rise time over signal to noise
  - Crank the PMT gain yield better time but worse dynamic range / linearity



Test setup

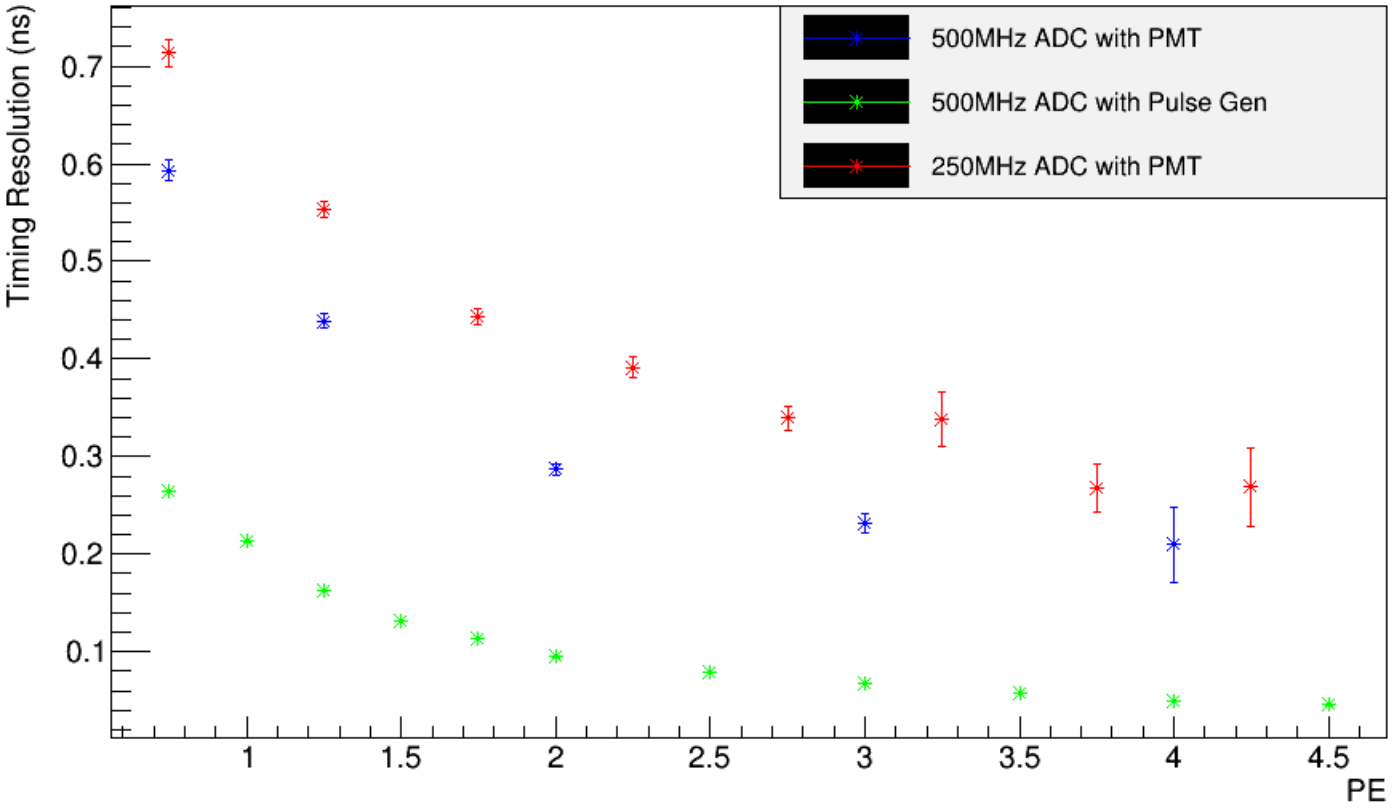
- Signal
  - PMT + shaper
    - R5912 PMT (8”) but Transit Time Spread ~ 3ns and R9875P with TTS<0.5ns but very fast pulse
    - Shaping using DEAP signal conditioning board. Not optimized for timing resolution
  - Arbitrary waveform generator
    - Allow changing pulse shape, and amplitude
- Digitizers
  - 500MHZ, 14bits, CAEN V1730
  - 250MHz, 12bits, CAEN V1720
  - 100MHz, TRIUMF custom FADC for GRIFFIN experiment
- Pulse analysis offline analysis for now
  - Test CAEN digital CFD later this year

PMT+SCB vs Arbirtrary waveform generator



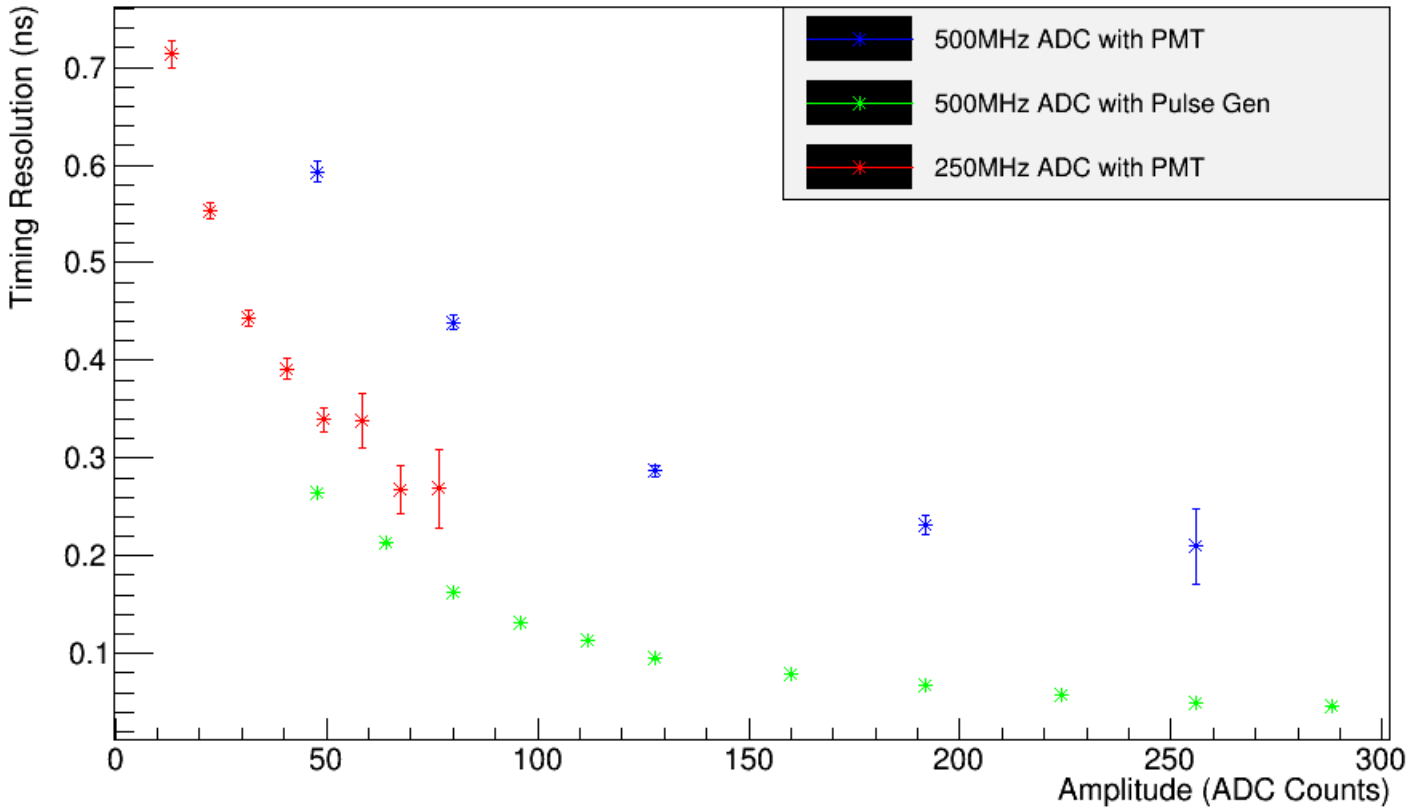
Timing resolution vs PE

PE is not a well defined quantity however…



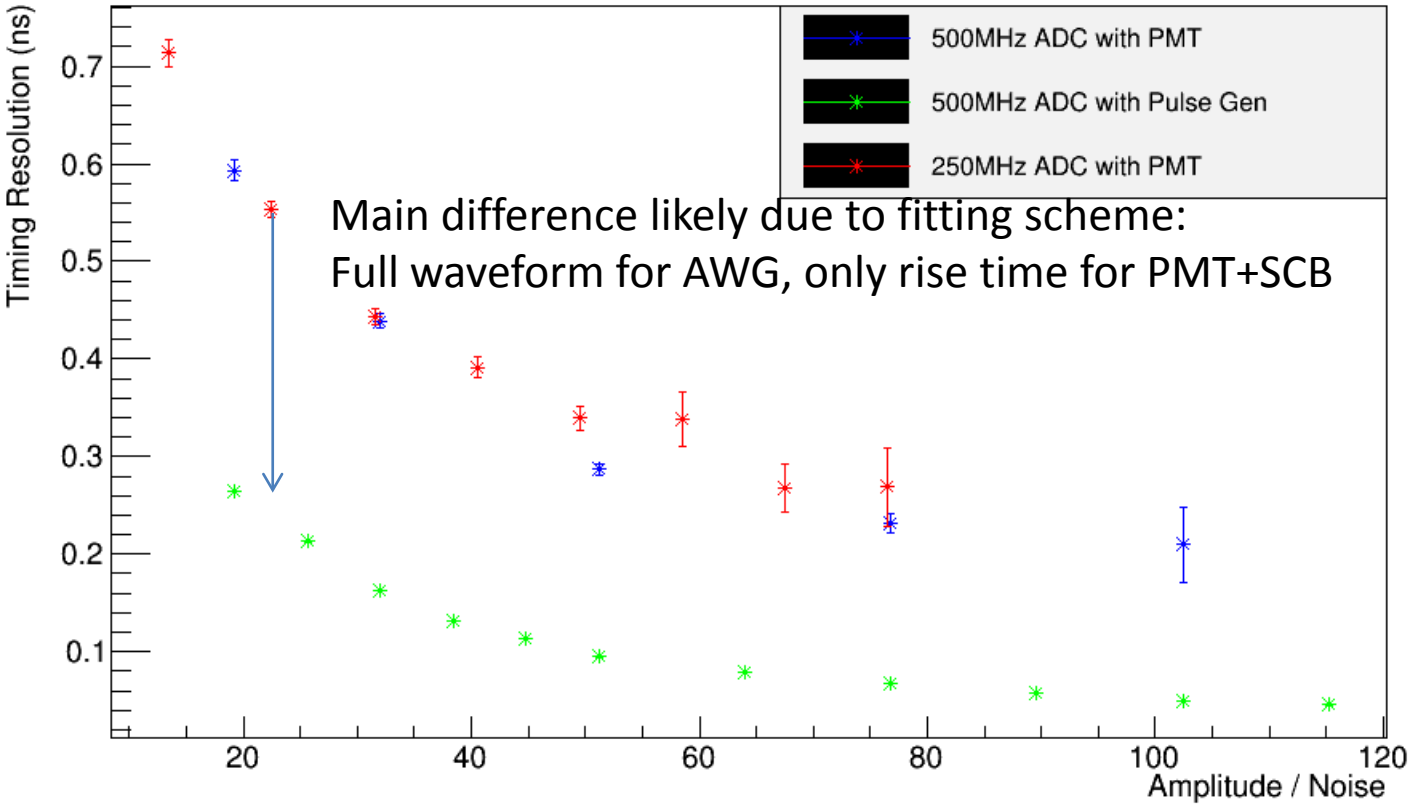
Timing resolution vs amplitude

Cranking up the PMT gain helps but compromise dynamic range.
Single PE amplitudes should be ~20ADC for 12 bits ADC and 80ADC for 14 bits ADC
So inferred SPE resolution is 0.55ns for 12bits/250MHz ADC, 0.42ns for 14bits/500MHz ADC



Timing resolution vs S/N

Good news: speed does not matter much... If rise time is the same



Future test plans

- Using AWG in next 2 months
  - Compare 500MHz, 250MHz and 100MHz FADC
  - Investigate scaling with signal to noise and rise time
  - Write a paper
- Build shapers optimized for 500MHz, 250MHz and 100MHz and 12-14-16 bits
  - Investigate performances
    - Especially noise
  - Identify a compelling solution for HK prototype
    - 500MHz is not a valid solution because it is too expensive and power hungry

Work in collaboration with Warsaw

Implementation in HK prototype

- Build on a mezzanine
  - Interface with carrier board
    - Interface specifications to be written by T2K collaboration
    - Carrier board hardware should be fleshed out
- Start design work in March 2015
  - Mezzanine hardware
  - Firmware
    - Step 1 shipping raw waveforms
    - Step 2 with online suppression
  - Also investigating the option of having CAEN provide the mezzanine
    - Repackaging existing mezzanine used in VME modules

Rapid-IO for communication

- Set up a project with UBC engineering students
  - Entertaining summary here http://m.youtube.com/watch?v=SLuMxaAzK0s
- Goal was to develop a fail-safe mesh network exploring various options
  - Student focused on rapidIO (as suggested)
  - Did not investigate other options thoroughly
- Development on Altera evaluation boards

RapidIO communication

- What we learned:
  - Multi-layer systems with a lot of build-in fonctionality
  - Very good monitoring and error checking capabilities
  - Students achieved 900Mbps so ~90% efficiency with fix routine
  - Students developed on the fly routing capabilities but efficiency only 50%
    - And on the fly re-routing is probably not desirable
- Overall promising solutions

Summary

- Promising results with flash ADC
  - Will start specific implementation for HK in 2014
    - Start with shaper and use commercial FADC
    - In collaboration with Warsaw group
  - Design and build mezzanine prototype in 2015
- Will also investigate added value of flash ADC regarding physics
- Promising results with rapidIO protocol
  - Flexible routing scheme and error checking
  - Development to continue in house
    - Mostly driven by other projects