Detector Electronics II FADC Optimization

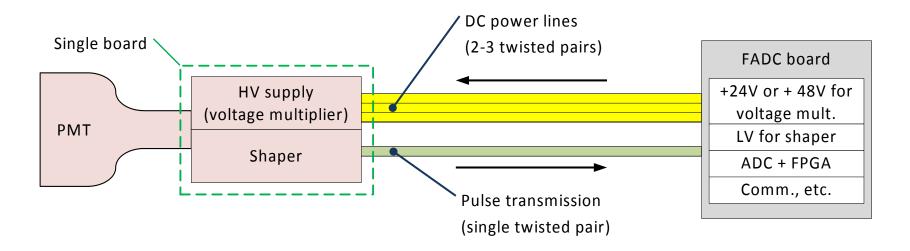
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What's in the Eol

- FADC digitization.
- Pulse stretching (i.e. pulse shaping).
- Standard commercial ADC:
 - 12-16 bits, 80-500 MHz.
- FPGA processing to find PMT hits and calculate pulse time and charge.
- 0.1-1250 p.e. dynamic range.
- Distinguish hits that differ by 10s of ns.

Suggested Setup



- HV supply and the shaper on a single board
- HV control link over the DC power line
- Fully differential signal transmission
 - Improved EMI performance
 - Ground is not used in signal transmission

- Use standard UTP telecom cable (4 pairs)
 - Single cable per PMT (no additional HV cable)
 - No HV going through the water

Simulation Purpose

- Get an initial estimate of the performance of the FADC acquisition scheme
- Try to determine optimum shaping, sampling frequency and the number of the ADC bits.
- Investigated parameters:
 - Time resolution
 - Charge resolution
 - Ability to distinguish piled-up pulsed
- What we want:
 - Lowest number of bits, lowest sampling frequency
 - But still meet performance requirements

ADC cost (USD per channel)

Resolution

		10 bits	12 bits	14 bits	16 bits
ing Rate (min)	80M	\$4 to \$8	\$7 to \$33	\$10 to \$40	\$42 to \$58
	100M	\$6 to \$25	\$15 to \$34	\$25 to \$58	\$57 to \$68
	125M	\$6 to \$22	\$15 to \$35	\$21 to \$78	\$63 to \$72
	150M	\$19 to \$21	\$19 to \$48	\$33 to \$96	\$52 to \$79
	200M	\$25 to \$41	\$31 to \$56	\$55 to \$110	
	250M	\$18 to \$35	\$30 to \$65	\$37 to \$106	\$93
ldι	300M	\$47	\$85	\$182	\$116 to \$133
Sampling	500M		\$110 to \$193		
	1G		\$162	\$272	

NOTE: This is only an ADC IC cost – it does not include additional analog electronics (anti-aliasing filter, shaper, cables, connectors, etc.)

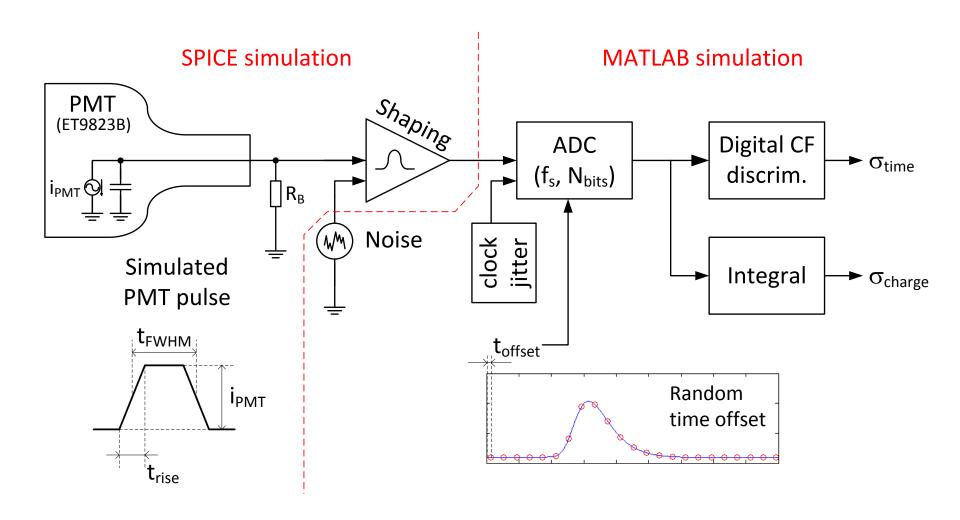
Eol Simulations 1/2

- Dynamic range: 2000 p.e. (to accommodate pulse pile-up)
- Pulse amplitude: 1 p.e. and 10 p.e.
- No PMT randomizations
 - Test only electronics-related errors
- Almost optimum shaping (LT-SPICE simulation)
 - 6th or 7th order RC-integrator
 - Approx. 3.5 samples on the rising edge
 - Use real amplifier models (i.e. apply bandwidth and slew-rate limitations, account for noise)

Eol Simulations 2/2

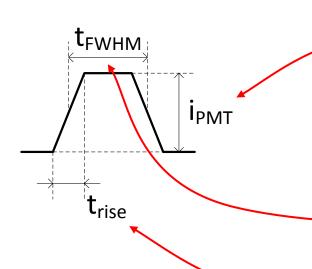
- Simulated parameter sets:
 - Fs = 80 MHz, 125 MHz, 250 MHz
 - Number of bits: 10, 12, 14, 16
- ADC simulation (done in MATLAB):
 - Time-base jitter
 - Random time offset between beginning of the shaper pulse and the phase of the sampling clock
 - Ideal ADC non-linearity was not simulated (yet)
- Time extraction using a digital constant-fraction discriminator

Eol Simulations – Setup



Eol Simulations – PMT pulse

Excerpt of the ET9823B datasheet (5" PMT) 2000 p.e. $\rightarrow i_{PMT}$ = 150 mA



Problem of the PMT gain:

$$q = 150 \cdot 10^{-3} \cdot 6 \cdot 10^{-9} = 9 \cdot 10^{-10} = 900 \, pC$$

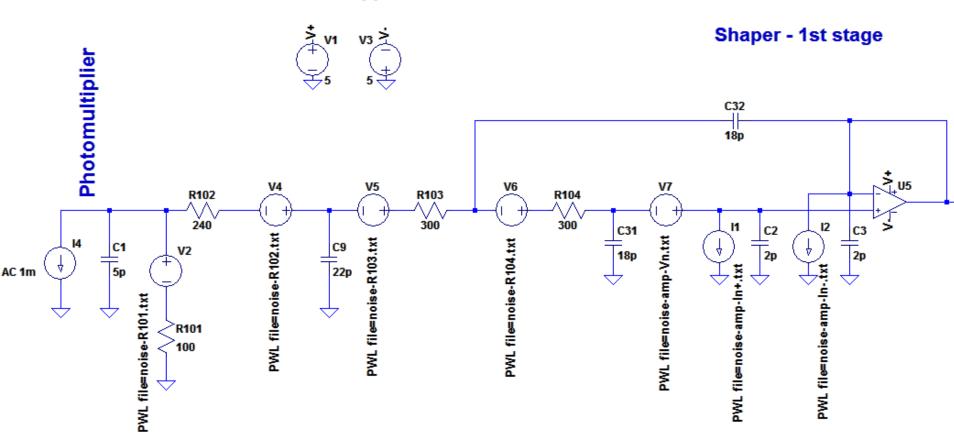
$$\frac{9 \cdot 10^{-10}}{1.6 \cdot 10^{-19}} = 5.625 \cdot 10^9 e$$
 2000 p.e.

pulsed linearity (-5% deviation) divider A divider B	mA mA	50 150	
rate effect (I _a for ∆g/g=1%): magnetic field sensitivity:	μΑ		
the field for which the output decreases by 50 %			
most sensitive direction	T x 10 ⁴	8.0	
temperature coefficient:	% °C ⁻¹	± 0.5	
timing:			
multi electron rise time	ns	3.5	
multi electron fwhm single electron rise time	ns ns	$\frac{6}{2.7}$	
single electron fise time	ns	3.6	
single electron jitter (fwhm)	ns	2.4	
transit time	ns	 55	
anode sensitivity in divider B:			
nominal anode sensitivity	A/Im	5000	
max. rated anode sensitivity	A/lm	10000	
overall V for nominal A/Im	V	2400	3000
overall V for max. rated A/lm	6	2550	
gain at nominal A/lm	x 10°	80	

Dropping PMT linearity requirement for large pulses is considered.

Eol Simulations – Shaper

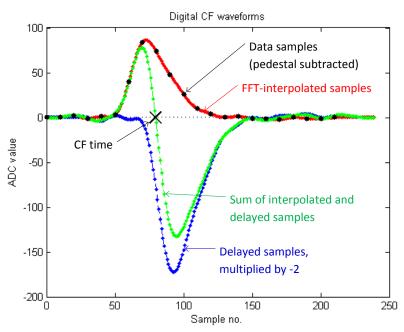
Power supplies

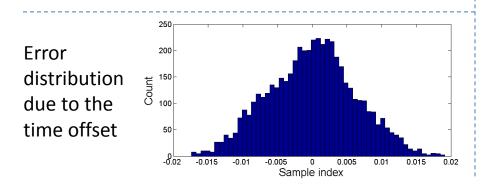


Need to stay within common mode range of the amplifier

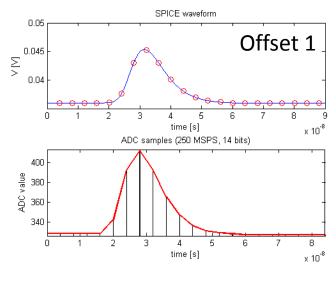
Eol Simulations - Time Extraction

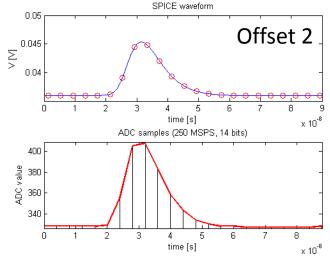




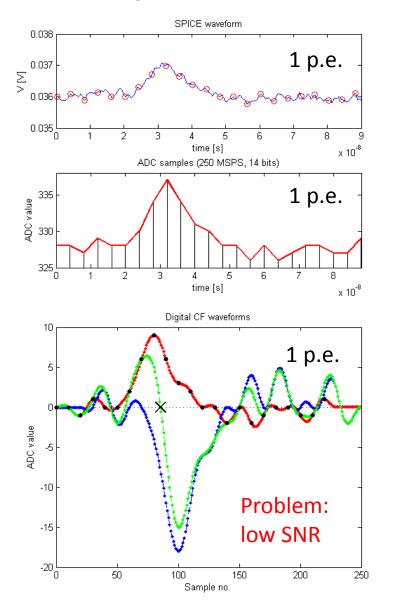


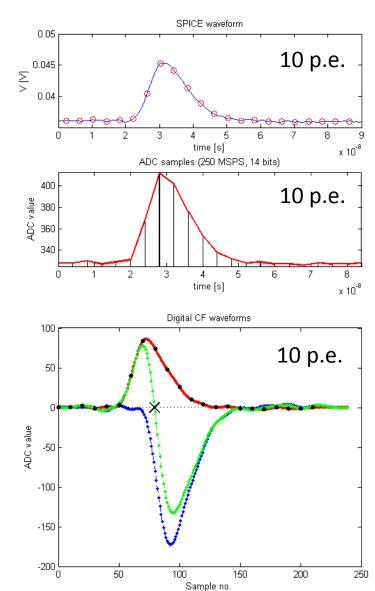
Error due to random time offset between sampling clock and the leading edge



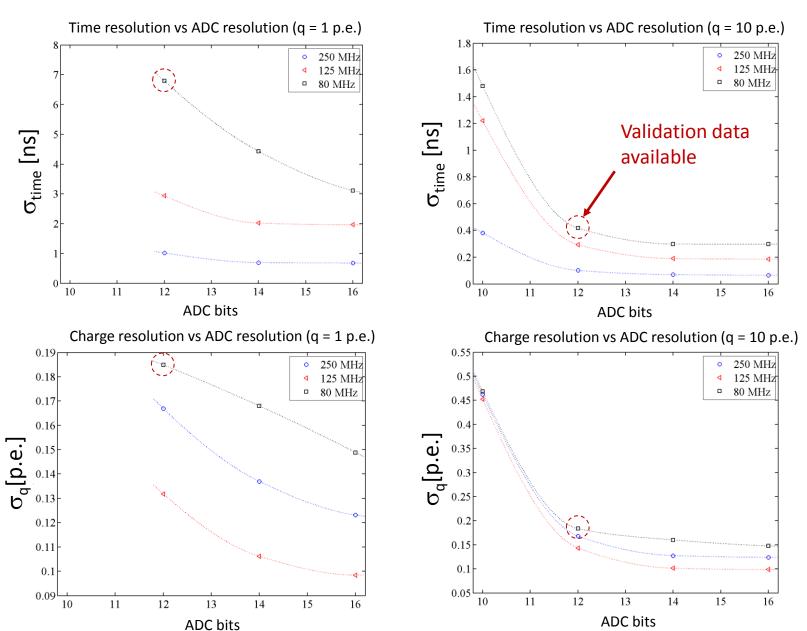


Example waveforms (250 MSPS, 14 bit)





Eol Simulations - Results



Eol Simulations – Conclusions

- Charge resolution is not very sensitive to signal-to-noise ratio even for noisy signals we get <1 p.e. resolution.
- Time extraction using a digital CF-algorithm is heavily dependent on signalto-noise ratio.
- If the model is accurate, then, using the assumed methods of signal processing, a 12-bit 250 MSPS system should provide sufficient timing performance, i.e. the limiting factor will be the PMT transit time spread.

Improve SNR

- Design all electronics in such a way that we can operate PMT at the highest possible gain.
- Decide whether we need PMT linearity in the full dynamic range.
- Fully understand shaper design.
- IceCube's pulse-compressor?

Optimize algorithms

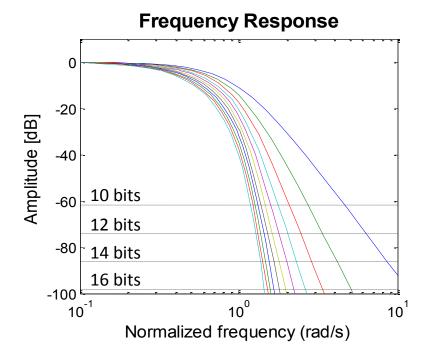
- Try a different algorithm for small pulses – see how radar people do their tricks (matched filtering)
- Optimize shaping, investigate various shaping techniques
- Apply digital filtering of input signal (should improve SNR)

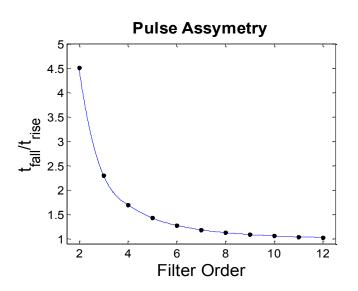
Shaper design 1/2

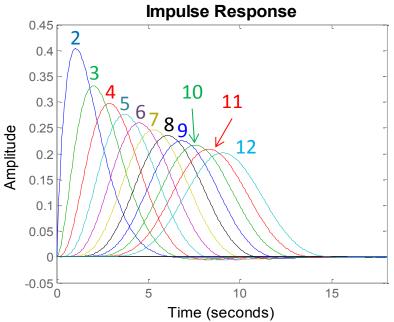
Shaper = low pass filter

- Filter design is a well established theory
- Bessel-type so that there is no ringing
- Amplifier bandwidth should be significantly higher than the stop-band corner frequency.

ADC SNR = (6.02N+1.76) dB

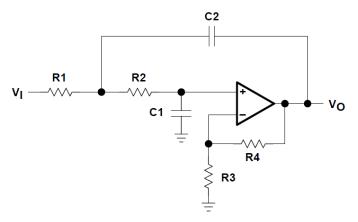




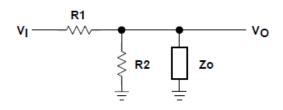


Shaper Design 2/2

Building block – Sallen-Key architecture

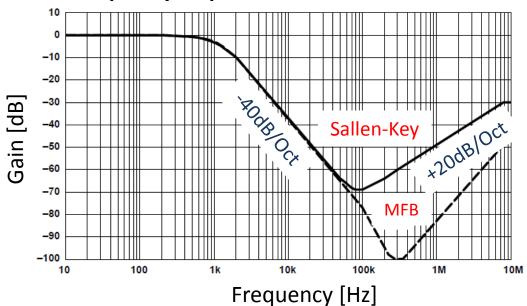


High frequency model



$$Zo = \frac{ZO}{1 + a(f)\beta}$$

Frequency response – real 2nd order LP filter



Advantages:

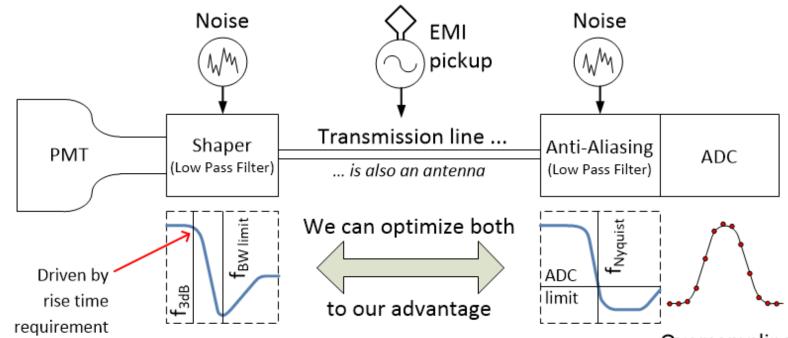
- Does not change pulse polarity
- More dynamic range (can use non-symmetric supplies)
- Possibly can use current-feedback op-amps

Disadvantage:

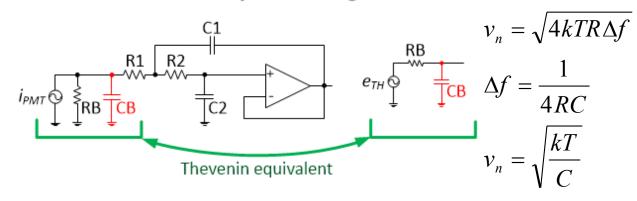
 Undesired stop-band behavior due to amplifier bandwidth limitations

Source: Texas Instruments, SLOA049B

Signal Chain



Dynamic range issue



Oversampling

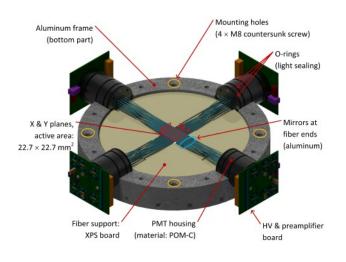
Know output from the shaper



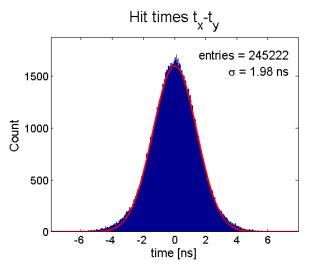
Use digital low-pass filtering to remove unwanted signals

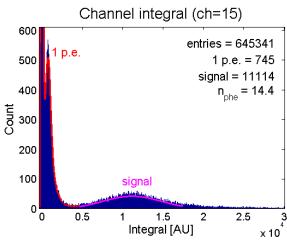
Model Validation 1/2

- Model validation possible using data from beam tests done for the COMPASS experiment.
- Scintillating fiber detector, similar acquisition scheme (Kuraray fibers, H8711-10 PMT, Shaping, ADC \rightarrow 12 bits, 80 MHz).
- Electron beam data available (test done at ELSA, Bonn, February 2014). Further tests in CERN, October 2014.
- 1.98 ns time resolution for a system with an average signal level of 14.4 p.e. and the dynamic range of approx. 60 p.e. !!! – probably due to SNR, investigation is under way.









Model Validation 2/2

- First prototype shaper design under way, to be completed next week (schematic).
 - Three versions for 100 MHz, 250 MHz and 500 MHz systems.
 - For now single-ended, 50 Ohm input impedance,
 50 Ohm output.
- Make tests using shaper prototype and pulse generator (Warsaw + TRIUMF) and various commercial ADC modules.
- Coordinate with Fabrice more tests with arbitrary waveform generator.

Conclusions & Work Plan

- Achieving desired performance will be a challenge for a single channel system, but we should try to avoid split gain system.
 - There is still some time to try various solutions.
- SNR is a critical issue needs to be improved in any way possible.
- My plan for the near future:
 - Finish shaper design and send it to Fabrice.
 - Go on holiday ☺
 - Investigate worse than expected time resolution of the SciFi and try to improve it by applying matched filtering algorithms.
 - Add an ADC non-linearity simulation to the model.
 - Run a second set of simulations with improved shaper designs and try time extraction using both the digital constant-fraction algorithm and matched filtering algorithms.
 - Analyze results and decide on optimum pulse shape (i.e. rise time and filter order).
 - Modify shapers for the SciFi before October test to see if the time resolution will improve.
 - Analyze ability to distinguish piled-up pulses.
- At some point, add PMT simulation and time spectrum of arriving photons.