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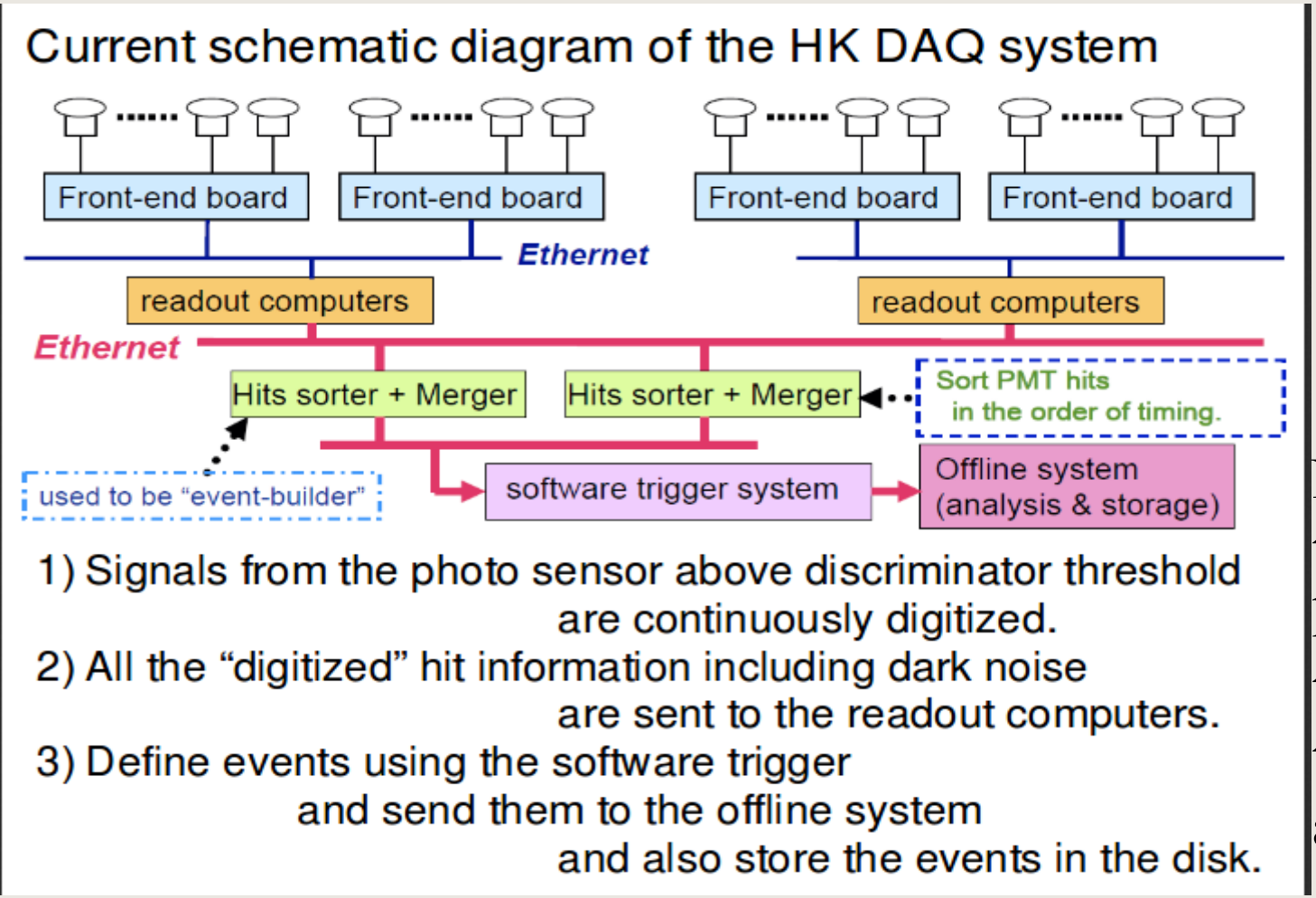
nuPRISM Electronics; FADC

Thomas Lindner | TRIUMF
NuPRISM Meeting, Feb 2014

NuPRISM : Baseline Plan

- Baseline plan would be to make the nuPRISM electronics as similar as possible to HK electronics. Features of electronics:
  - Front-end electronics, including digitization and high voltage, underwater, as close to PMTs as possible.
  - Mesh network between front-end cards.
  - FADC digitization (Canadian suggested option).
- Using similar electronics maximizes benefit of nuPRISM as HK prototype.

Reminder: Hyper-K Electronics/DAQ



No global hardwar
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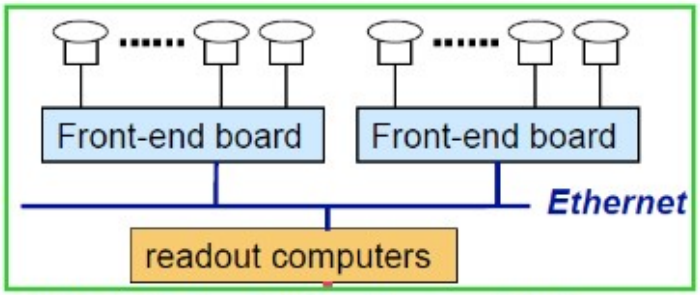
Hayato-san, previous HK meetings

Hyper-K Communication Scheme

Possible front-end electronics module connections

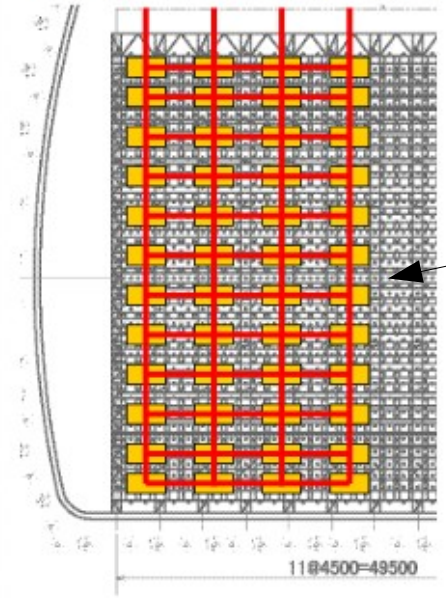
~ Design of the data flow



1) Assuming to use 1GbE

- Robustness
- Power consumption

HK detector Side view



2) Connect neighboring Front-end boards each other

- Reduce total length of the cables
- Avoid single point failure

Usually, data collected by a module are transferred to the upper module (vertically)

If a module failed, transfer data to the other module instead of the failed module (horizontally).

Data rate at the top modules has to be enough smaller than 1Gb/sec.

Hayato-san, previous HK meetings

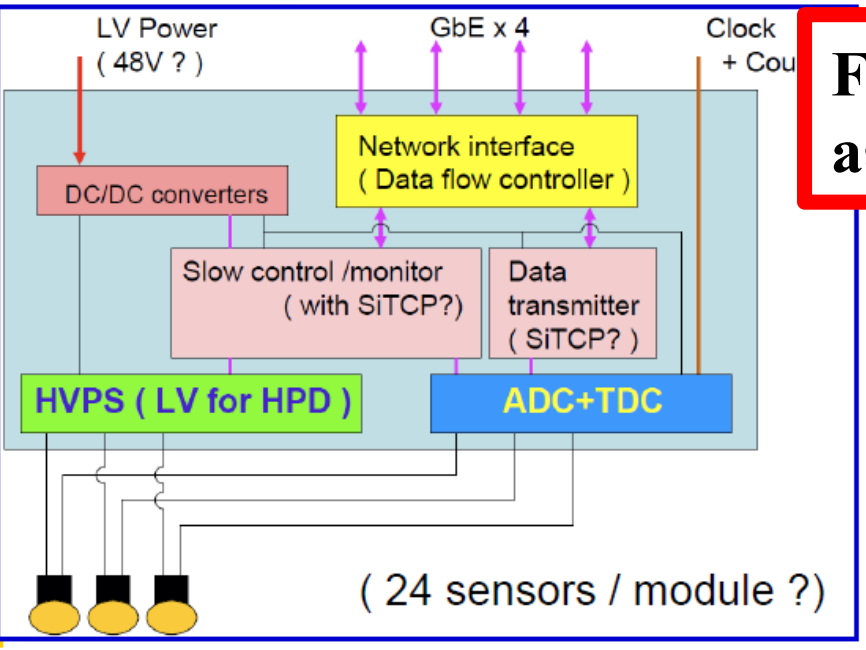
Electronics sit in water: Redundant communication needed.

Though maybe less likely now to have in-water electronics...

HyperK: Baseline Front-end Digitization

- Baseline signal digitization: TDC + ADC (like SK).
- One potential concern: the TDCs used for SK electronics are no longer available; need to find new ones.
  - Possible chips being investigated.

Schematic diagram of the front-end board



Hayato-san, previous HK meetings

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For NuPRISM, use FADC as alternative to ADC/TDC.

QTC/ADC specification (performance)

irements)

~ 0.3 mV)

HIT

e. RMS (< 5 p.e.)

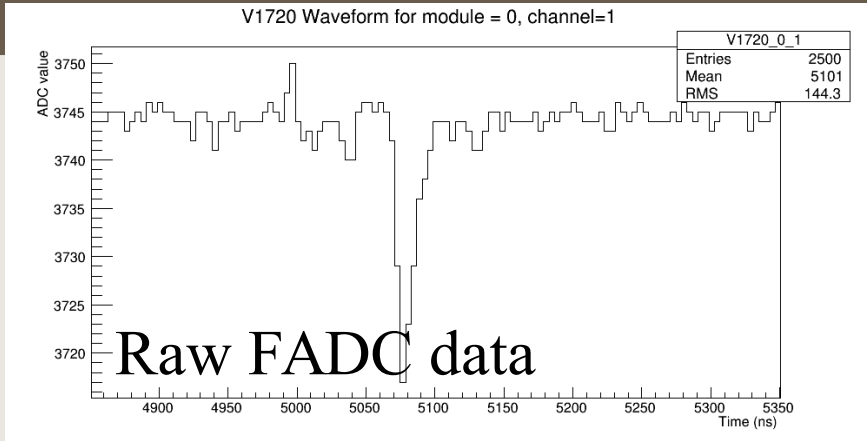
- **Charge Dynamic Range** 0.2~2500pC (0.1 ~ 1250 p.e.)
- **Timing Respons** 0.3ns RMS (@ 1p.e.)
  0.2ns RMS (> 5p.e.)

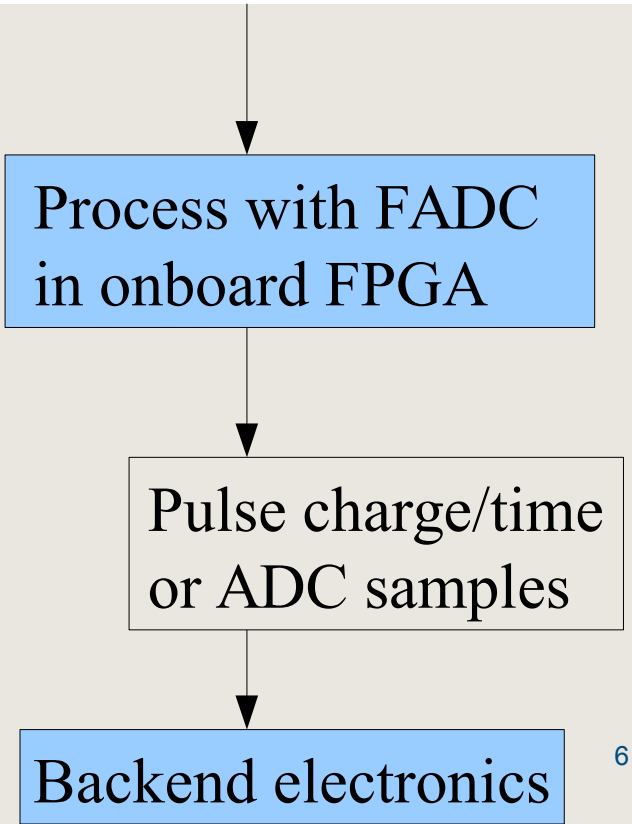
TDC specification (performance)

- **Least Time Count** 0.52 ns
- **Time resolution** 250ps
- **Dynamic range** ≥15bits
- **Continuous running mode**

FADC Digitization - Overview

- Proposal is to use FADC (Flash ADC) instead of TDC/ADC.
  - Something like 125-500 MHz sampling, 12-16 bit resolution.
- FADC data is continuously processed using FPGA on front-end board; firmware finds hits and only send pulse summary to backend.
  - Pulse summary is either just Q/T (for small pulses) or a set of ADC samples (for large pulses).





FADC Option - Overview

Current work is focused on these two questions:
1) Can we quantify gains of FADC? What physics does this help? *Starting WCSim studies, but nothing to show yet.*

2) Can we meet timing resolution and dynamic range requirements? (reminder: 0.3ns resolution, 0.05-1250 PE range)
Focus of this talk is tests of timing resolution for different FADC designs.

Pros

- More information on charge distribution 1us after first pulse.

Cons:

- Higher power (?) and cost (?)
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

FADC Benefits for nuPRISM

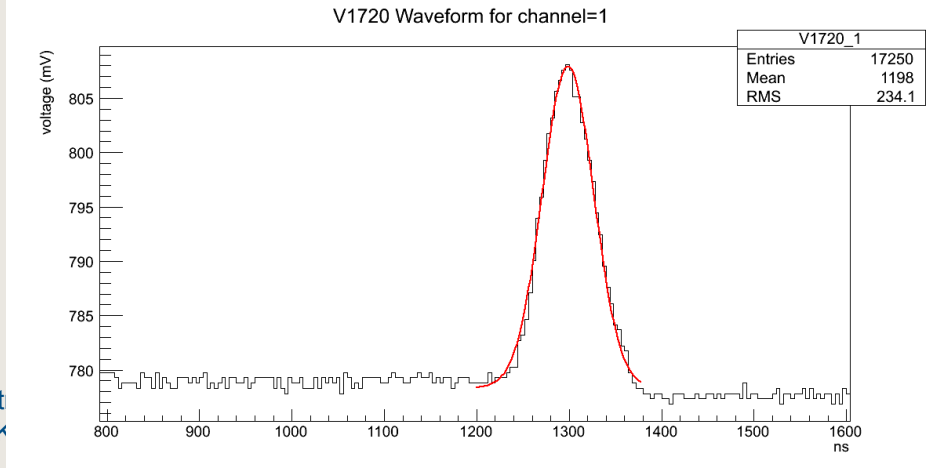
What benefits do you get from more detailed/dead-timeless FADC digitization?

For nuPRISM there will be a large number of events in each beam spill. Having the maximum amount of information about the time profile of each channel (with no dead-time!) will be very critical, particularly if we try to reconstruct multiple events in a single beam bunch.

Muon and decay electron as seen in ND280-FGD.

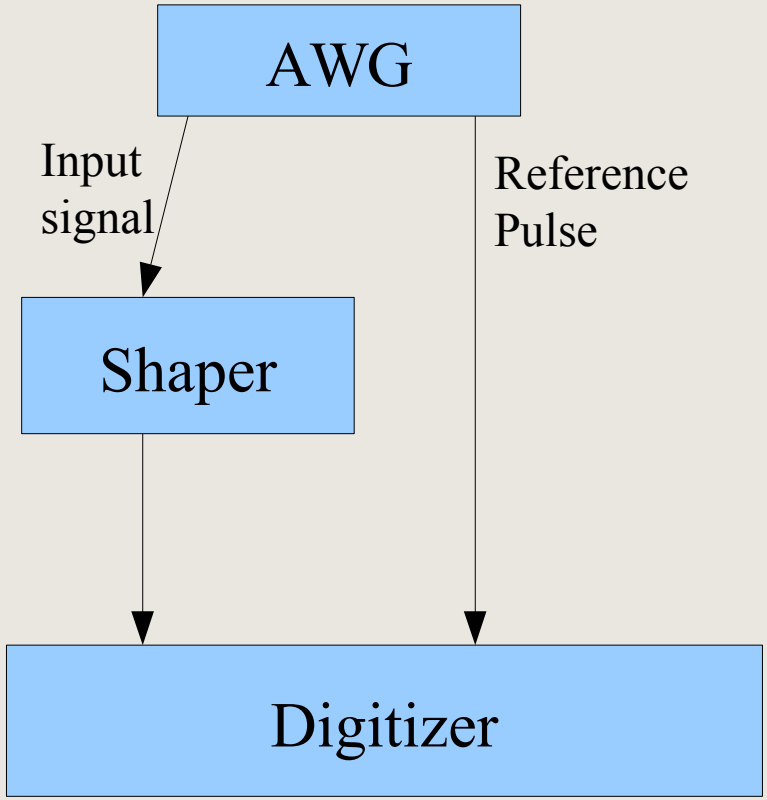
Time Measurements with digital waveform

- Extracting precise time from FADC pulse depends on many factors:
  - Low electronics noise
  - Sufficient number of samples on leading and falling edge.
    - Need to shape pulse if not enough samples
  - Precision of ADC
    - Higher precision ADC (14 bit vs 12 bit) can help, but only if noise is small
  - Frequency of ADC
    - Faster ADC is better (but higher power, more expensive)
- Talk will show ongoing studies of balancing these characteristics using set of shapers from Marcin (next talk) and TRIUMF digitizers.



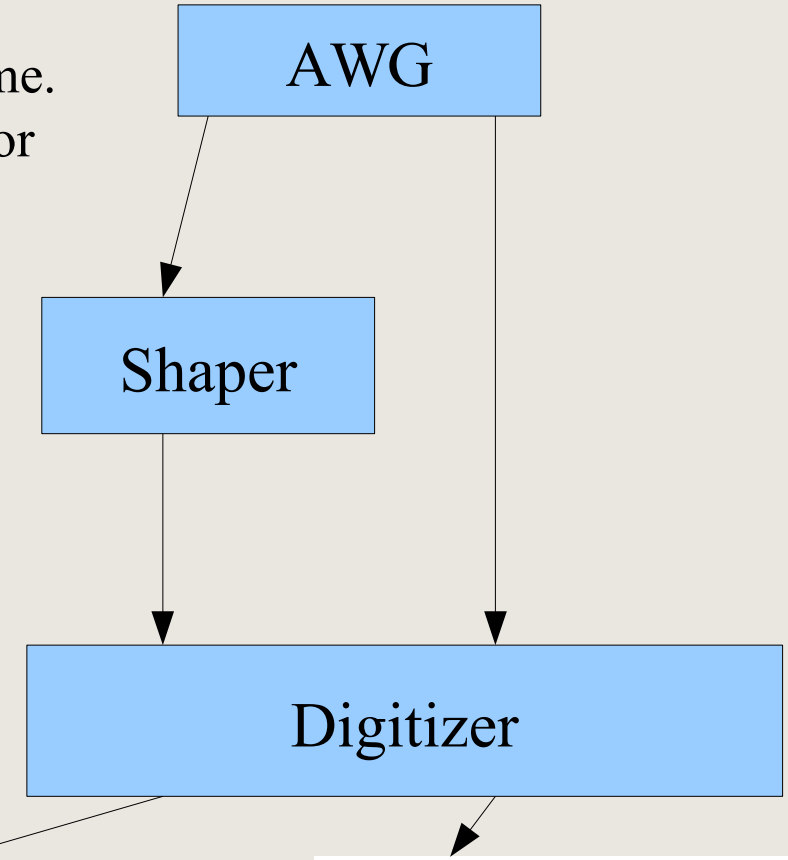
Test Setup

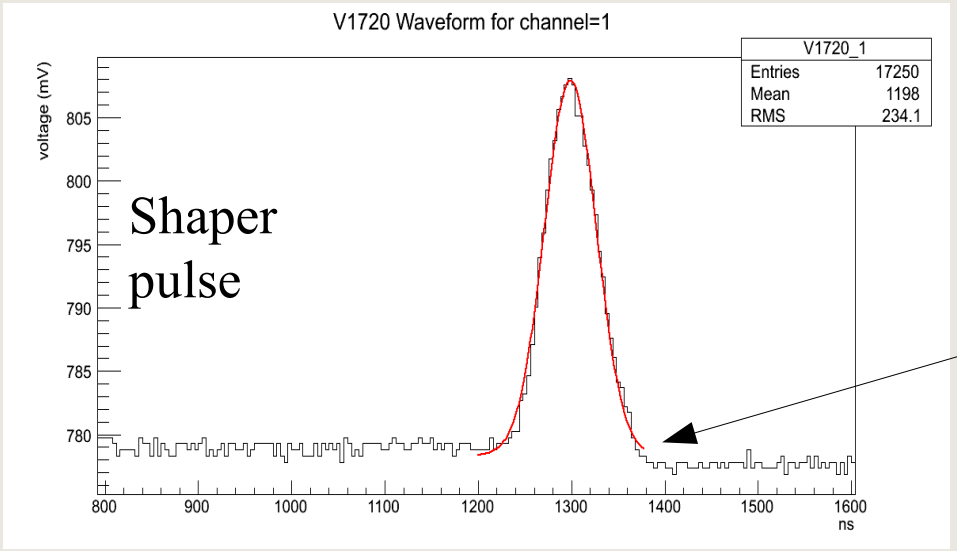
- Use arbitrary waveform generator (AWG) to create input pulses.
  - AWG has no intrinsic pulse jitter (unlike PMTs) so can probe directly the timing resolution of electronics.
- Have on hand 250MHz and 500MHz digitizers; acquiring 100MHz digitizer soon.

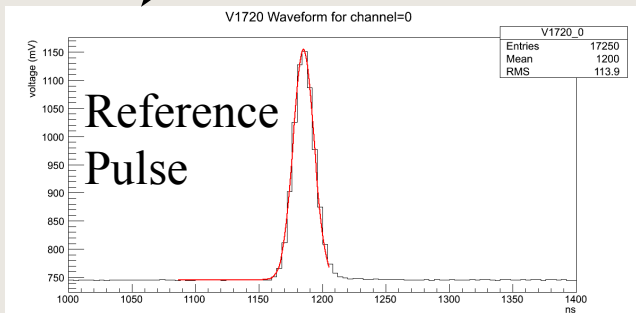


Test Setup Analysis

- Currently fit the pulse to extract pulse time.
  - Eventually want to use digital CFD or matched filter, closer to what can be implemented in FPGA.
- Width of histogram of signal – reference times gives the timing resolution.







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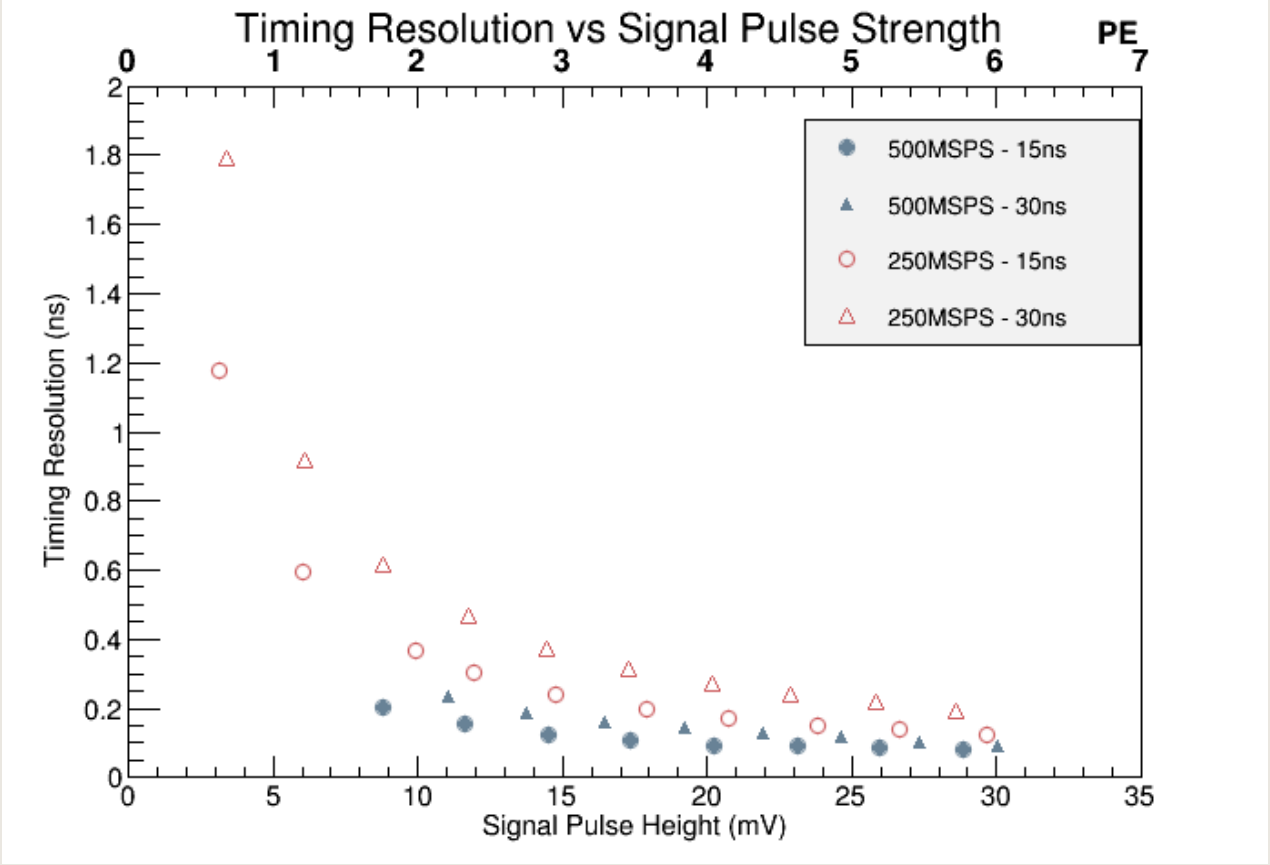
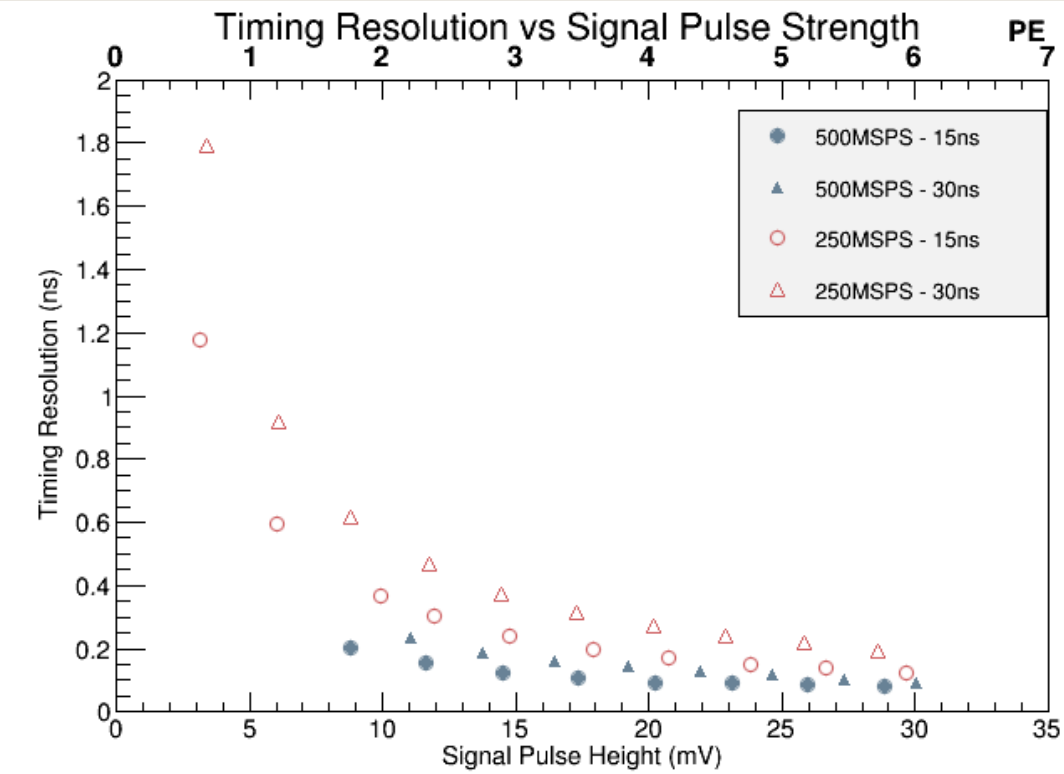
Timing Resolution Results

- Plot shows timing resolution vs signal pulse height for various combinations of shapers and digitizer.
- Results are preliminary; results depend fairly strongly on details of how well fitting is done. This has not been optimized much.



Timing Resolution Results

- For pulses above ~10mV we can meet timing resolution requirements with 250MHz digitizer.
- Can play with PMT gain to make single PE pulses this big, but need to understand implications for dynamic range.
- Ongoing work to compare these results with Marcin's simulation and develop reliable models of electronics.



Budget Estimate (assuming 3000 channels)

- FADC board (16 ch): quantity = 220, cost per board = $1000, total = $220,000.
  - Custom board for FGD (made at TRIUMF) was $700, for 64 channel board.
  - Doesn't include cost for development, that will be covered separately.
- High voltage: Don't directly have any estimates of the cost for high voltage on front-end cards.
  - For 2km it seems they had $75/channel ($225k total), but I don't know different that would be for in water high voltage.
  - Hayato-san estimated $100/channel ($300k total) in early HK meeting.
- Surface electronics: we estimated this at $84/channel, $250k total.
  - This is based on custom electronics cards at surface; could probably get away with something simpler with PCs.
- Total : $770k. Other estimates are higher, near $1.3M.

Future Plans

- Summer 2015: finalize decision about digitizer frequency for prototype.
- Summer 2015: start design of digitizer card.
- Fall 2015: fabricate and test prototype digitizer card.
- 2016: do production of digitizer cards for HK prototype.

Conclusions

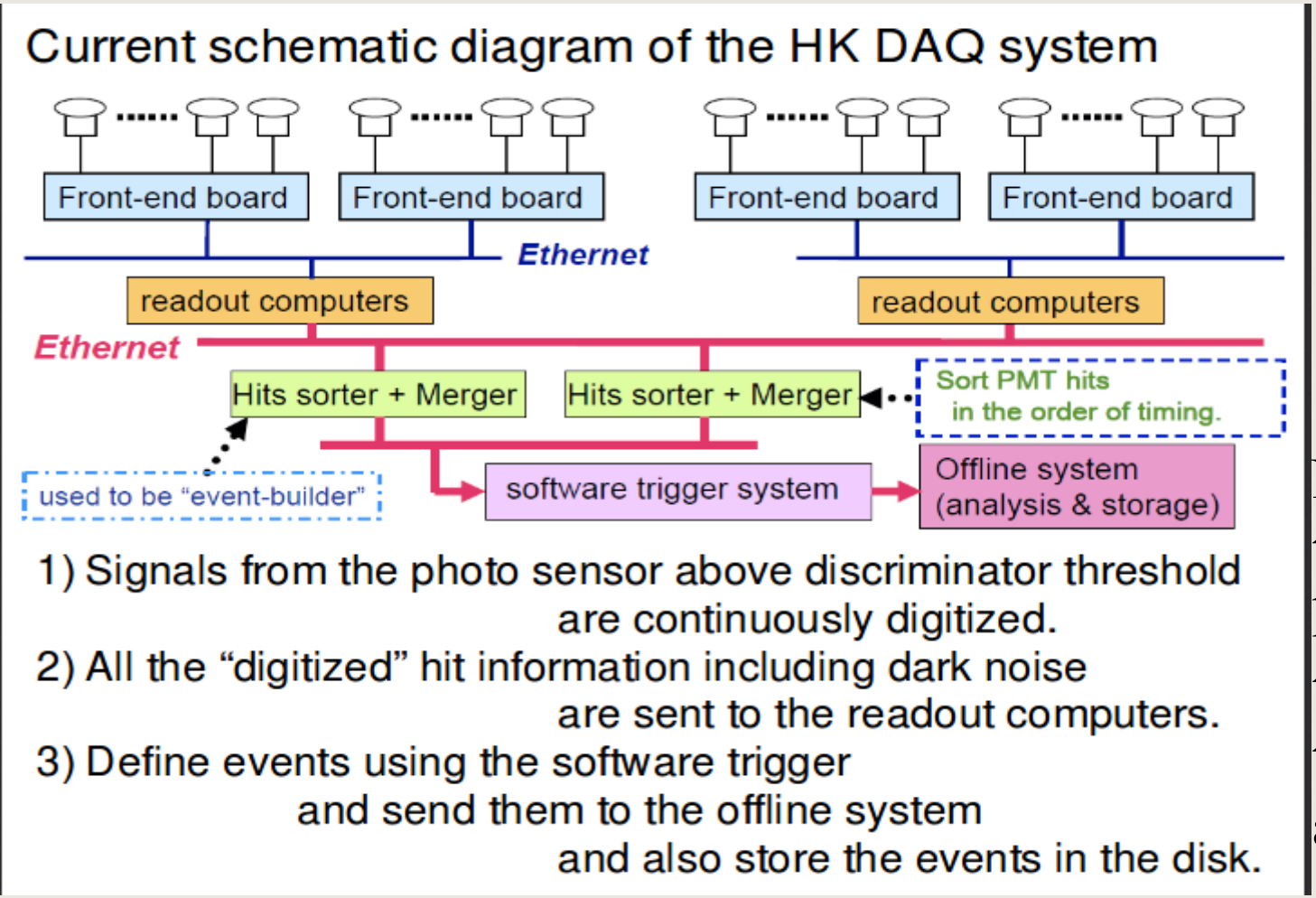
- Working on understanding which digitizer can be used to meet timing resolution requirements.
  - Based on Marcin's studies have fabricated set of shaper circuits.
  - Have done initial tests of achievable timing resolution; lots more work to be done.

Backups

NuPRISM FADC Data rate

- For HK the data rate from FADC is dominated by data from PMT dark noise.
- How about data rate per channel for nuPRISM?
  - Dark noise: 10kHz * 12 byte/hit = **120kB/s**
  - Spill hits: 8bunch*20%hit*50 byte/hit *0.5Hz = **40B/s**
    - Save 30 samples per hit ~ 50byte/hit (large pulses)
    - Assuming 20% of channels are hit in each bunch (for on-axis configuration).
  - Cosmics: 21000 Hz * 20% hit * 50 bytes = **210kB/s**
    - PDG says 70 muons / (s * m^2 * sr) (>1GeV muons).
    - 21000 cosmic muons / s through nuPRISM.
  - Data rate might be dominated by cosmics; need more study.

Hyper-K Electronics/DAQ



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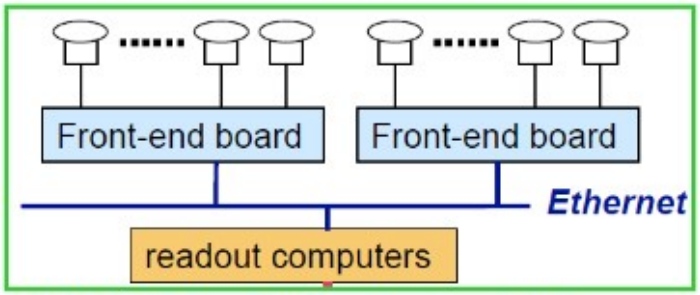

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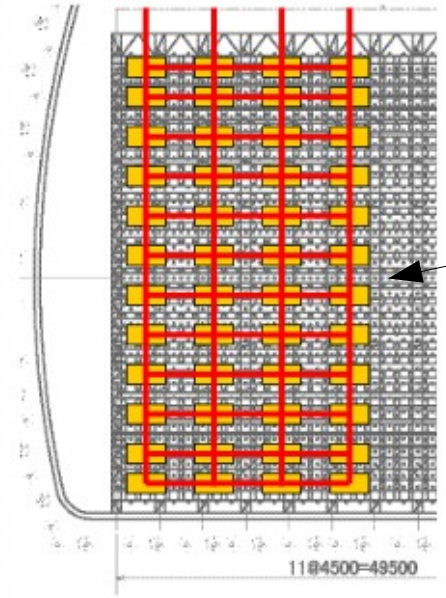

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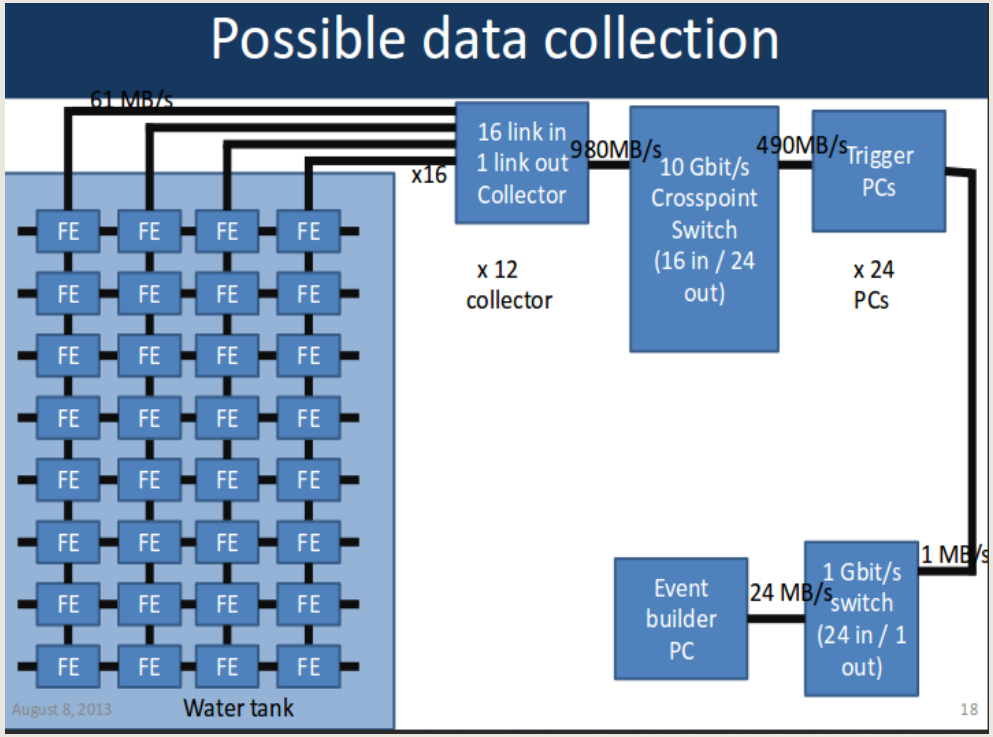
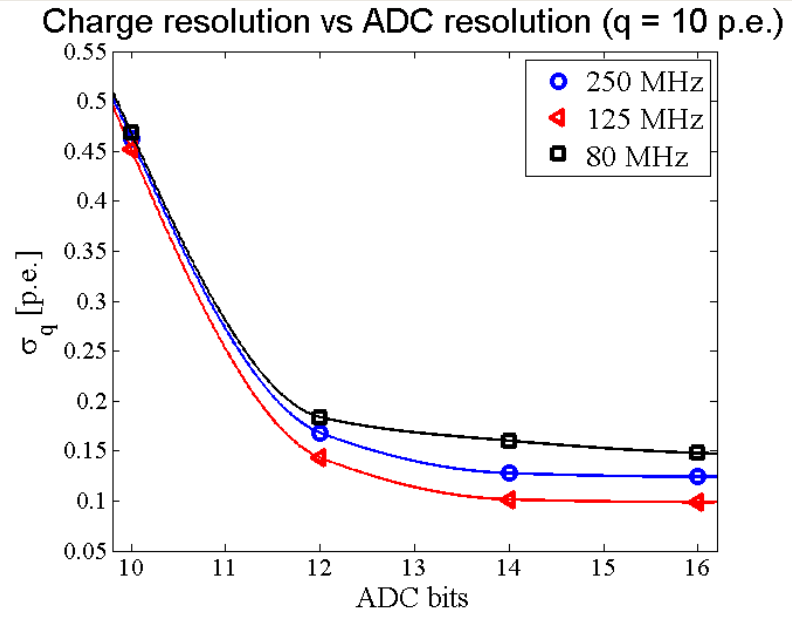
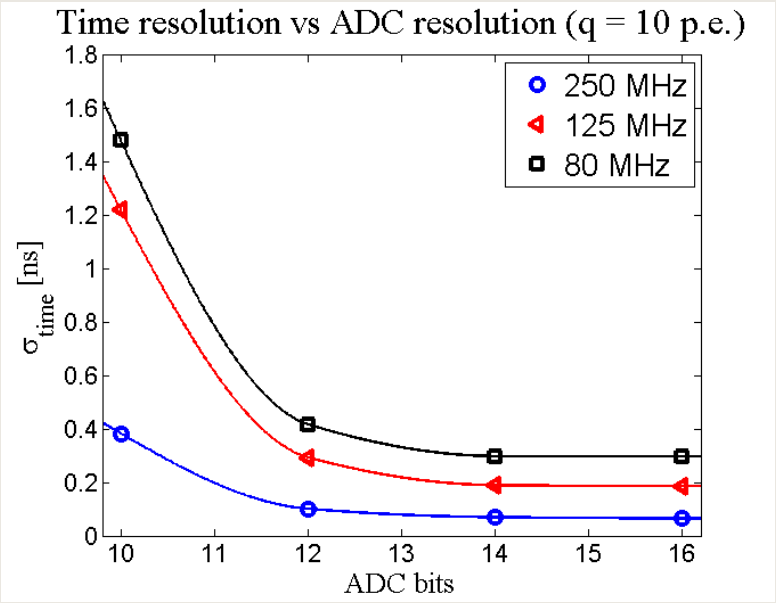
Back-end Architecture

- Possible back-end architecture.
- Data from front-end electronics get time-sliced and sent to different PCs.
- PCs make trigger decisions and decide if event(s) get logged to disk.
- Maximum 12GB/s for rate is dominated by dark noise.



Marcin's Simulation Results





Digitizers

- Currently using set of different commercial CAEN digitizers

V1730
500MSPS

V1720
250MSPS

DT5724 100MSPS

Timing Test Analysis

- Histogram difference between fitted signal and reference times.
- Width is timing resolution.