

Hyper-K Electronics; FADC and Communication Options

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TRIUMF, Warsaw University of Technology
6th HK Open Meeting, Jan 2014**

Overview

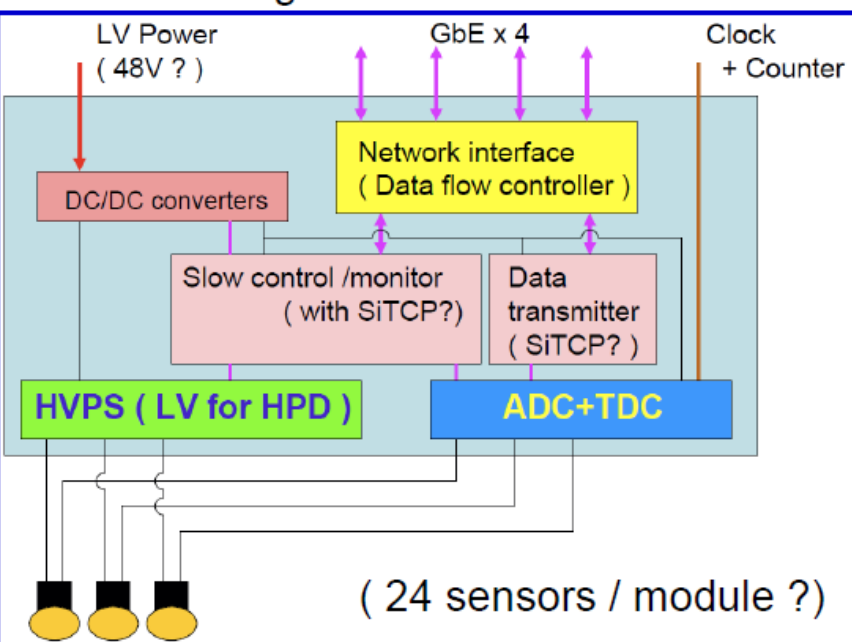
- FADC digitization work
 - Reminder of proposal
 - Work on optimizing shapers
 - Ongoing tests of shaper+digitizer options
- Work on RapidIO communication
- Timeline
- Thoughts on alternate tank designs

HyperK:

Baseline Front-end Digitization

- Baseline signal digitization: TDC + ADC (like SK).

Schematic diagram of the front-end board



QTC/ADC specification (performance)

(current performance = minimum requirements)

- **Built-in Discriminator** $\frac{1}{4}$ p.e. (~ 0.3 mV)
- **Processing Speed** ~ 1 usec/HIT
- **Charge Resolution** ~ 0.05 p.e. RMS (< 5 p.e.)
- **Charge Dynamic Range** 0.2~2500pC (0.1 ~ 1250 p.e.)
- **Timing Respons** 0.3ns RMS (@ 1p.e.)
0.2ns RMS (> 5 p.e.)

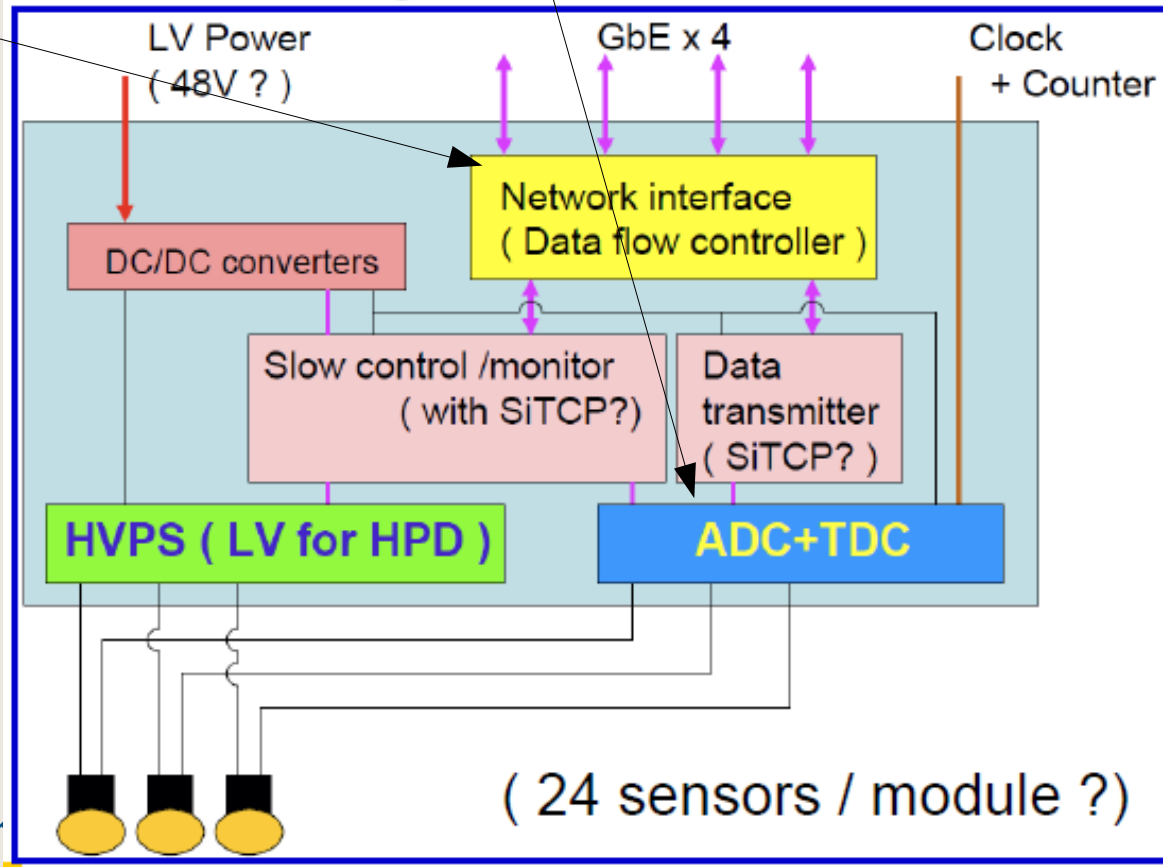
TDC specification (performance)

- **Least Time Count** 0.52 ns
- **Time resolution** 250ps
- **Dynamic range** ≥ 15 bits
- **Continuous running mode**

Canadian Front-end Electronics Interests

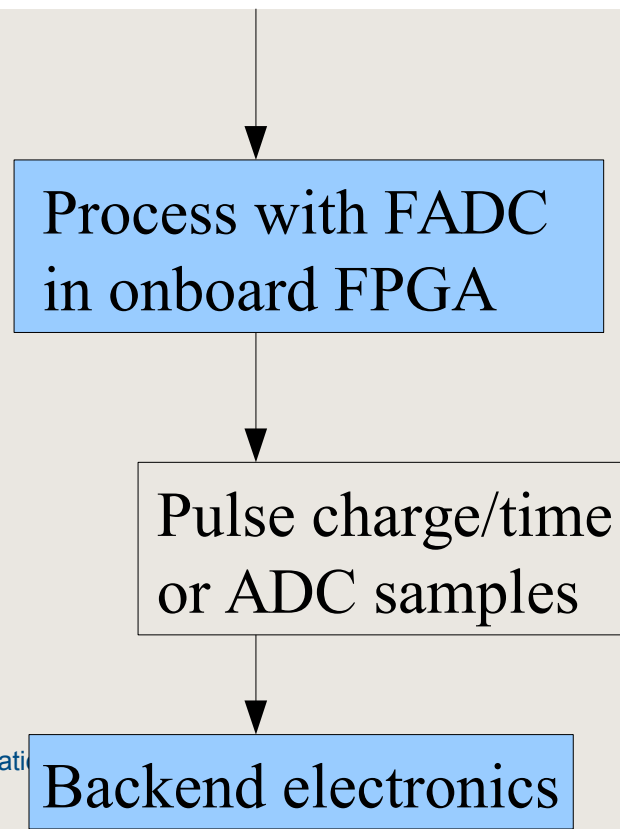
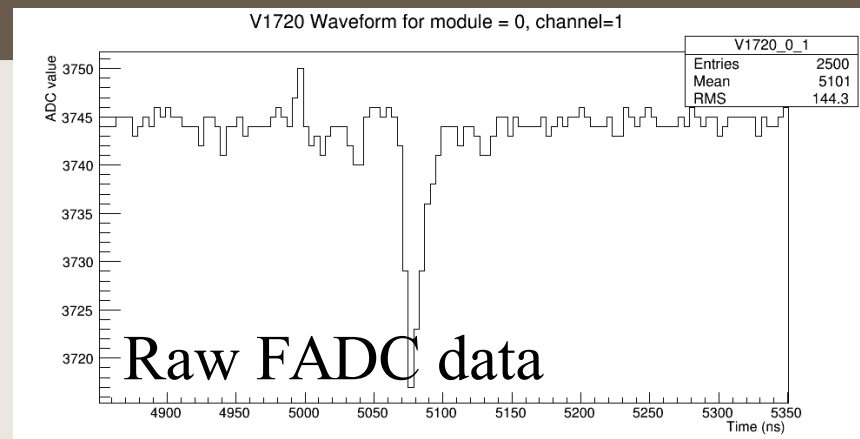
- FADCs instead of TDC/ADC for digitization
- Redundant communication protocol

Schematic diagram of the front-end board



FADC Option - Overview

- Proposal: use FADC (Flash ADC) instead of TDC/ADC.
 - Something like 100-500 MHz sampling, 12-16 bit resolution.
- FADC data is continuously processed using FPGA on front-end board; firmware finds hits and only send pulse summary to backend.
 - Pulse summary is either just Q/T (for small pulses) or a set of ADC samples (for large pulses).



FADC Option - Overview

Current work is focused on these two questions:

1) Can we quantify gains of FADC? What physics does this help?
Starting WCSim studies, but nothing to show yet.

2) Can we meet timing resolution and dynamic range requirements?
(reminder: 0.3ns resolution, 0.05-1250 PE range)

Focus of this talk is tests of timing resolution for different FADC designs.

Pros

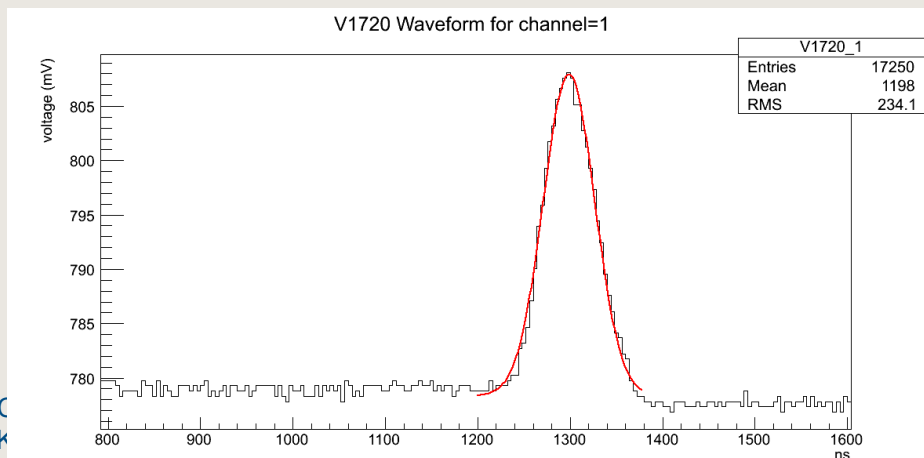
- More information on charge distribution 1us after first pulse.

Cons:

- Higher power (?) and cost (?)
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

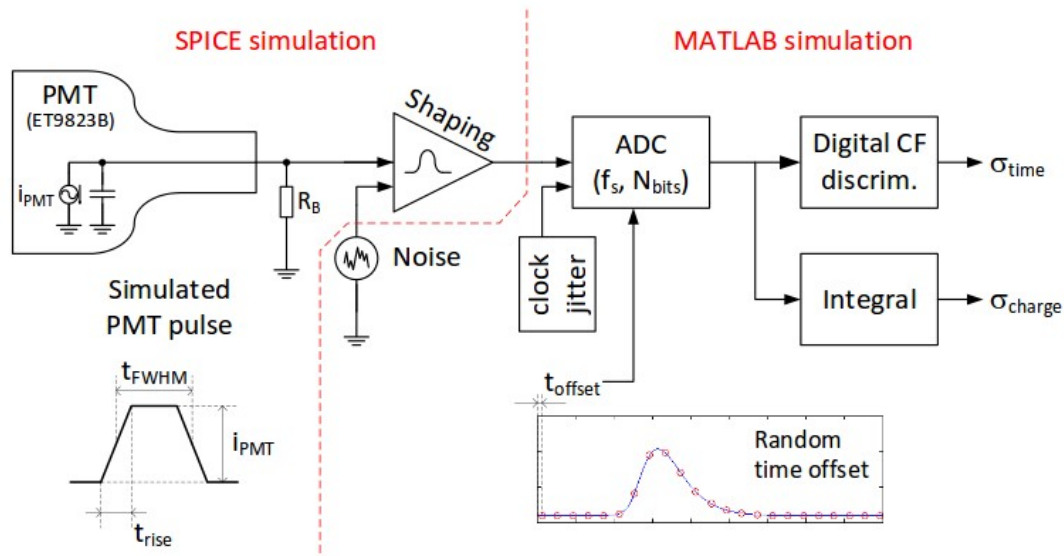
Time Measurements with digital waveform

- Extracting precise time from FADC pulse depends on many factors:
 - Low electronics noise
 - Sufficient number of samples on leading and falling edge.
 - Need to shape pulse if not enough samples
 - Precision of ADC
 - Higher precision ADC (14 bit vs 12 bit) can help, but only if noise is small
 - Frequency of ADC
 - Faster ADC is better (but higher power, more expensive)
- Talk will show ongoing studies of balancing these characteristics.

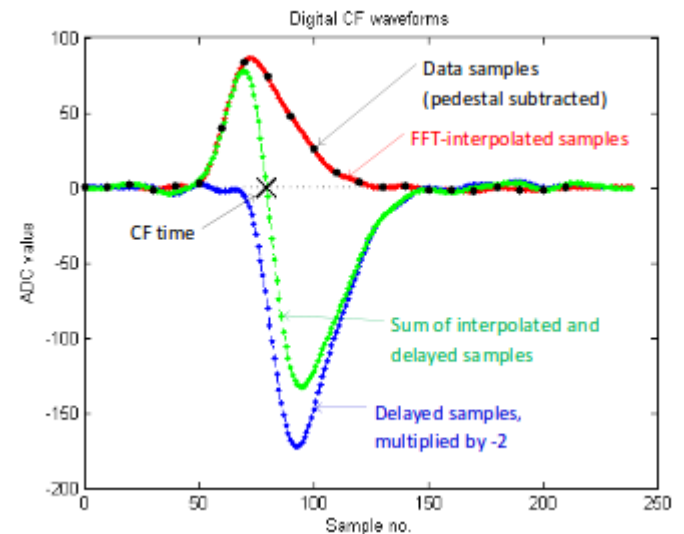


Study of Shaper and Digitizer

- Marcin Ziembicki has done a detailed study of optimal combinations of shaper and digitizer.
- Used combination of SPICE and Matlab to estimate timing and charge resolutions for optimal shapers with different digitizers.

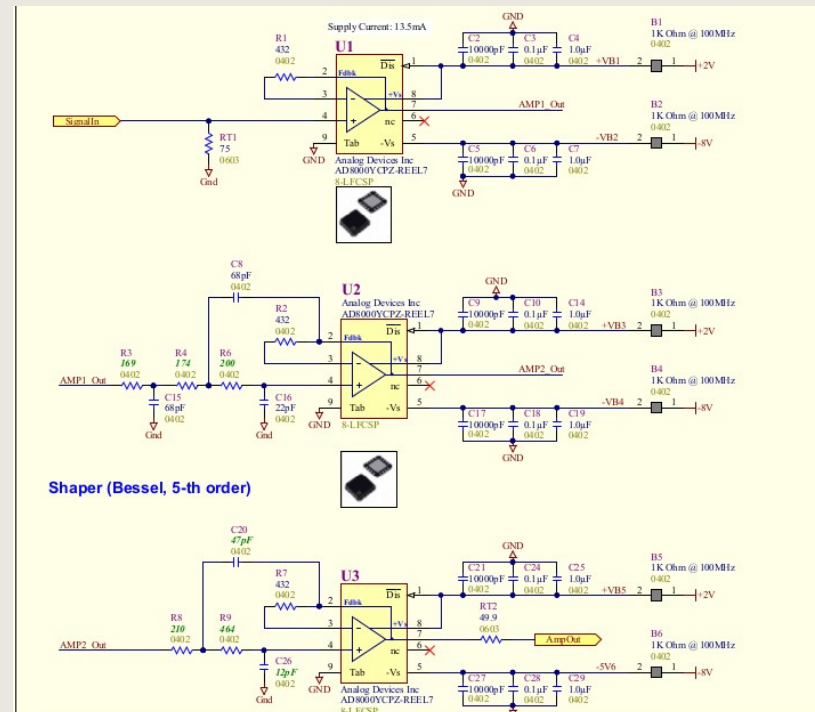
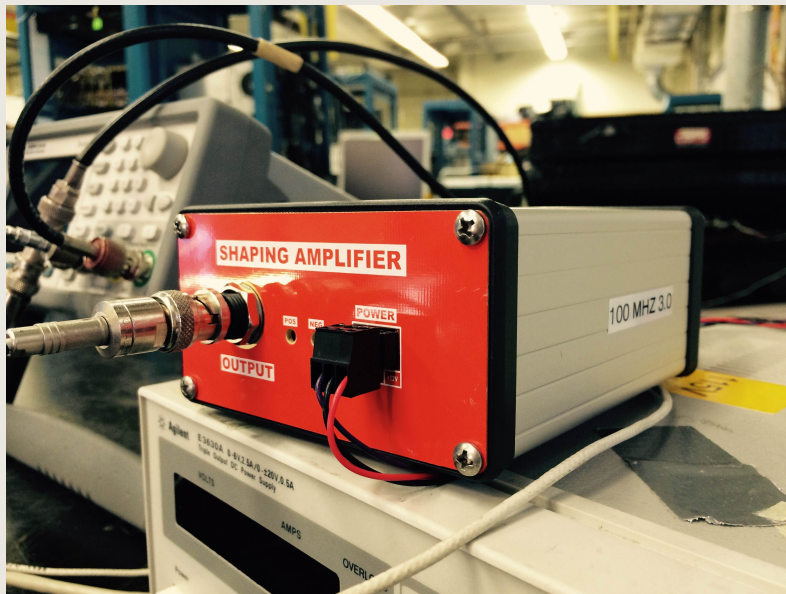


Digital Constant-Fraction



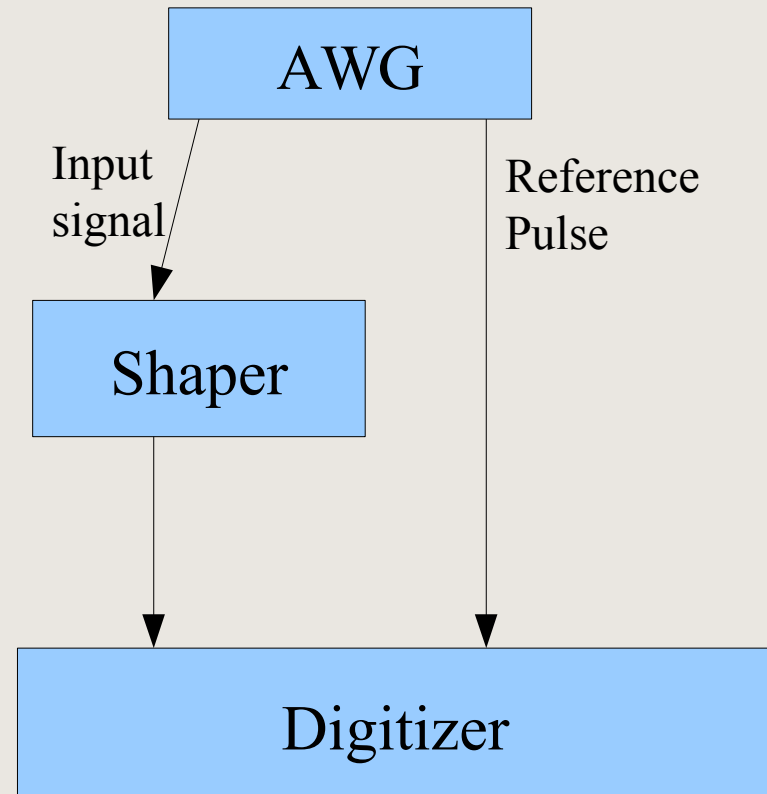
Results of Simulation

- Found various combinations of shaper and ADC that should meet requirements.
- Based on studies we constructed 4 different versions of shaper circuit with different shaping times, so that we can do proper hardware tests.



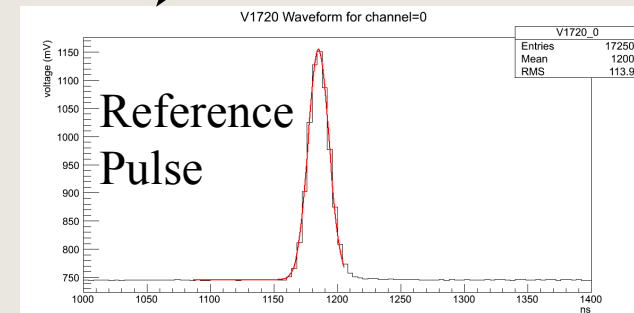
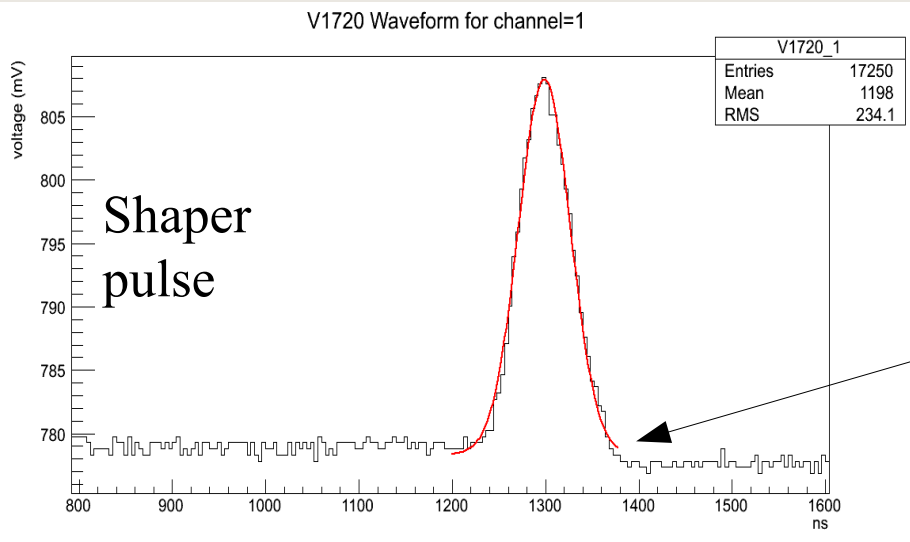
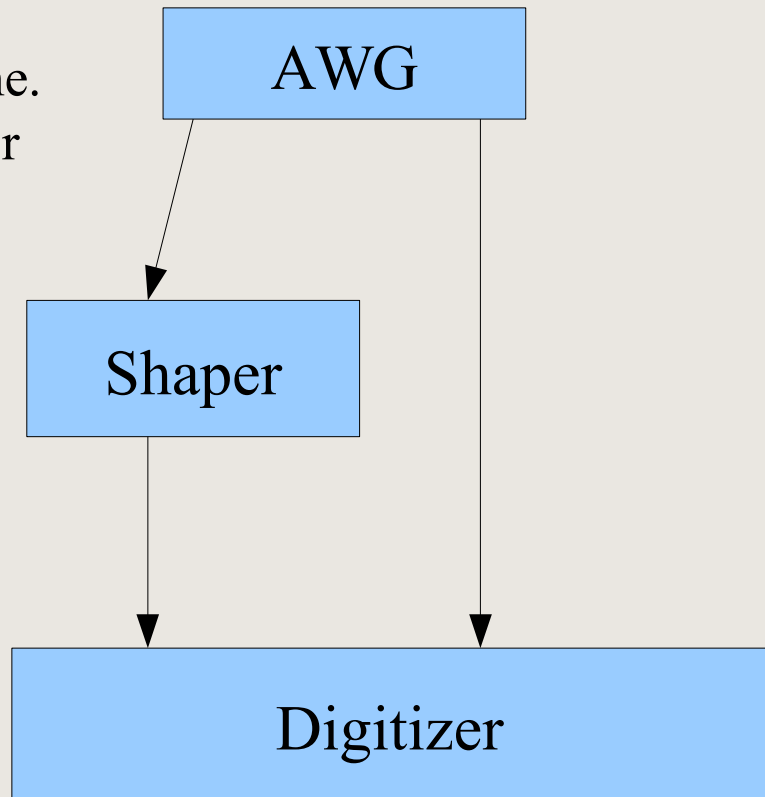
Test Setup

- Use arbitrary waveform generator (AWG) to create input pulses.
 - AWG has no intrinsic pulse jitter (unlike PMTs) so can probe directly the timing resolution of electronics.
- Have on hand 250MHz and 500MHz digitizers; acquiring 100MHz digitizer soon.



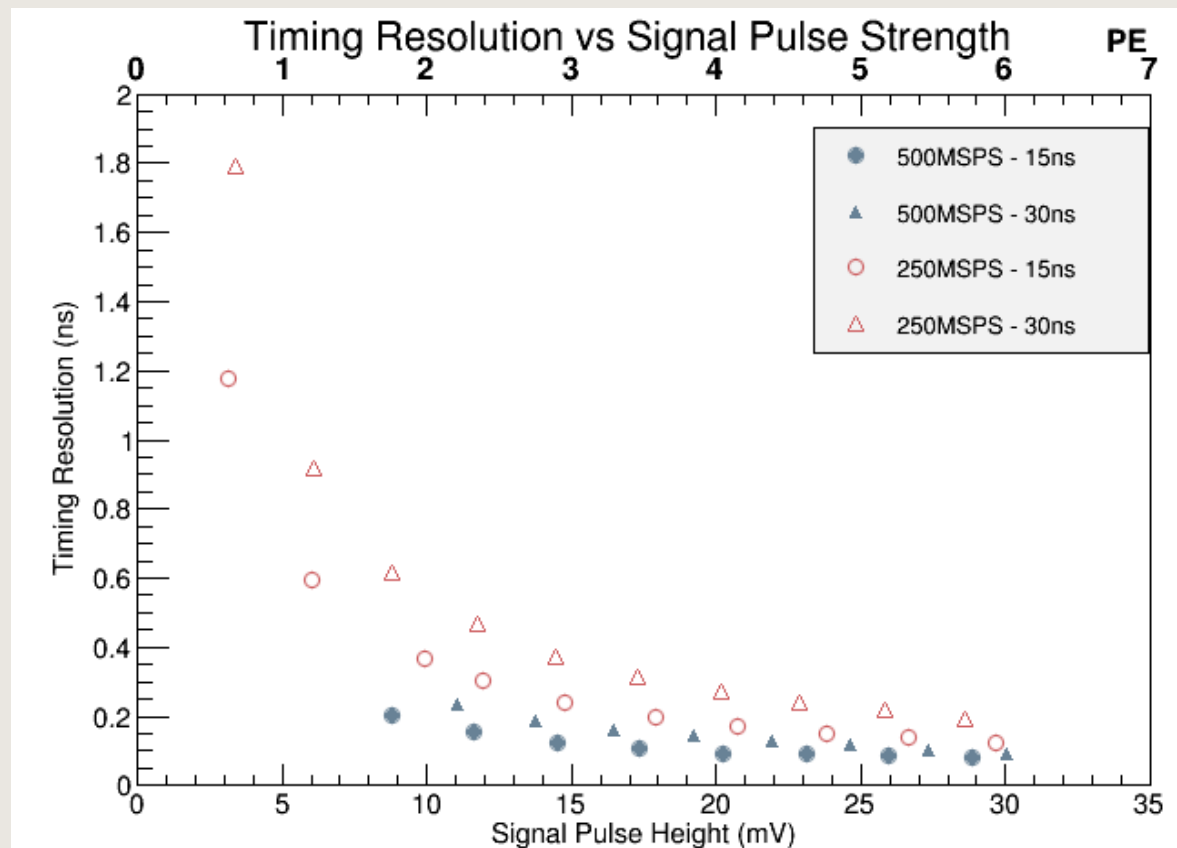
Test Setup Analysis

- Currently fit the pulse to extract pulse time.
 - Eventually want to use digital CFD or matched filter, closer to what can be implemented in FPGA.
- Width of histogram of signal – reference times gives the timing resolution.



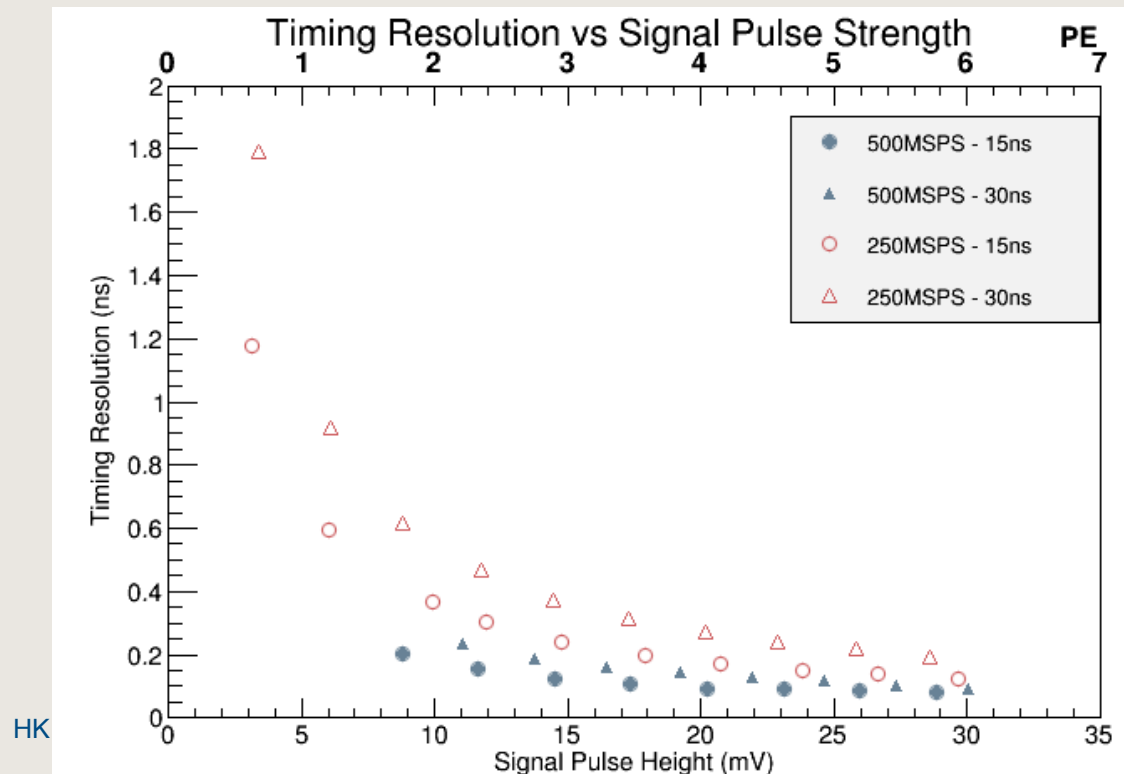
Timing Resolution Results

- Plot shows timing resolution vs signal pulse height for various combinations of shapers and digitizer.
- Results are preliminary; results depend fairly strongly on details of how well fitting is done. This has not been optimized much.



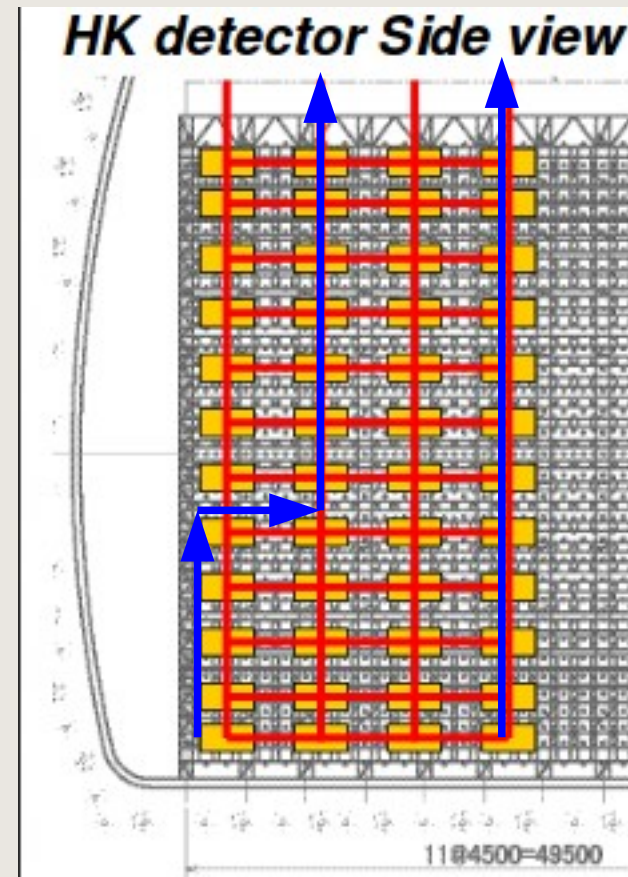
Timing Resolution Results

- For pulses above $\sim 10\text{mV}$ we can meet timing resolution requirements with 250MHz digitizer.
- Can play with PMT gain to make single PE pulses this big, but need to understand implications for dynamic range.
- Ongoing work to compare these results with Marcin's simulation and develop reliable models of electronics.



Communication Work

- Have an ongoing set of UBC engineering students who are working on some tests of a possible communication scheme based on RapidIO protocol.
- RapidIO is alternative to ethernet/TCP-IP protocol.
- RapidIO seems interesting because it allows ways of specifying routing of data packets.
- Could use this functionality to route packets for redundant mesh network.



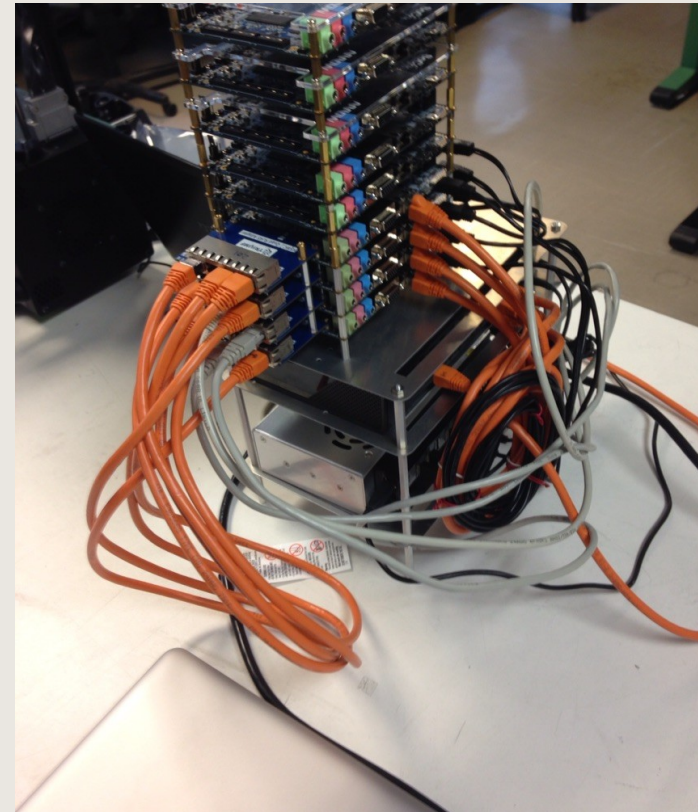
RapidIO Test

- Currently testing of the RapidIO communication using a set of Altera FPGA evaluation boards.
 - Specifically Terasic evaluation board with Altera FPGA (with NIOS CPU) and dual ARM processors.
 - Made custom extension card to allow 5 cat-6 cables to attach to each board.
- Hopefully students will also compare RapidIO to other possible protocols (ie ethernet).



RapidIO Status

- Implemented 4 RapidIO cores in FPGA on each board; each RapidIO core has associated DMA engine.
- Managed to get each of 4 links running at 550Mb/s.
- Testing routing functionality using stack of 9 evaluation cards.
- Have also purchased PC card that supports RapidIO transfer (*Starbridge PCIe to sRIO card, based on TSI 721*)



Future Plans

- Summer 2015: finalize decision about digitizer frequency for prototype.
- Summer 2015: start design of digitizer card.
- Fall 2015: fabricate and test prototype digitizer card.
- 2016: do production of digitizer cards for HK prototype.

Quick Thoughts on Alternate Tank Designs

- With straight vertical walls of alternate tank design, I assume that PMT frame becomes cheaper and stronger.
- Perhaps it becomes possible to support the weight of having cable from top of tank to each PMT. So could have digitizing electronics outside water (like SK).
 - Would be very long signal cables for PMTs at bottom of tank (~200m?); check signal degradation.
 - But significant benefits in terms of risk management: fixing/replacing/upgrading electronics becomes simple. Also, power dissipation no longer an issue.
- If we stick with underwater electronics, perhaps possible to have communication cable to each front end card, instead of mesh network.

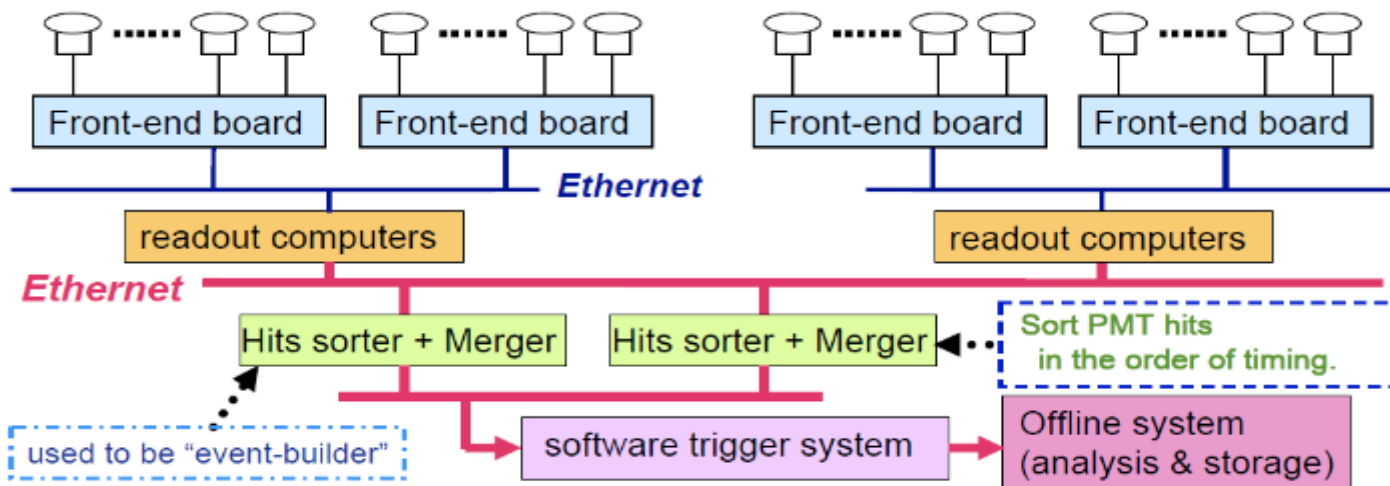
Conclusions

- Working on understanding which digitizer can be used to meet timing resolution requirements.
 - Based on Marcin's studies have fabricated set of shaper circuits.
 - Have done initial tests of achievable timing resolution; lots more work to be done.
- Ongoing work on testing RapidIO as communication protocol.

Backups

Hyper-K Electronics/DAQ

Current schematic diagram of the HK DAQ system



- 1) Signals from the photo sensor above discriminator threshold are continuously digitized.
- 2) All the "digitized" hit information including dark noise are sent to the readout computers.
- 3) Define events using the software trigger and send them to the offline system and also store the events in the disk.

No global hardware triggers; all PMT hits stream up to PCs where trigger decisions are made.

Hayato-san, previous HK meetings

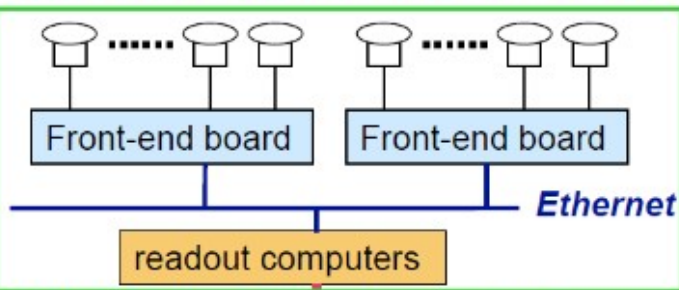
Hyper-K Communication Scheme

Possible front-end electronics module connections

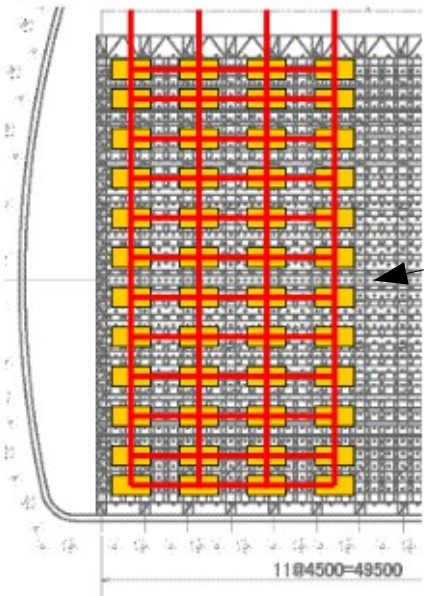
~ Design of the data flow

1) Assuming to use 1GbE

- Robustness
- Power consumption



HK detector Side view



2) Connect neighboring Front-end boards each other

- Reduce total length of the cables
- Avoid single point failure

Usually, data collected by a module are transferred to the upper module (vertically)

If a module failed, transfer data to the other module instead of the failed module (horizontally).

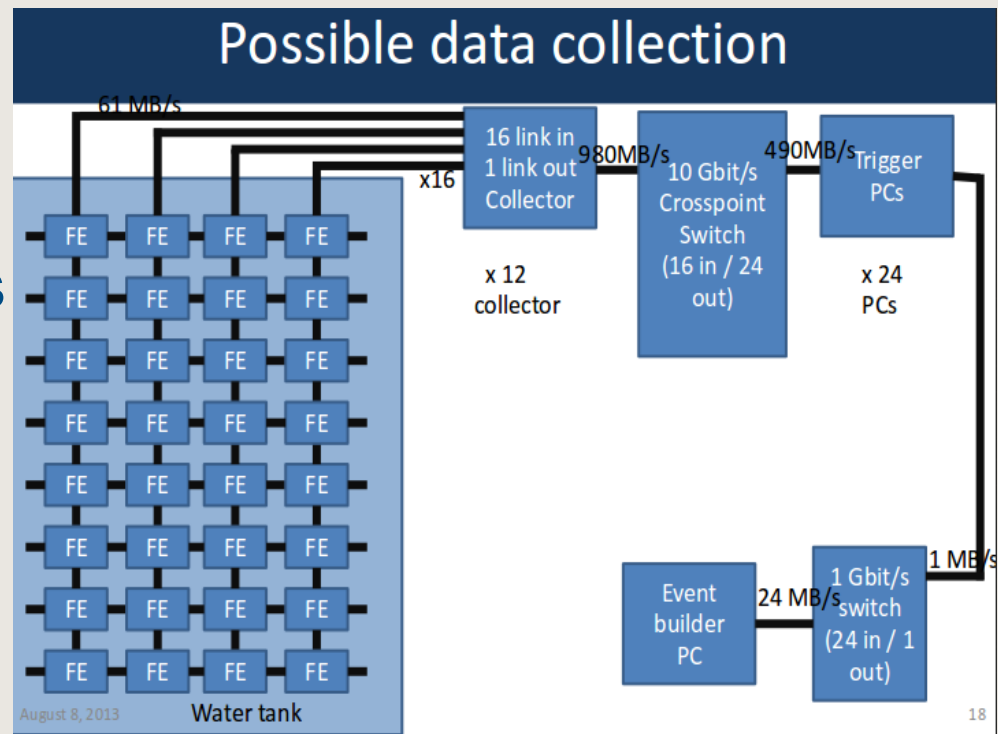
Data rate at the top modules has to be enough smaller than 1Gb/sec.

Electronics sit in water:
Redundant communication needed.

Hayato-san, previous HK meetings

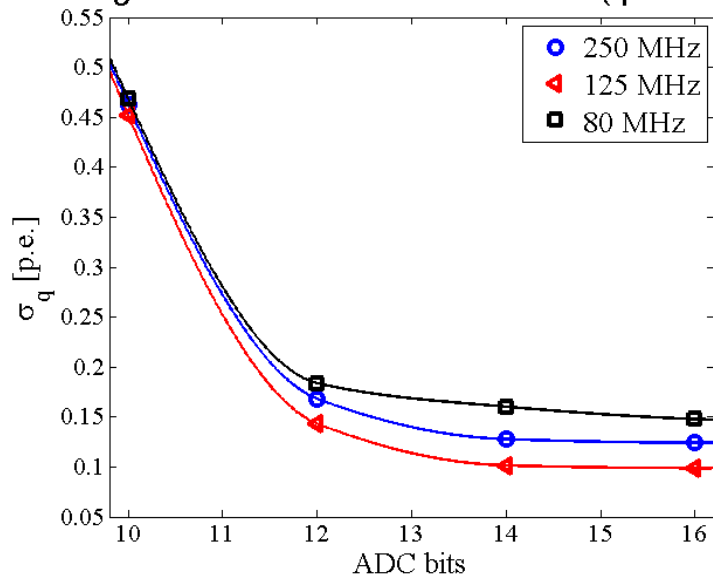
Back-end Architecture

- Possible back-end architecture.
- Data from front-end electronics get time-sliced and sent to different PCs.
- PCs make trigger decisions and decide if event(s) get logged to disk.
- Maximum 12GB/s for rate is dominated by dark noise.

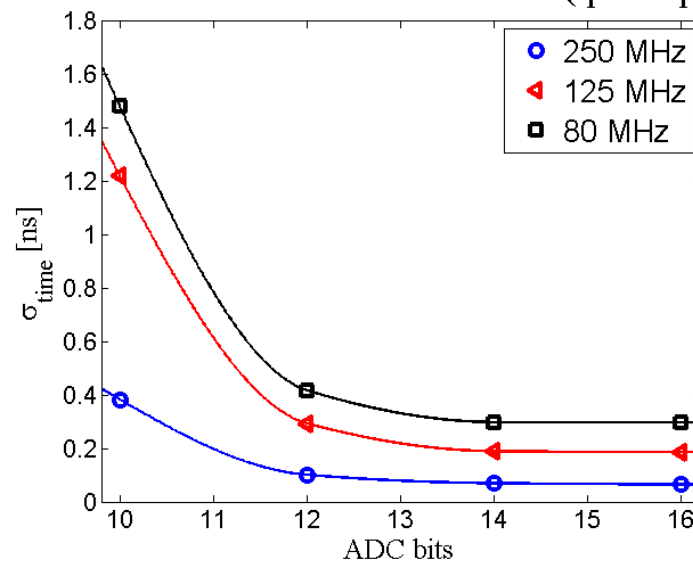


Marcin's Simulation Results

Charge resolution vs ADC resolution ($q = 10$ p.e.)



Time resolution vs ADC resolution ($q = 10$ p.e.)



Digitizers

- Currently using set of different commercial CAEN digitizers



V1730
500MSPS



V1720
250MSPS



DT5724 100MSPS

Timing Test Analysis

- Histogram difference between fitted signal and reference times.
- Width is timing resolution.

