# DAQ

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# Procedure to design a DAQ system

- ✓ Characteristics of ( analog ) signal from the photo sensor

- ✓ Requirements from physics
  - ➢ Charge resolution
  - ➢ Charge dynamic range
  - ➢ Timing resolution
  - ➢ Allowed dead time etc…

- ✓ Number of photo sensors

  ➡ Possible combinations of

  1. Digitization technology
  2. Communication ( bus ) technology
  3. Sizes of intermediate buffers

  Another constraints

  Power consumption

  Size of the circuit boards ( form factor )

# Procedure to design the “HK DAQ system”

✓ Characteristics of ( analog ) signal from the photo sensor

*HPD? or PMT?*

✓ Requirements from physics

- ➢ Charge resolution
- ➢ Charge dynamic range
- ➢ Timing resolution
- ➢ Allowed dead time etc…

→ Signal digitization ~ possible options

- **QTC + TDC**

  ~ similar to SK

- **FADC** ( with shaper )

***R&D ~ Evaluation of the performance has been started.***

# Procedure to design the “HK DAQ system”

- ✓ Number of photo sensors

  *10k ~ 20k / unit detector ( compartment )*

- ✓ Another constraints
  - ***Electronics modules have to be located under the water?***

    ***Water tight chassis***

    ***Signal connection method under the water***

    ***( Water tight connectors )***
  - ***Electronics outside of water : Long cable ( up to ~ 150m )***

    ***Signal degradation***

    ***Cabling route and method***

    ***( Signal connection method under the water )***
  - ***Timing synchronization***

    ***Reference clock & counter distributions***
  - ***Stability ( “re-initialization” or “reset” is not allowed***

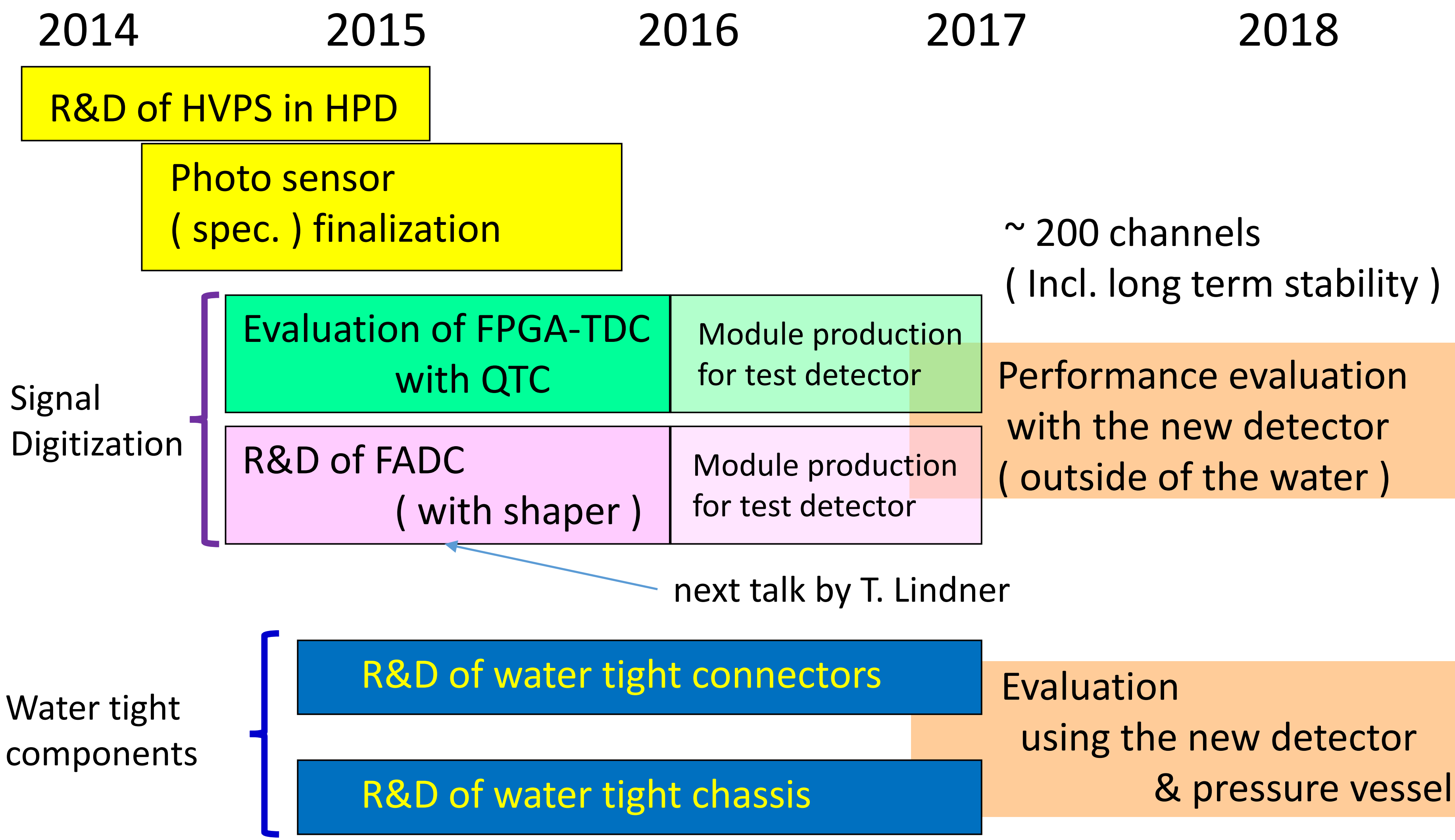
    ***for a week ~ months )***
  - ***Cost***

# Procedure to design the "HK DAQ system"

1) Evaluation of the digitization methods
    1) FADC ( 100 ~ 250 MHz ) + shaper
    2) QTC ( developed for SK QBEE )
    + FPGA based TDC ( used in g-2 experiment )

    Check
        timing and charge resolution
        charge dynamic range
    and
        evaluate feasibility including cost estimation.
2) Evaluate communication methods ( data transfer )
    SiTCP ( standard TCP/IP protocol )
    Rapid IO
3) Study reference clock & counter distribution methods
4) Evaluate water tight chassis
5) R&D of water tight connections ( incl. cables and connectors )

# Procedure to design the “HK DAQ system”

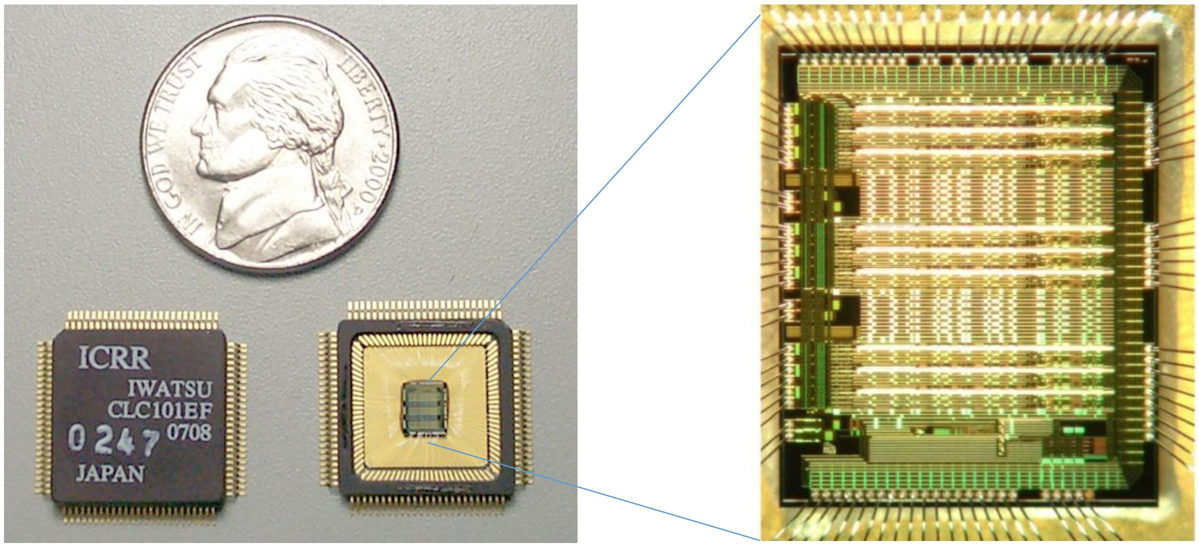


# R&D status of QTC + FPGA based TDC option

Availability of QTC chips

QTC (CLC101EF) : Charge to time converter ASIC

custom ASIC by ICRR & Iwatsu




We have spare chips for SK : Borrow them for R&D.

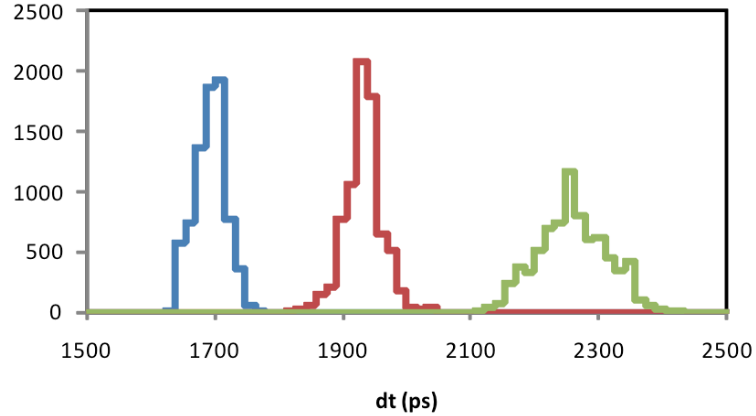
Process rule : 0.35 μm ( CMOS )

→ Expected to be available for several years from now.
There seems to exist industrial demands of this process.
( If the process rule is changed, need to re-design. )

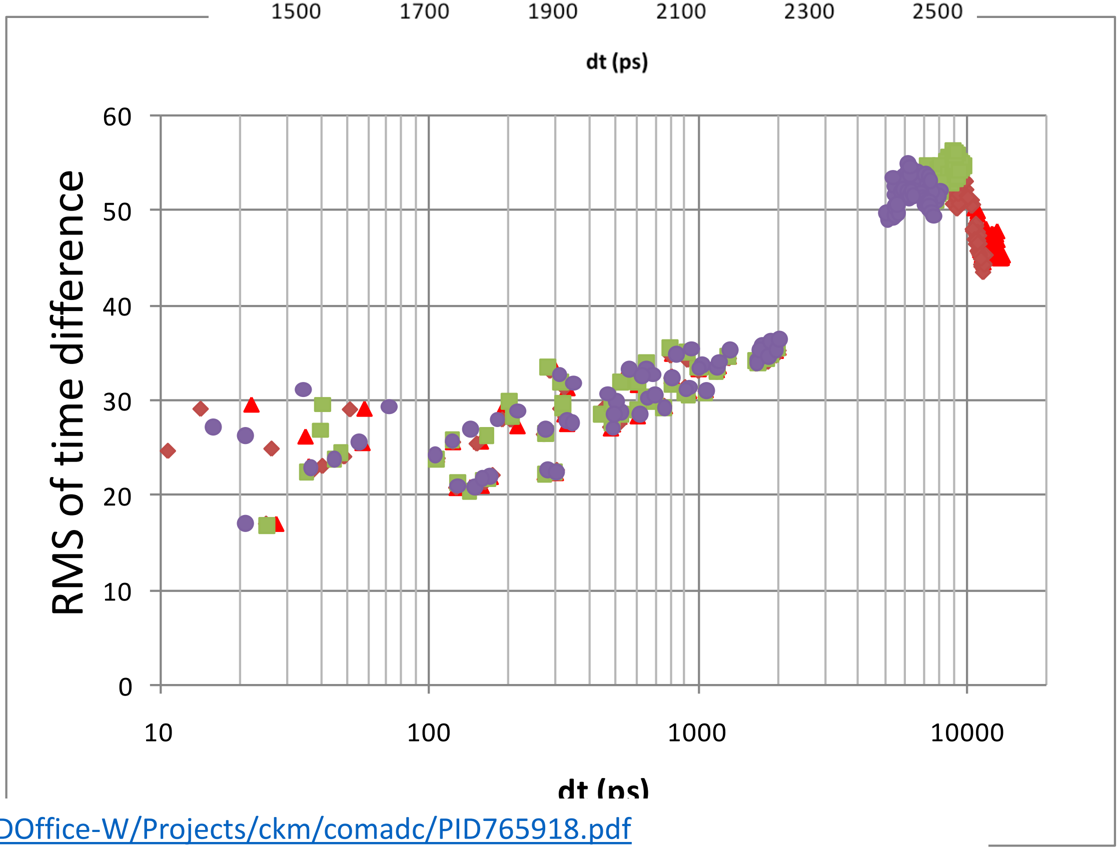
→ Possible re-production of the same chip.

# R&D status of QTC + FPGA based TDC option

Results of FPGA-based TDC
“Wave Union”
by Jin-Yuan Wu, Fermilab




sub-ns
RMS




http://www-ppd.fnal.gov/EEDOffice-W/Projects/ckm/comadc/PID765918.pdf

http://www-ppd.fnal.gov/EEDOffice-W/Projects/ckm/comadc/LowPowerWUTDC_paper11c.pdf

Ed Kearns ( BU )

# R&D status of QTC + FPGA based TDC option

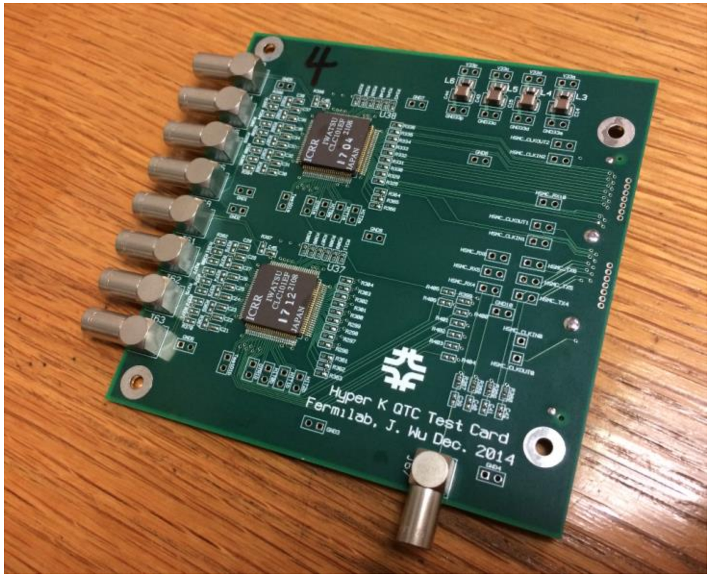
## Hyper-K Electronics R&D with U.S.-Japan Program

Direct upgrade path from current SK electronics “QBEE”

- QTC chip by Iwatsu (ADC)
- ~~TDC chip by KEK~~ ⇒ FPGA-based TDC by Fermilab
- 10 Mb/s Ethernet readout by Boston ⇒ upgrade to 100 Mb/s or Gb

Prototype circuit designed to test integration and performance of ADC and TDC

- delivered 1/16/2015


Altera Cyclone III FPGA Starter Kit + Custom circuit with QTC

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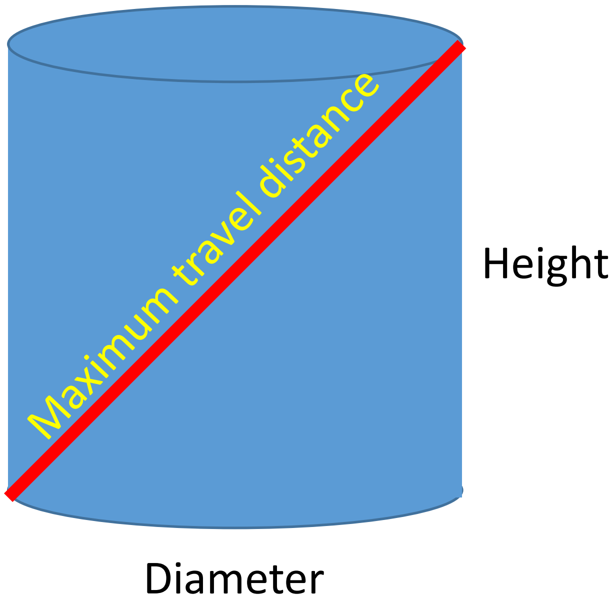
# Procedure to design the "HK DAQ system"
## ~ *Impact of new detector designs* ~

Large detector ~ longer trigger window & event window




Gate width ~ 4 * $\sqrt{(\text{Height})^2+(\text{Diameter})^2}$ (ns)

For Super-Kamiokande,
trigger window ~ 200ns.

For Hyper-Kamiokande ( new designs )
trigger window ~ 400 ~ 500 ns.

***Why width of trigger / event window matters?***

Trigger efficiency, fake event rate
Energy resolution
Vertex resolution

***Effect of ( dark ) noise may be non-negligible***

# Procedure to design the "HK DAQ system"

## ~ *Impact of new detector designs* ~


Example : SK

| | |
|---|---|
| # of sensors | 12 k |
| Noise ( dark ) rate | 4 kHz |
| Window | 200ns |

→ ***12k (PMTs) * 4kHz * 200ns ~ 10 hits***

1MeV corresponds to ~ 6 hits for SK ( 40% coverage )

Current lowest threshold in SK ( SLE trigger ) ~ 34 hits

34 hits ~ 10 ( dark hits ) + 24 hits ( signal )

24 hits / sqrt ( 10 ) ~ 7.6

***Much higher than noise fluctuations***

24hits ~ 6 ( hits / MeV ) * 4 ( MeV )

# Procedure to design the "HK DAQ system"

## ~ *Impact of new detector designs* ~


Assumption : HK

| | |
|---|---|
| # of sensors | **15 k** |
| Noise ( dark ) rate | **10 kHz** |
| Window | **500ns** |

→ ***15k (sensors) * 10kHz * 500ns ~ 75 hits***

1MeV corresponds to ~ ***3 hits*** for ***20% coverage equivalent***

Assuming ***8MeV*** threshold

75 hits ( noise ) + ***24 hits ( signal )*** = ***99 hits***

***24 hits / sqrt(75) = 2.7***

- May exist fake events from noise.
- For energy reconstruction,
  window could be 10 ~ 50ns ( after TOF subtraction ).
  But noise hits may affect resolutions.

# Procedure to design the "HK DAQ system"

## *~ Impact of new detector designs ~*

Amount of data from the detector ( before applying trigger )

Assumption : HK

| | |
|---|---|
| # of sensors | **15 k** |
| Noise ( dark ) rate | **10 kHz** |

→ ***15k (sensors) * 10kHz***

***~ 0.15 Ghits / sec / detector***

***~ 2.4 GBytes / sec / detector***

# of hits from μ :

100 Hz ( ***worst*** case ) * 15k ( sensors )

→ ***~ 0.015 Ghits / sec / detector***

***~ 0.24 GBytes / sec / detector***

***~ 10 times smaller than dark noise hits***