

nuPRISM Electronics

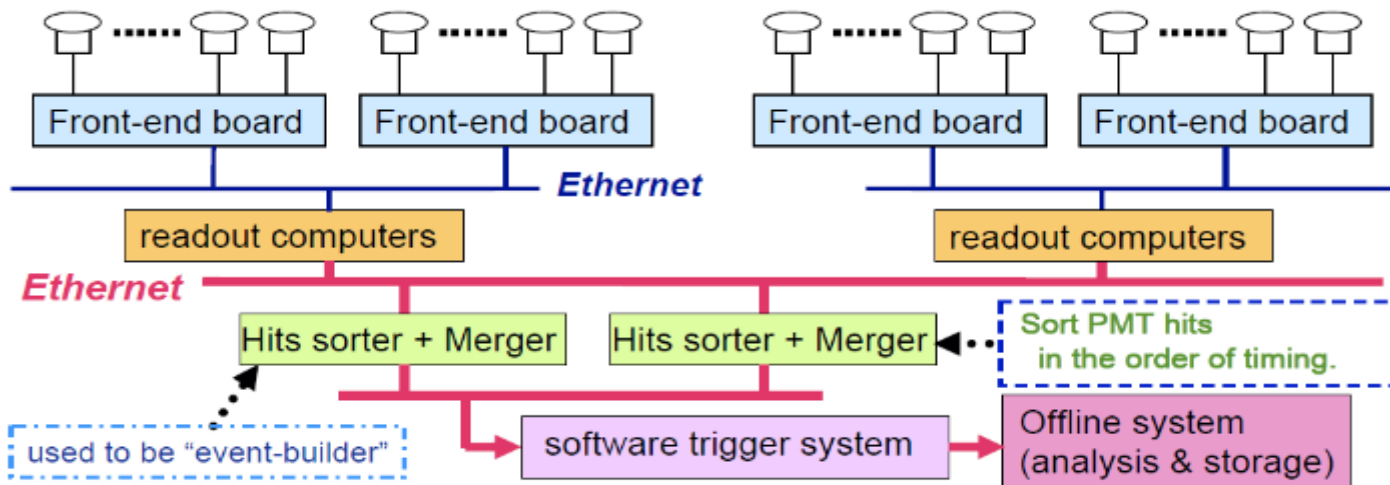
Thomas Lindner | TRIUMF
NuPRISM Meeting, March 2014

NuPRISM Electronics: Baseline Plan

- Baseline plan would be to make the nuPRISM electronics as similar as possible to HK electronics. Features of electronics:
 - Front-end electronics, including digitization and high voltage, underwater, as close to PMTs as possible.
 - FADC digitization (our suggested option).
- Using similar electronics maximizes benefit of nuPRISM as HK prototype.

Reminder: Hyper-K Electronics/DAQ

Current schematic diagram of the HK DAQ system



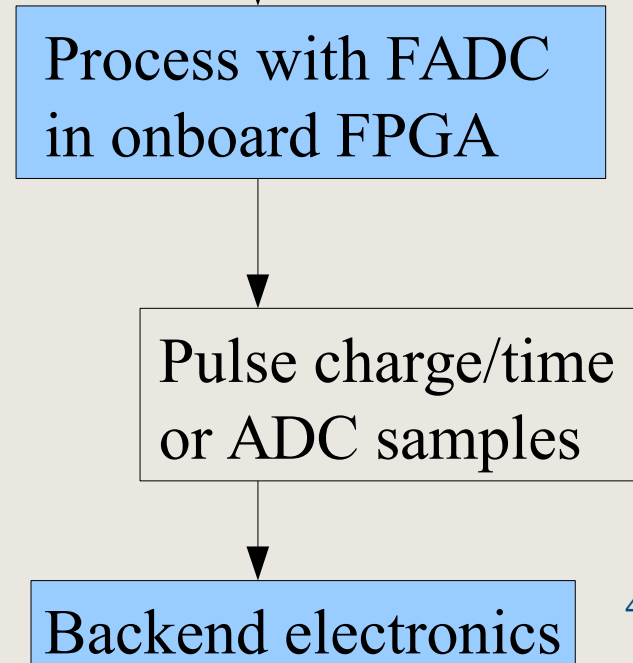
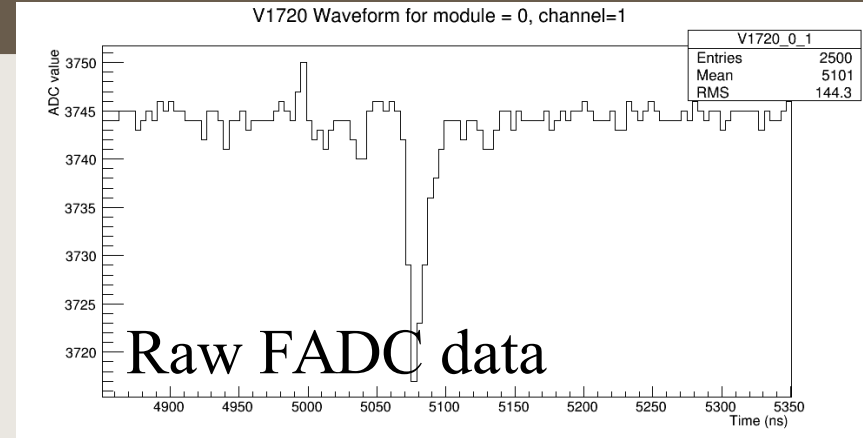
- 1) Signals from the photo sensor above discriminator threshold are continuously digitized.
- 2) All the “digitized” hit information including dark noise are sent to the readout computers.
- 3) Define events using the software trigger and send them to the offline system and also store the events in the disk.

No global hardware triggers; all PMT hits stream up to PCs where trigger decisions are made.

Hayato-san, previous HK meetings

FADC Digitization - Overview

- Proposal is to use FADC (Flash ADC) instead of TDC/ADC.
 - Something like 125-500 MHz sampling, 12-16 bit resolution.
- FADC data is continuously processed using FPGA on front-end board; firmware finds hits and only send pulse summary to backend.
 - Pulse summary is either just Q/T (for small pulses) or a set of ADC samples (for large pulses).



FADC Option - Overview

Current work is focused on these two questions:

1) Can we quantify gains of FADC? What physics does this help?
Starting WCSim studies, but nothing to show yet.

2) Can we meet timing resolution and dynamic range requirements?
 (reminder: 0.3ns resolution, 0.05-1250 PE range)
Focus of this talk is tests of timing resolution for different FADC designs.

Pros

- More information on charge distribution 1us after first pulse.

Cons:

- Higher power (?) and cost (?)
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

FADC Benefits for nuPRISM

What benefits do you get from more detailed/dead-timeless FADC digitization?

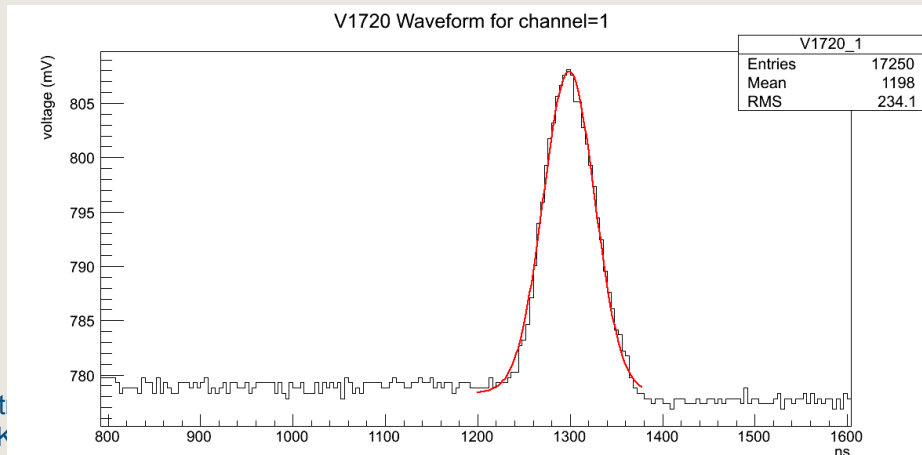
For nuPRISM there will be a large number of events in each beam spill. Having the maximum amount of information about the time profile of each channel (with no dead-time!) will be very critical, particularly if we try to reconstruct multiple events in a single beam bunch.

Muon and
decay electron
as seen in
ND280-FGD.

Time Measurements with digital waveform

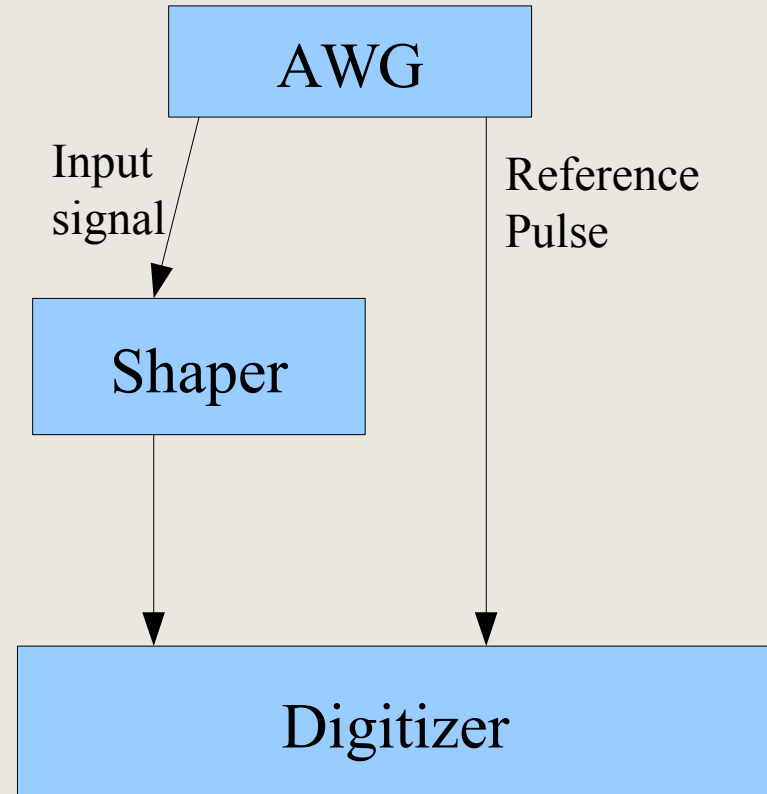
- Extracting precise time from FADC pulse depends on many factors:
 - Low electronics noise
 - Sufficient number of samples on leading and falling edge.
 - Need to shape pulse if not enough samples
 - Precision of ADC
 - Higher precision ADC (14 bit vs 12 bit) can help, but only if noise is small
 - Frequency of ADC
 - Faster ADC is better (but higher power, more expensive)

- Talk will show ongoing studies of balancing these characteristics using set of shapers from Marcin (next talk) and TRIUMF digitizers.



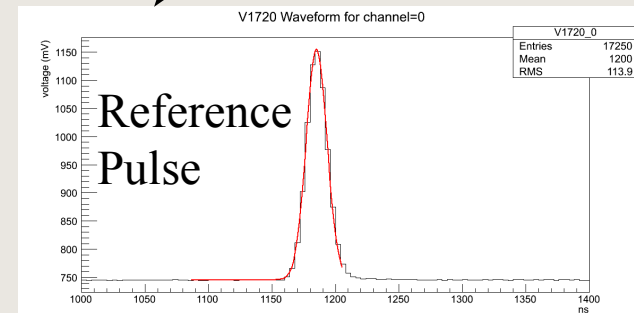
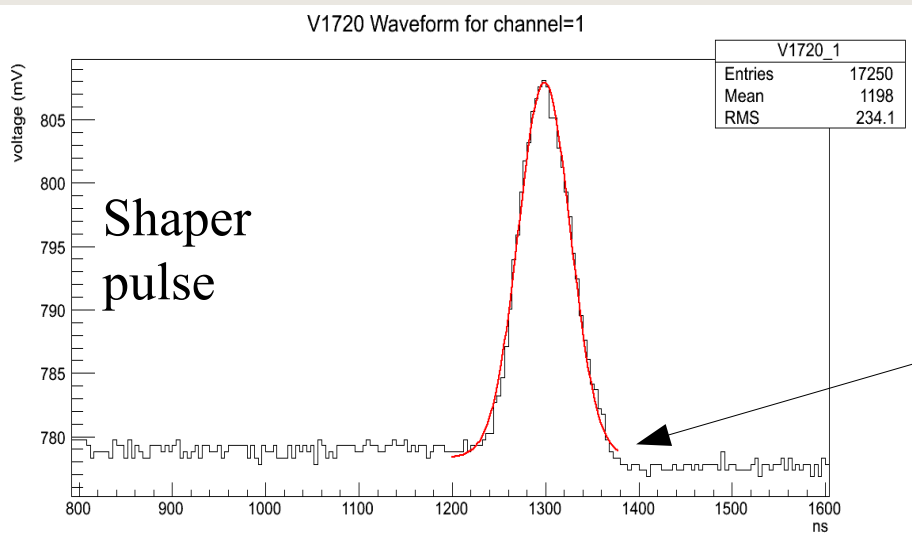
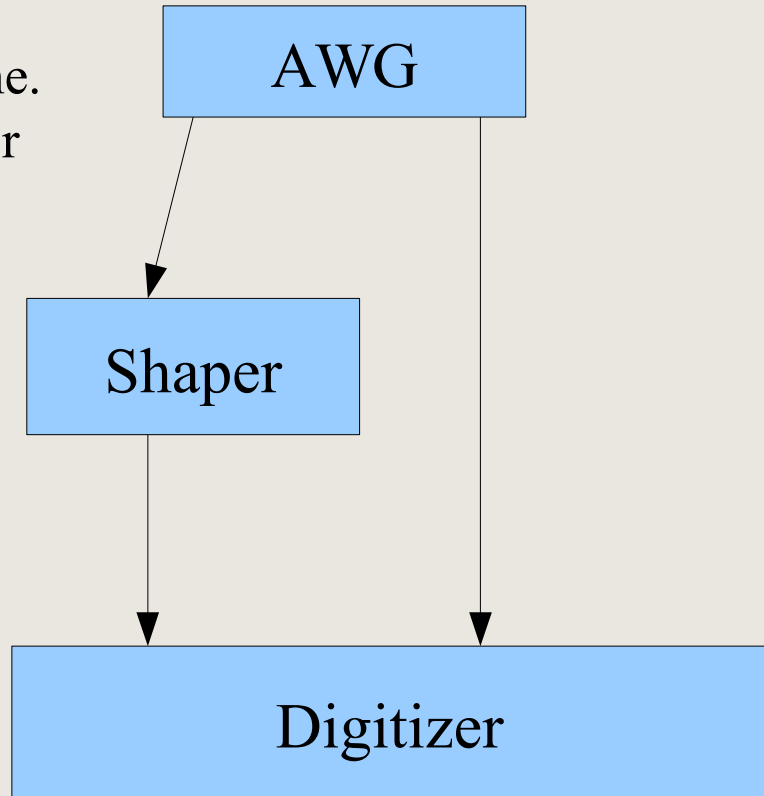
Test Setup

- Use arbitrary waveform generator (AWG) to create input pulses.
 - AWG has no intrinsic pulse jitter (unlike PMTs) so can probe directly the timing resolution of electronics.
- Have on hand 100MHz, 250MHz and 500MHz digitizers.



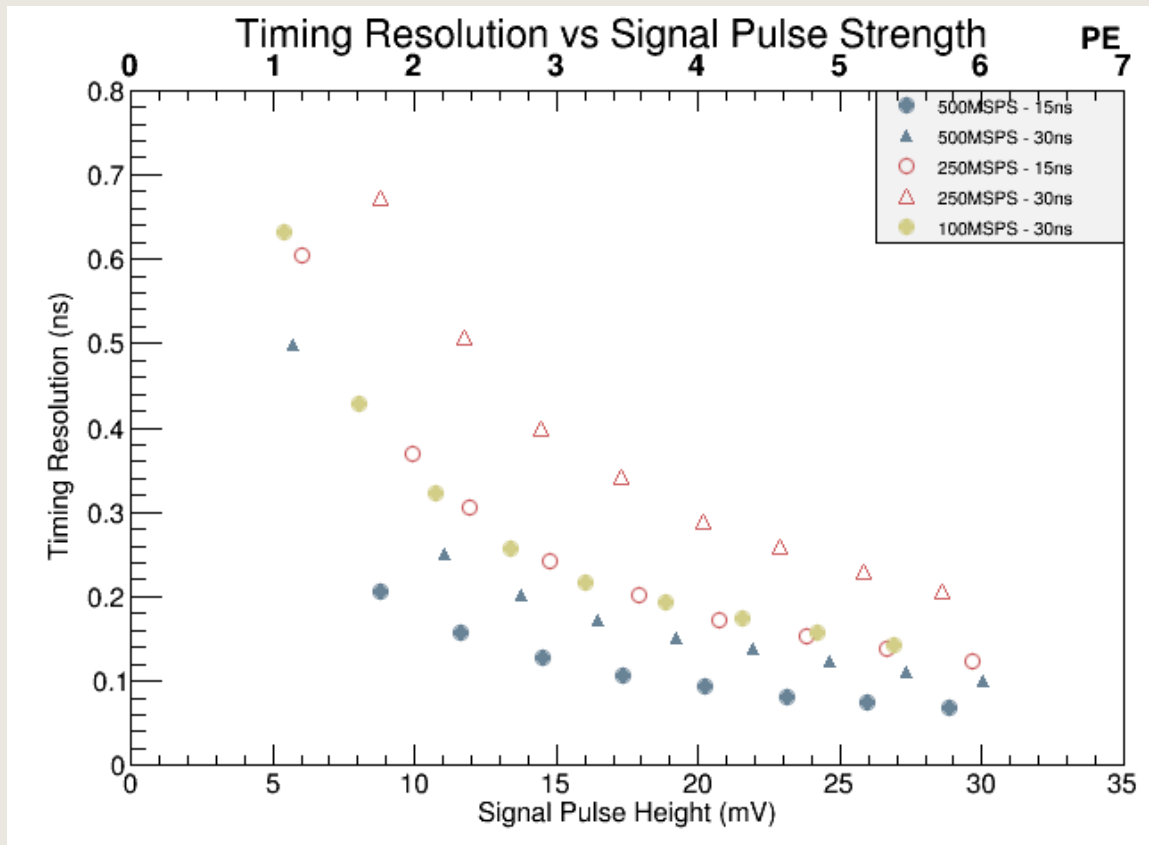
Test Setup Analysis

- Currently fit the pulse to extract pulse time.
 - Eventually want to use digital CFD or matched filter, closer to what can be implemented in FPGA.
- Width of histogram of signal – reference times gives the timing resolution.



Timing Resolution Results

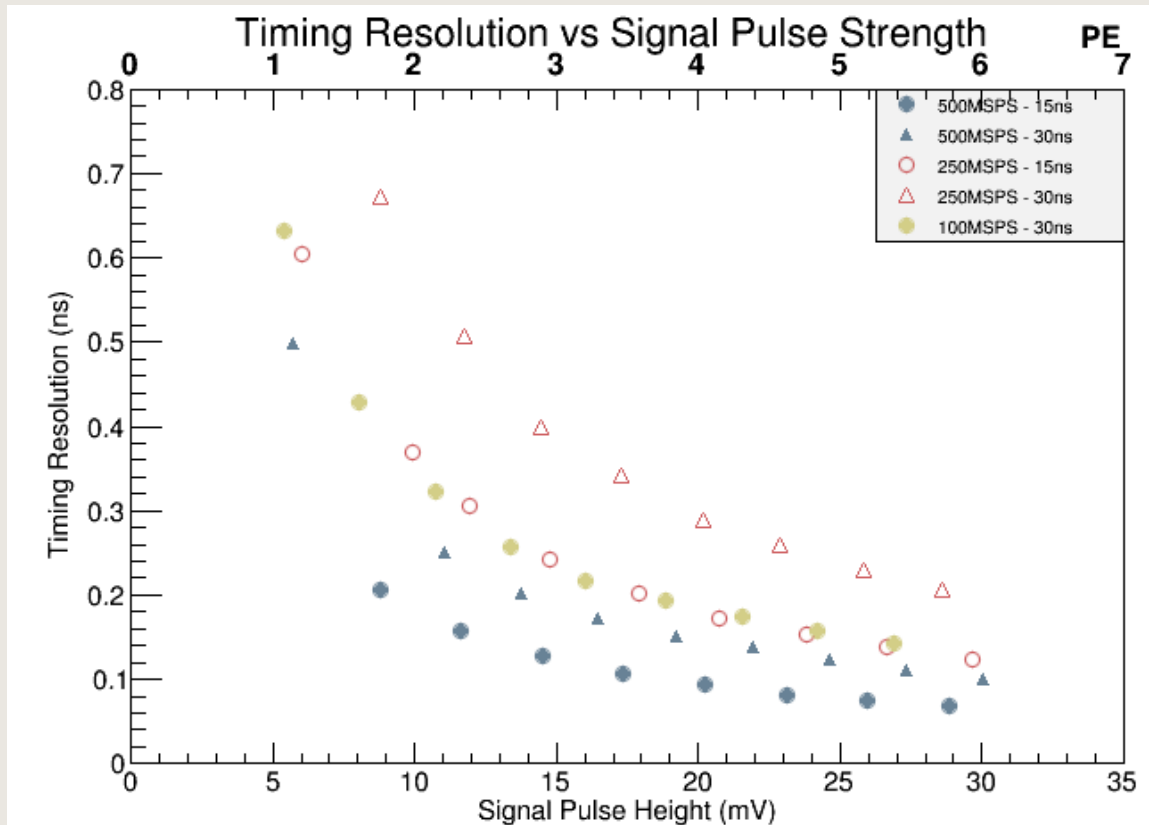
- Plot shows timing resolution vs signal pulse height for various combinations of shapers and digitizer.
- Results depend fairly strongly on details of how well fitting is done. This has not been fully optimized.



Timing Resolution Results

- Results with 100MHz, 14bit digitizer are very promising. Get pretty good timing resolution of 0.6ns at 5mV.*
 - 100MHz digitizer had lower intrinsic noise than other digitizers.
- With 1PE at 5mV height would get ~0-400PE dynamic range (digitizer uses ADC with 2V range).

* Mike got quotes on R5912 8" PMT, which has intrinsic time jitter of ~1.0ns for 1PE pulse. So ~0.6ns jitter from electronics is ok, though not ideal

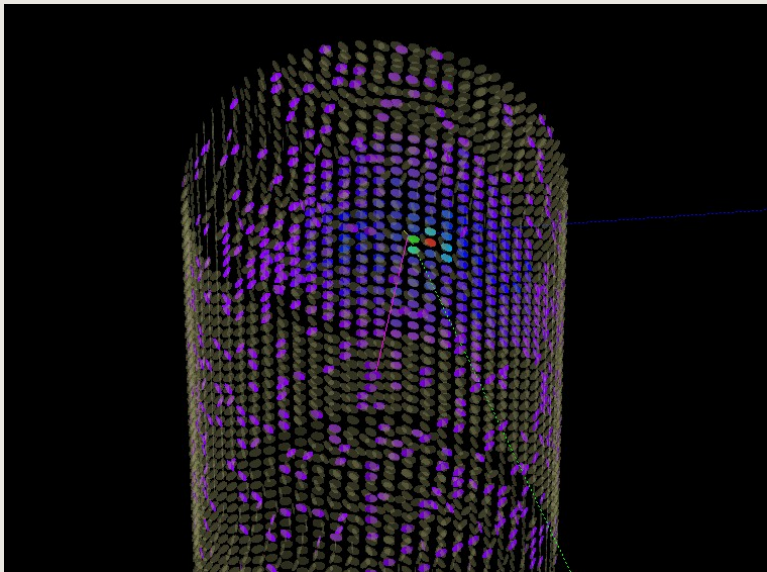


Dynamic Range Study

- Default goal is to achieve same dynamic range as HK electronics: 0-1250PE.
- But is that necessary?
- Did a crude test with nuPRISM WCSim from 2 weeks ago
- Did simulations with muons/electrons of various energy; check distributions of number of PEs in channels.
- Many caveats:
 - No neutrino interactions with multiple rings. Multiple rings would increase chance of high charge in a particular PMT.
 - Used default 8inch PMT in WCSim, not HQE PMTs. So expect higher QE and hence more PEs.

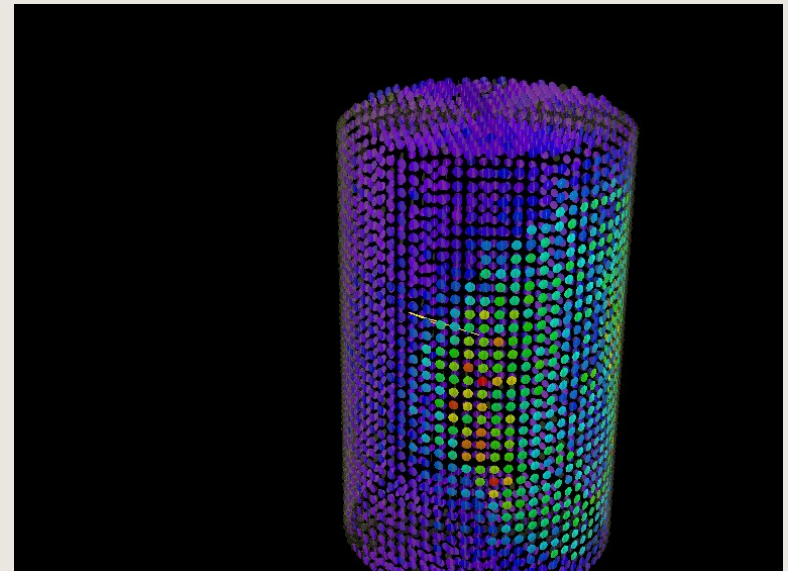
Muons/Electrons

- Simulated muons and electrons starting from various points in tank. Manually tuned muon starting point + energy to get particles that just stopped within ID.



0.7GeV muon

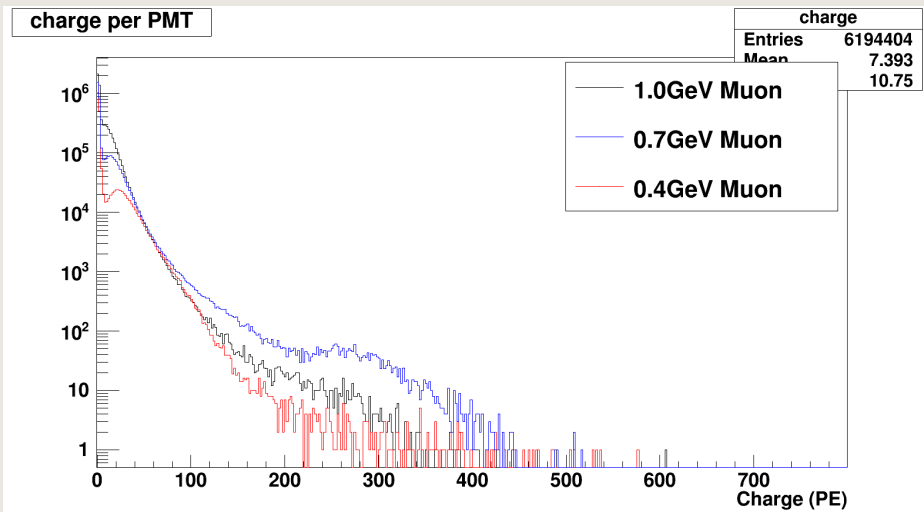
Muons ususally seemed to have highest charge at center of filled in ring.



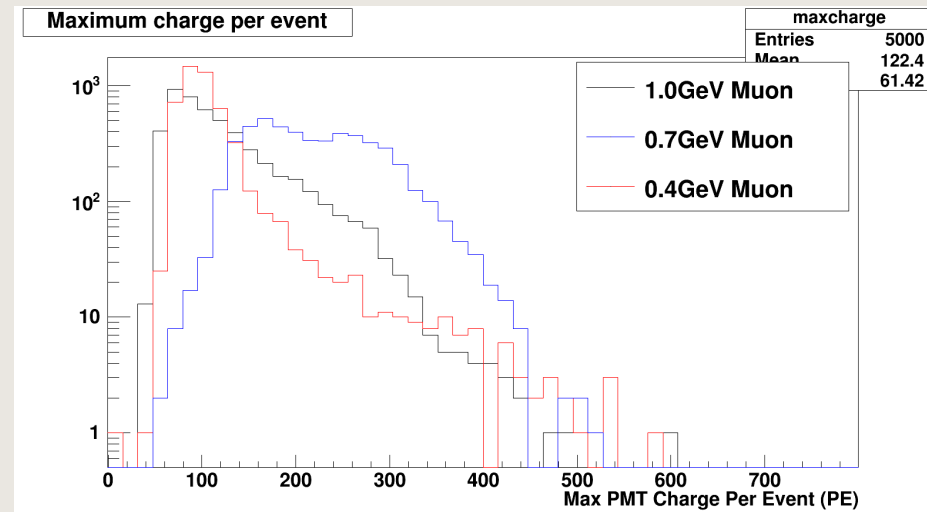
5GeV electron

PE distributions - Muons

- Maximum PE for muons doesn't seem to depend strongly on energy.
- Quite rare to have any hits above 400PE.



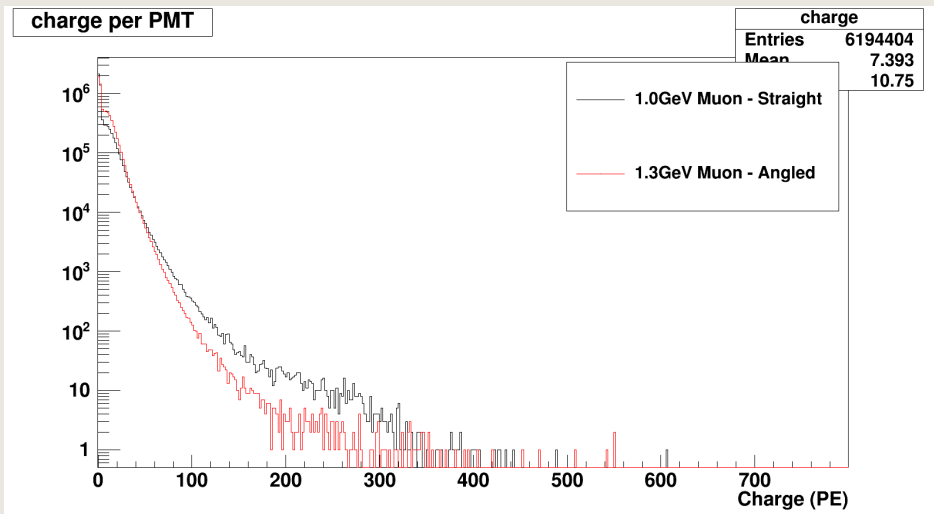
Charge for each PMT in each event



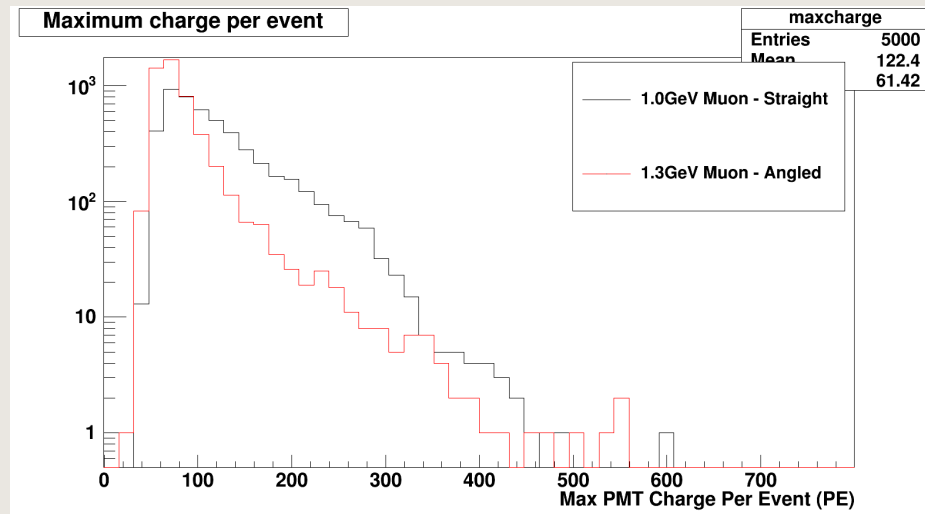
Charge for largest PMT hit in each event

PE distributions – Angled Muons

- Similar results for angled muons



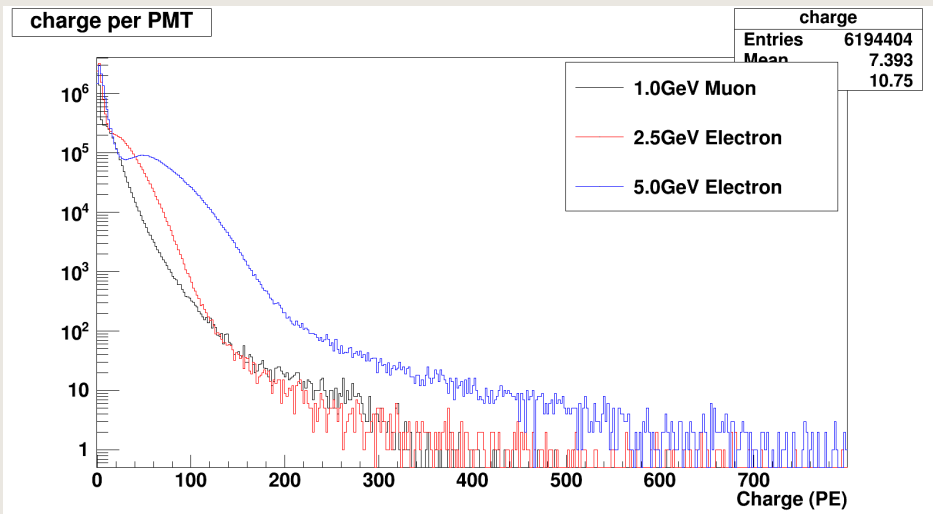
Charge for each PMT in each event



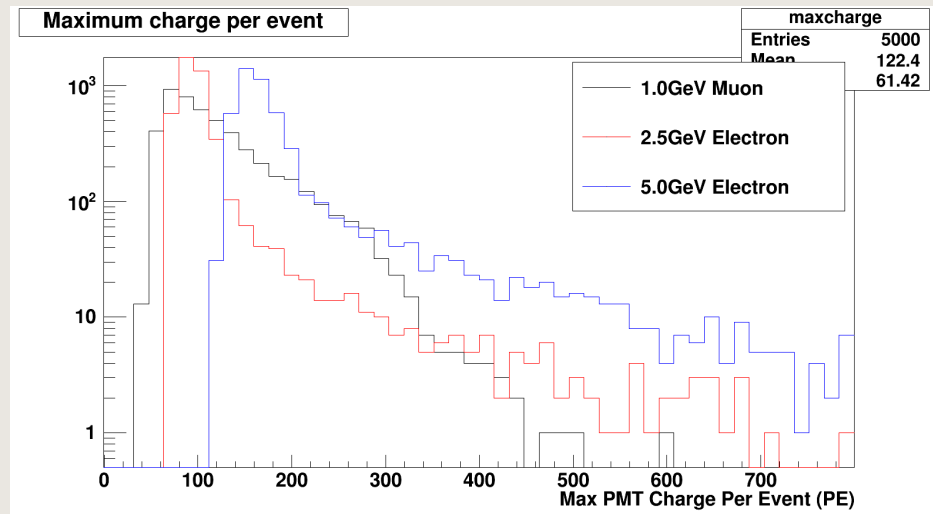
Charge for largest PMT hit in each event

PE distributions – Electrons

- For the electrons we have more of a problem. 5GeV electrons can push up to pretty high charge.



Charge for each PMT in each event



Charge for largest PMT hit in each event

Dynamic Range Summary

- Some first results on dynamic range suggest we might be able to lower dynamic range.
- Need to understand effect of
 - How much higher QE and multi-ring
 - How high do we want to go with electrons
- Also, saturating a couple hits might not matter much for overall energy reconstruction. Try rerunning fitqun with charge saturation at 500PE.

Open Questions for Proposal

- Haven't thought much more about the question of in-water or out-water electronics.
 - If out-of-water, do we need a realistic design for how to manage cables? And of how to deal with extra weight of cables?

Conclusions

- Working on understanding which digitizer can be used to meet timing resolution requirements.
 - Based on Marcin's studies have fabricated set of shaper circuits.
 - Have done initial tests of achievable timing resolution; lots more work to be done.
- Started studies on dynamic range requirements. May be able to loosen requirements.

Backups

NuPRISM FADC Data rate

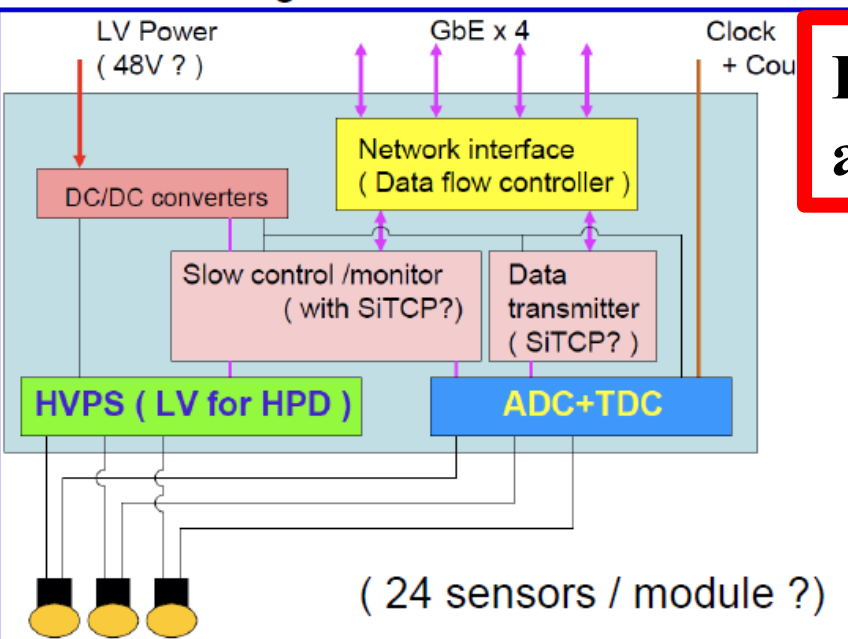
- For HK the data rate from FADC is dominated by data from PMT dark noise.
- How about data rate per channel for nuPRISM?
 - Dark noise: $10\text{kHz} * 12 \text{ byte/hit} = \mathbf{120\text{kB/s}}$
 - Spill hits: $8\text{bunch} * 20\% \text{ hit} * 50 \text{ byte/hit} * 0.5\text{Hz} = \mathbf{40\text{B/s}}$
 - Save 30 samples per hit $\sim 50\text{byte/hit}$ (large pulses)
 - Assuming 20% of channels are hit in each bunch (for on-axis configuration).
 - Cosmics: $21000 \text{ Hz} * 20\% \text{ hit} * 50 \text{ bytes} = \mathbf{210\text{kB/s}}$
 - PDG says $70 \text{ muons} / (\text{s} * \text{m}^2 * \text{sr})$ ($>1\text{GeV}$ muons).
 - 21000 cosmic muons / s through nuPRISM.
 - Data rate might be dominated by cosmics; need more study.

HyperK:

Baseline Front-end Digitization

- Baseline signal digitization: TDC + ADC (like SK).
- One potential concern: the TDCs used for SK electronics are no longer available; need to find new ones.
 - Possible chips being investigated.

Schematic diagram of the front-end board



QTC/ADC specification (performance)

For NuPRISM, use FADC as alternative to ADC/TDC.

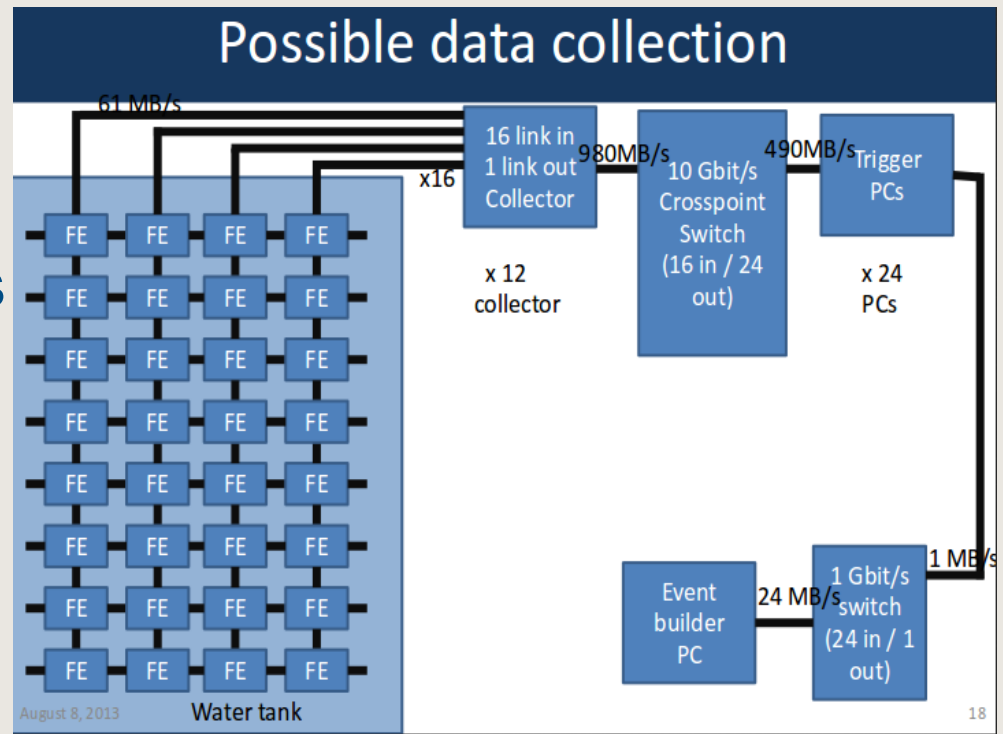
- **Charge Dynamic Range** 0.2~2500pC (0.1 ~ 1250 p.e.)
- **Timing Respons** 0.3ns RMS (@ 1p.e.)
0.2ns RMS (> 5p.e.)

TDC specification (performance)

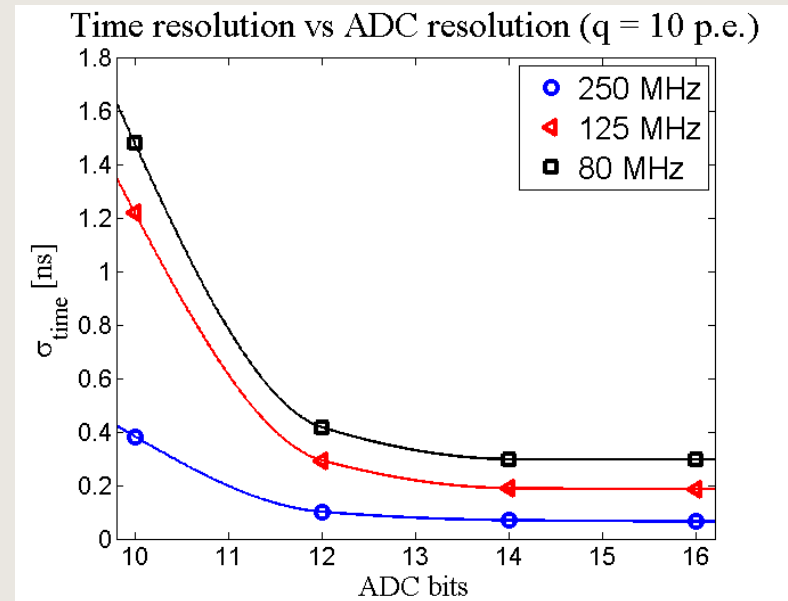
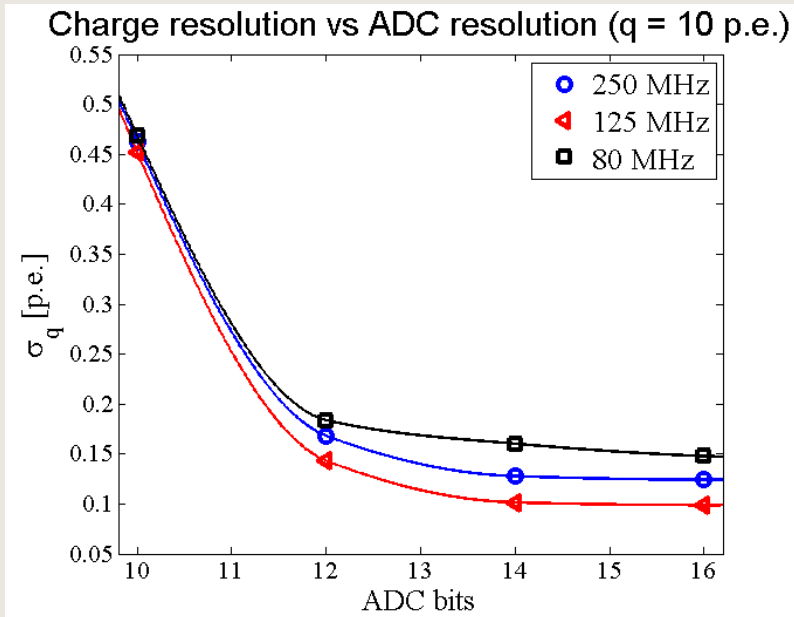
- **Least Time Count** 0.52 ns
- **Time resolution** 250ps
- **Dynamic range** ≥15bits
- **Continuous running mode**

Back-end Architecture

- Possible back-end architecture.
- Data from front-end electronics get time-sliced and sent to different PCs.
- PCs make trigger decisions and decide if event(s) get logged to disk.
- Maximum 12GB/s for rate is dominated by dark noise.



Marcin's Simulation Results



Digitizers

- Currently using set of different commercial CAEN digitizers



V1730
500MSPS



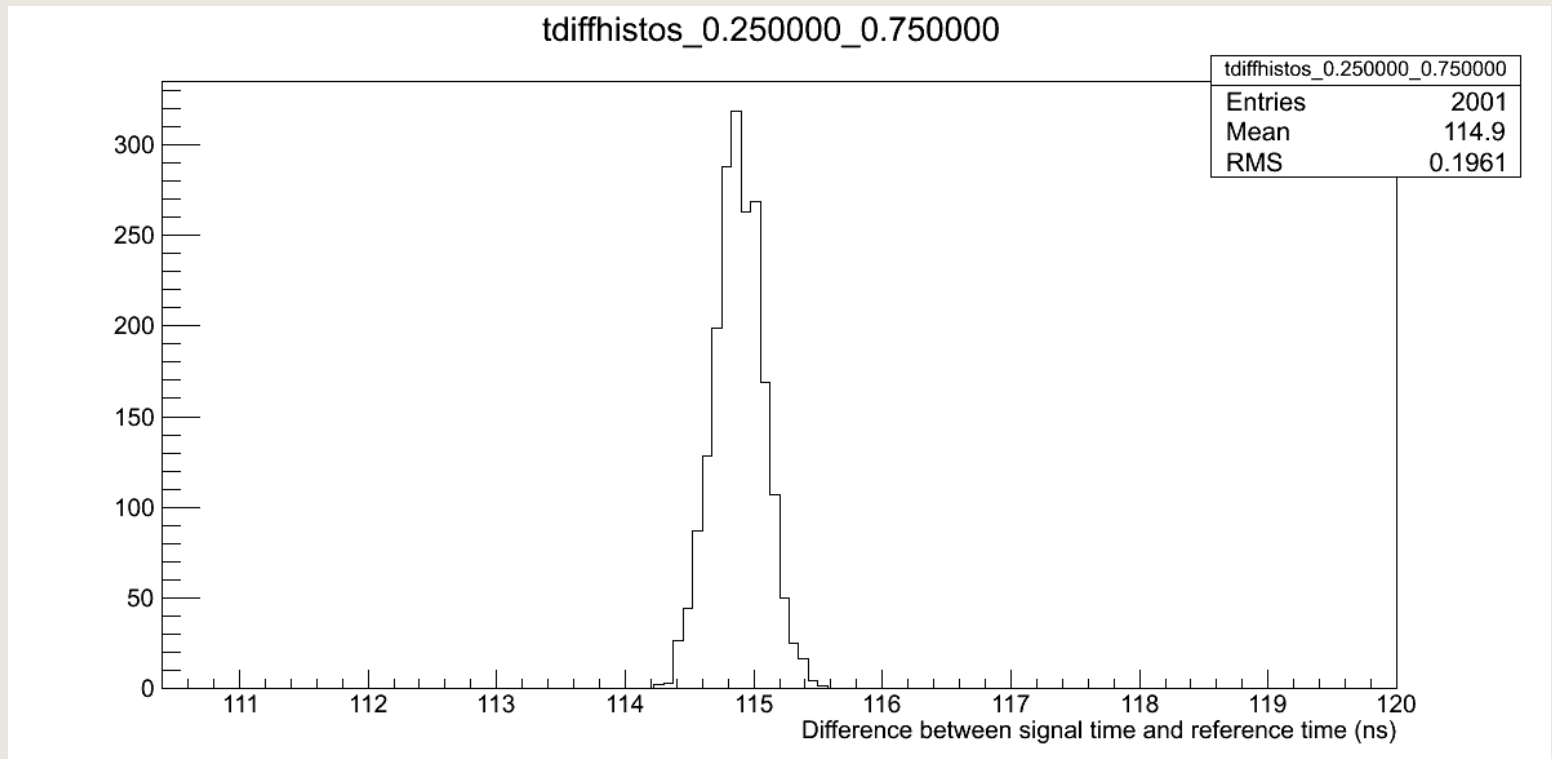
V1720
250MSPS



DT5724 100MSPS

Timing Test Analysis

- Histogram difference between fitted signal and reference times.
- Width is timing resolution.



Budget Estimate (assuming 3000 channels)

- FADC board (16 ch): quantity = 220, cost per board = \$1000, total = \$220,000.
 - Custom board for FGD (made at TRIUMF) was \$700, for 64 channel board.
 - Doesn't include cost for development, that will be covered separately.
- High voltage: Don't directly have any estimates of the cost for high voltage on front-end cards.
 - For 2km it seems they had \$75/channel (\$225k total), but I don't know different that would be for in water high voltage.
 - Hayato-san estimated \$100/channel (\$300k total) in early HK meeting.
- Surface electronics: we estimated this at \$84/channel, \$250k total.
 - This is based on custom electronics cards at surface; could probably get away with something simpler with PCs.
- Total : \$770k. Other estimates are higher, near \$1.3M.