McGill Digital Frequency Multiplexed (DfMux) Readout

LiteBIRD Warm Readout Electronics

2015-12 B-mode from Space Workshop

Development Team

- McGill team: A. Bender (now Argonne), J-F Cliche, A. Gilbert, T. de Haan (now UCB), J. Montgomery, G. Smecher (now Urthecast)
- COM DEV: N. Rowlands, K. Smith, A. Wilson

- *With strong collaboration from: UC Berkeley, U. Chicago, LBNL, NIST, Stanford, Wisconsin.*
- See: **A. Bender** *et al.,* "Digital frequency domain multiplexing readout electronics for the next generation of millimeter telescopes", **SPIE 2014 arXiv:1407.3161.**

fMUX: Heritage & Staged Development

AC-bias,
Scalable System
MUX Demonstration

Full
Multiplexer

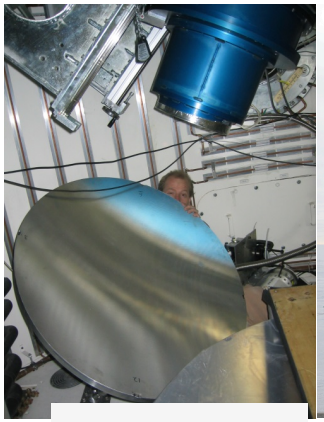
2nd Generation
Digital

Low Power,
Flight Worthy

64x, Lower Power

Satellite

APEX-SZ
320 TES, 2006
Analog fMux



(LBNL/UCB)

South Pole Telescope
1000 TES, 2007
Analog fMux

(LBNL/UCB)

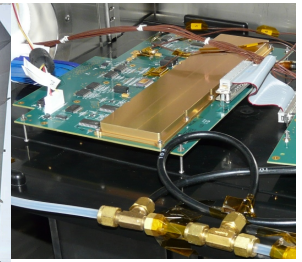
POLARBEAR
1274 TES, 2012

SPTpol
2000 TES,
2012/01
Digital fMux

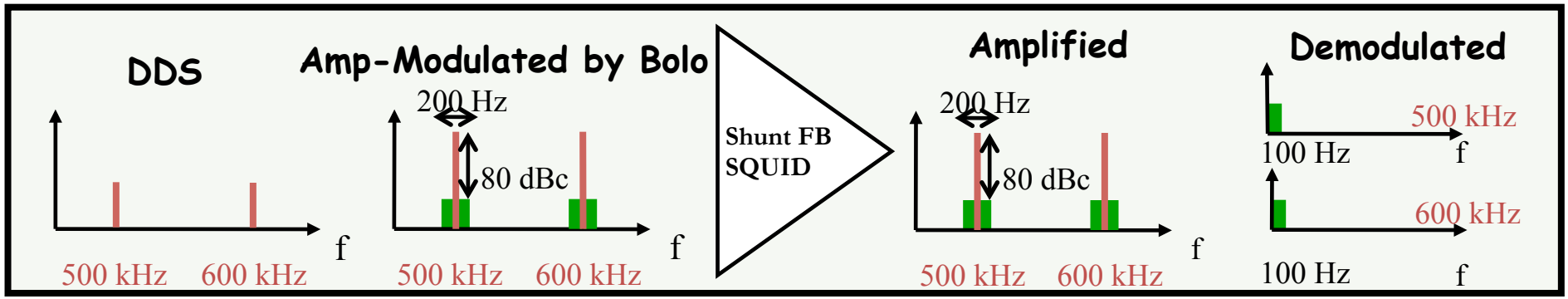
EBEX
1500 TES, 2013
Digital fMux
LD Balloon

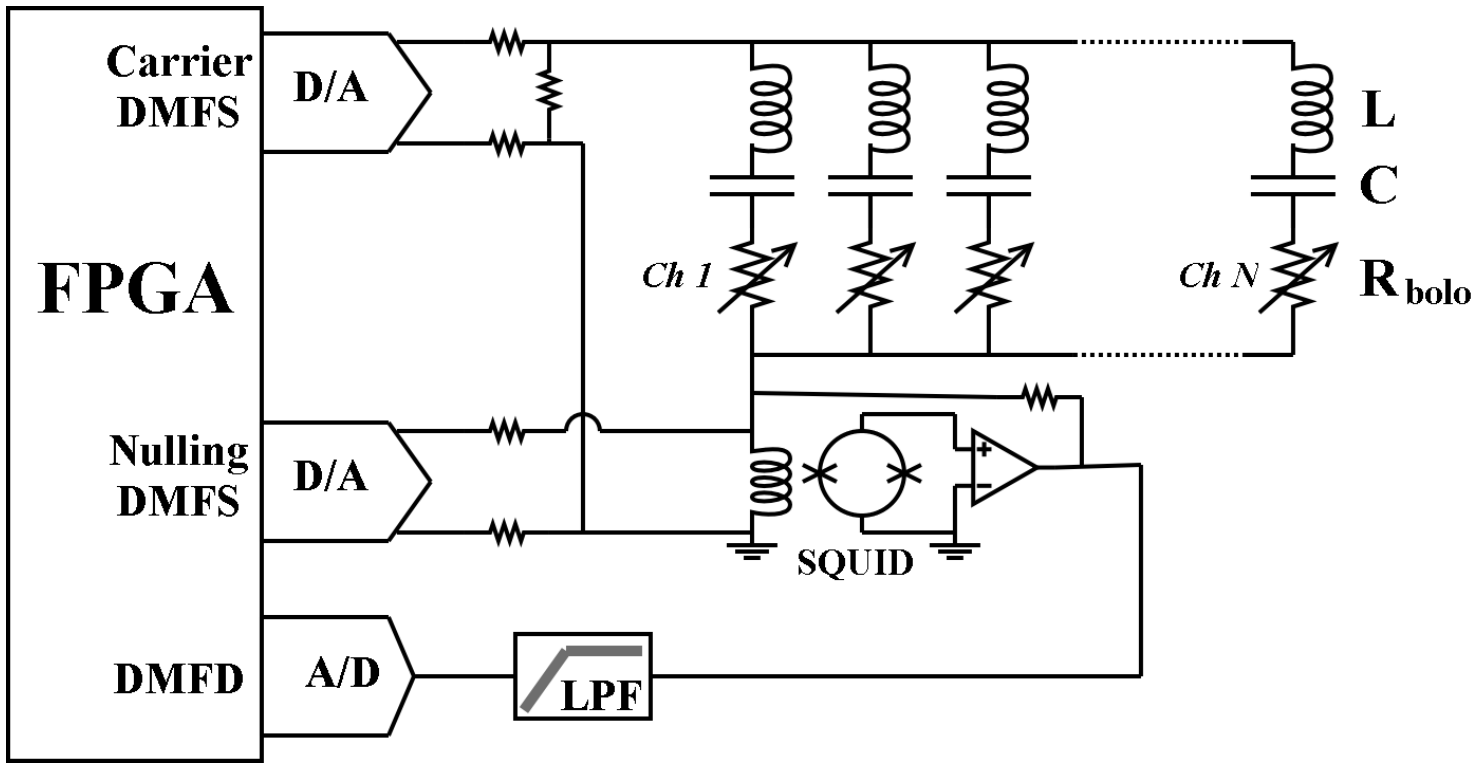
Simon's Array/PB2
22,768 TES, 2016
New COTS Digital fMUX

SPT3g
15,000 TES, 2016
New COTS Digital fMux



MHz Frequency Domain Multiplexer

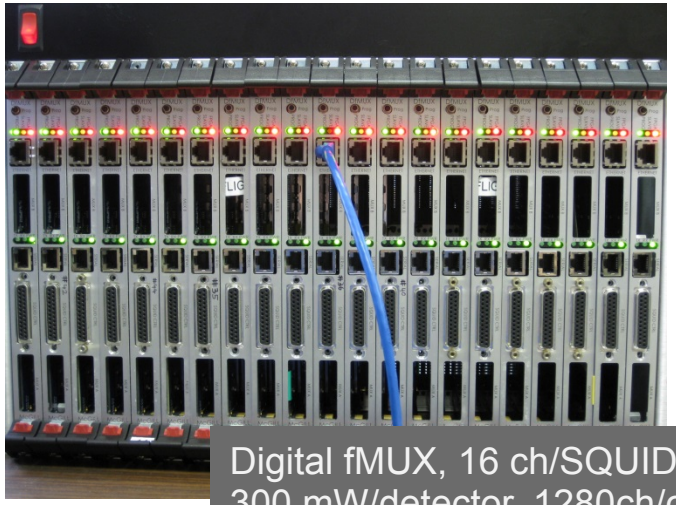




DFMUX Readout system

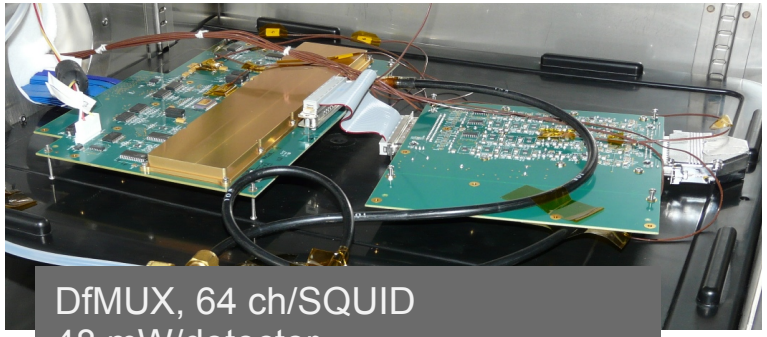
(LBNL/UCB)

Analog fMUX, 7 ch/SQUID
3 W/detector, 320ch/crate
2006 South Pole Telescope



Digital fMUX, 16 ch/SQUID
300 mW/detector, 1280ch/crate
2010 EBEX Balloon
2010 SPTpol

DfMUX, ICE System 64 ch/SQUID
(warm components to 128x)
100 mW/detector, 8192ch/crate
2016 SPT3g
2016 PolarBEAR2, Simon's Array

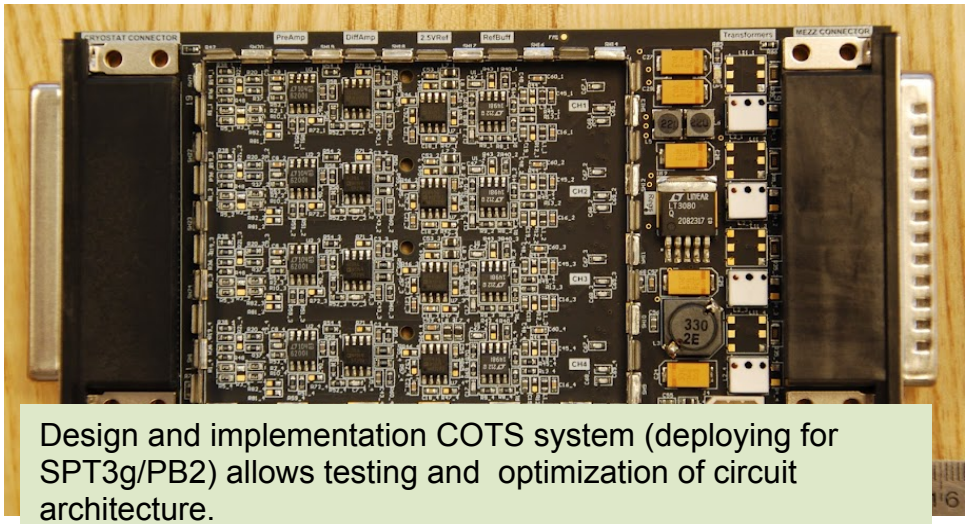


DfMUX, 64 ch/SQUID
48 mW/detector
2014 Flight Representative System
→ LiteBIRD

McGill / COM DEV / CSA Tech Devel.

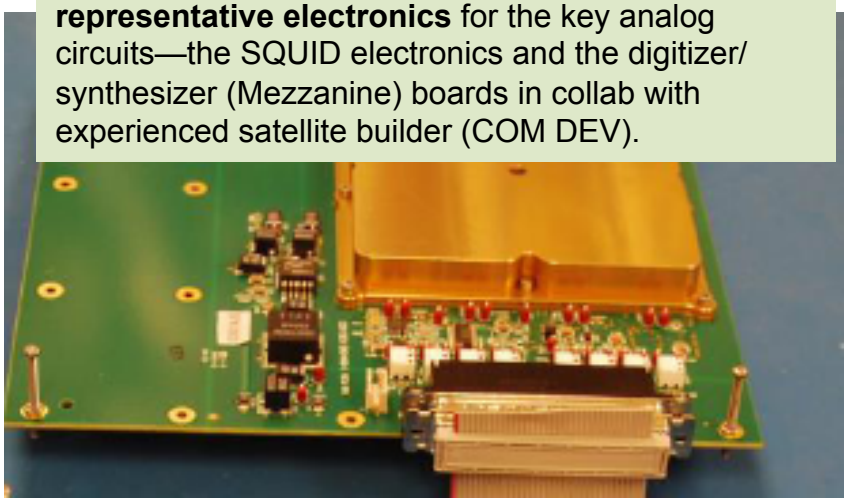
- Canadian Space Agency STDP-4 Program: Jan 2012 – Jan 2014
  - **Canadian Collaboration**
    - McGill University (Project Lead)
    - COM DEV – (prime contractor for JWST, SPIRE, etc. in Canada)
- **Overall objective**: demonstrate TES readout electronics for satellite platforms, focus on LiteBIRD.
- **Technical goals of the project**:
  - Reduce power consumption per bolometer by a factor of 5 → 50 mW/ detector
    - Increase multiplexing factor by a factor of 4 to 64x (more bolometers per wire)
    - Use newer generation low-power FPGAs with new signal processing algorithms
    - Reduce dynamic range requirements for the SQUID with Digital Active Nulling.
  - Lower load on thermal stages (less wires)
    - Reduce restrictions on wire length or maximum operating frequencies with DAN
  - Maintain system performance, including noise.
  - Produce a flight representative model for environmental testing.
    - DSP/FPGA not included yet.

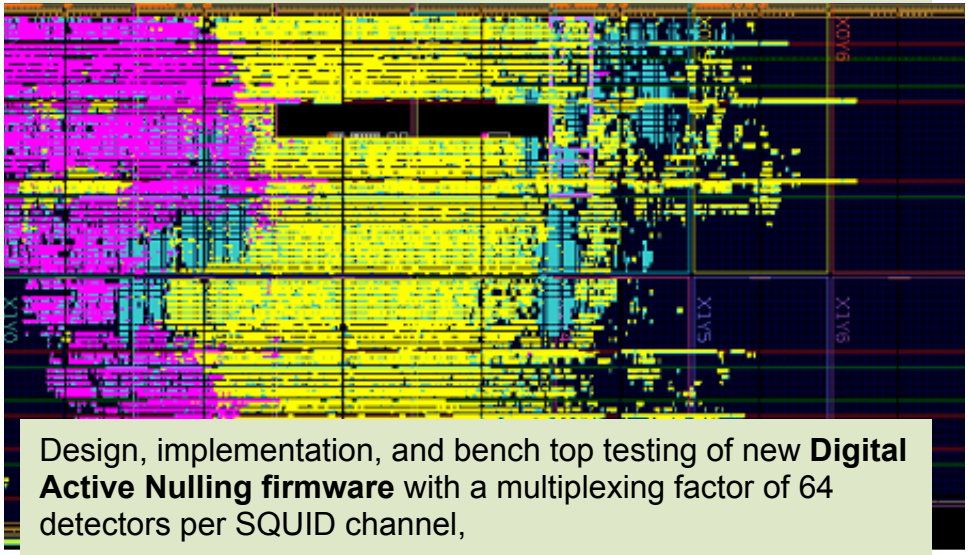
CSA Tech Project Methodology



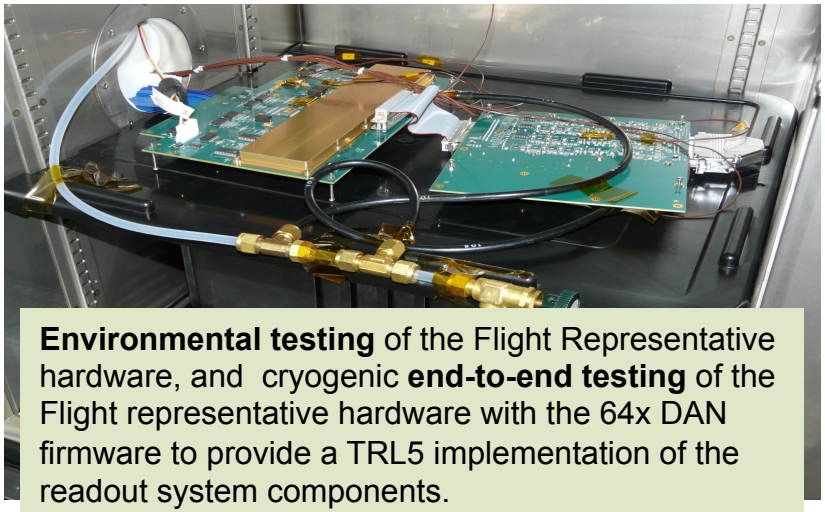
Design and implementation COTS system (deploying for SPT3g/PB2) allows testing and optimization of circuit architecture.

Design, construction and testing of **flight representative electronics** for the key analog circuits—the SQUID electronics and the digitizer/ synthesizer (Mezzanine) boards in collab with experienced satellite builder (COM DEV).





Design, implementation, and bench top testing of new **Digital Active Nulling firmware** with a multiplexing factor of 64 detectors per SQUID channel,



Environmental testing of the Flight Representative hardware, and cryogenic **end-to-end testing** of the Flight representative hardware with the 64x DAN firmware to provide a TRL5 implementation of the readout system components.

CSA Project: Environment requirements

- Design for L2: determines the radiation & thermal environments
  - Use COM DEV's JWST studies, assumes thin alum. shielding for electronics.
- The mission life was assumed to be 2.5 years, with factor 2 margin (5 years)

Environment	Requirement	Relevance
Radiation	50 krad TID (under 1mm Alum)	Flight qualified / rad hard parts selection
Thermal Operation Thermal Survival	-10 C to +50 C -40C to +100C	Parts selection, test temperature range
Thermal Stability	1 C / 24 hr	
EMC	MIL-STD-461	Susceptibly dependent on configuration – must be self shielding
Magnetic	< 400 nT DC < 0.3 nT AC	Susceptibility to DC fields to be tested
Vibration	TBD	Dependent on mission / launcher

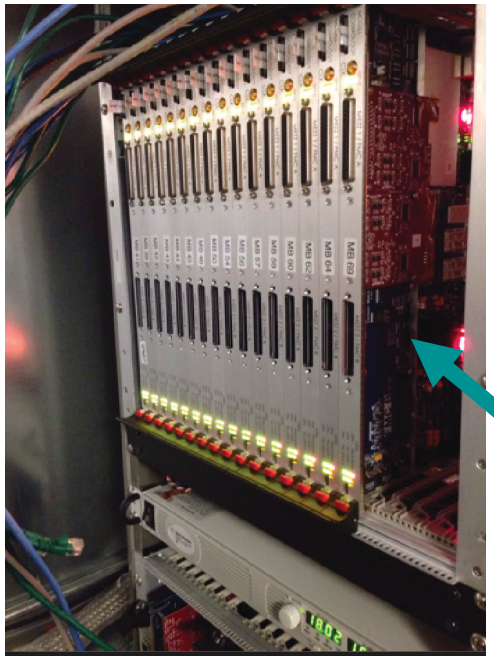
Performance Evaluation Criteria

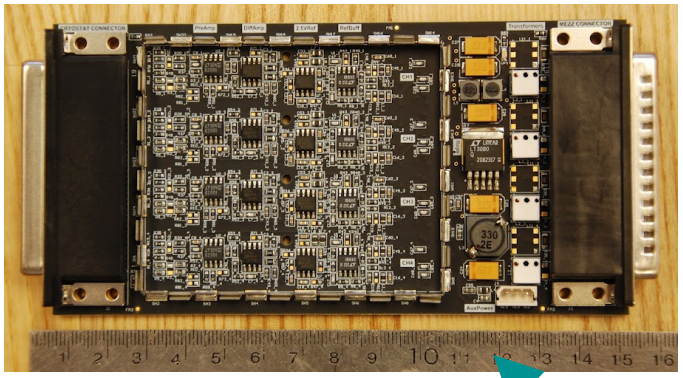
- **Detector stability**:
  - The system must allow for stable and robust operation of the TES bolometers deep in transition.
- **Readout system noise**
  - The readout system should produce insignificant increase in overall detector noise (< 10 pA/√Hz)

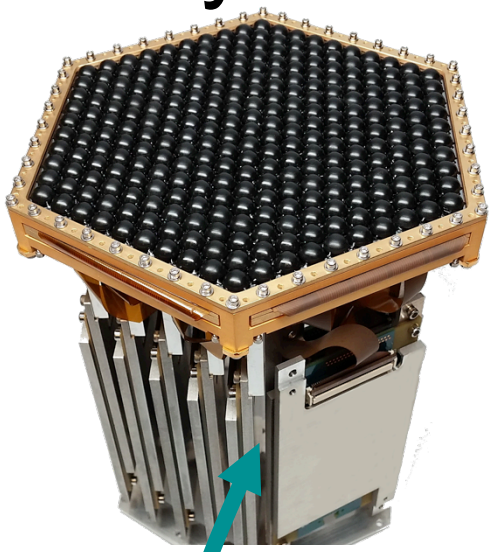
  → *achieve 7pA/√Hz typical*
- **Multiplexing factor**
  - Target 64 TES readout per SQUID readout module

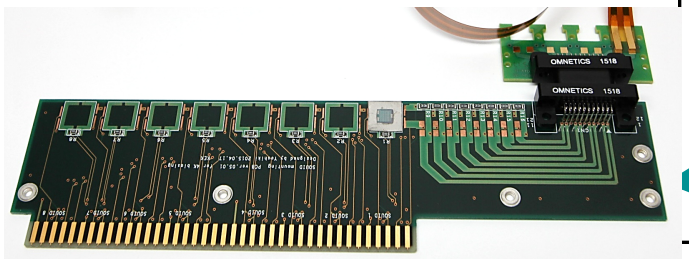
  → Recently (post-project) *128x available for warm system, but cold components presently support 64x only.*
- **Power Dissipation**
  - Target 40-60 mW/detector → *achieved 48 mW/det @64x*
  - With FPGA demo electronics. FPGA board design will change (improve!?) this.

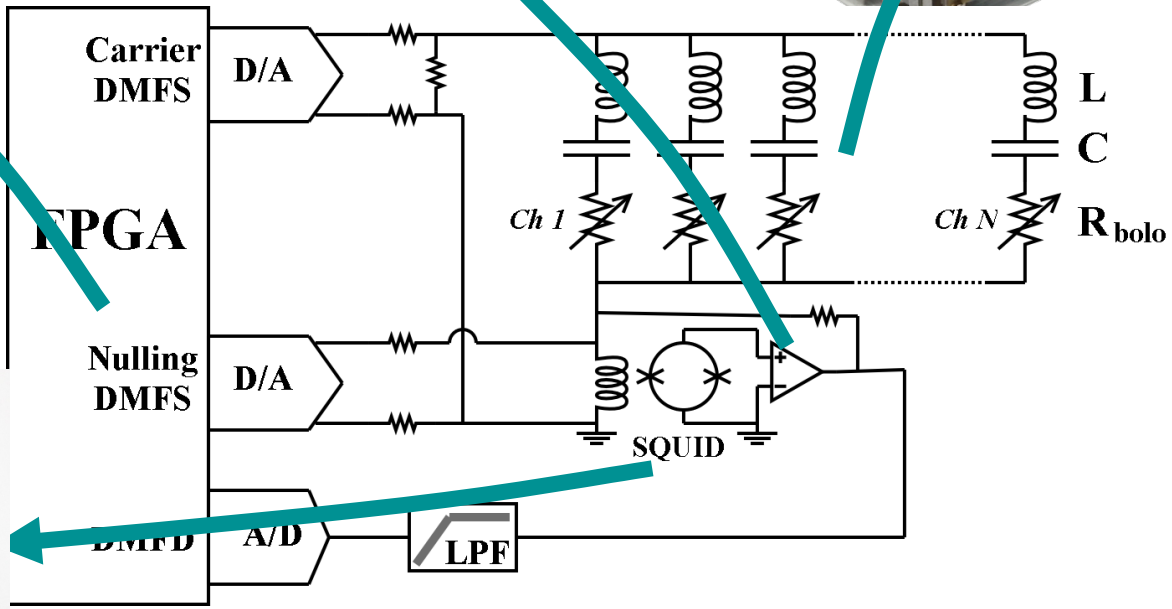
DfMux Readout: Ground-based System



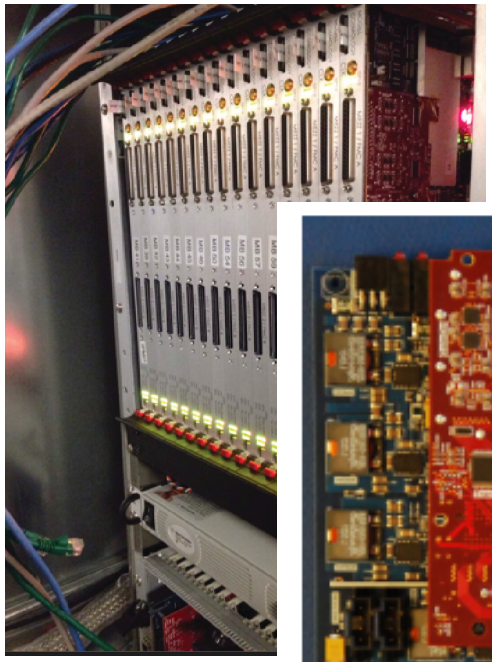


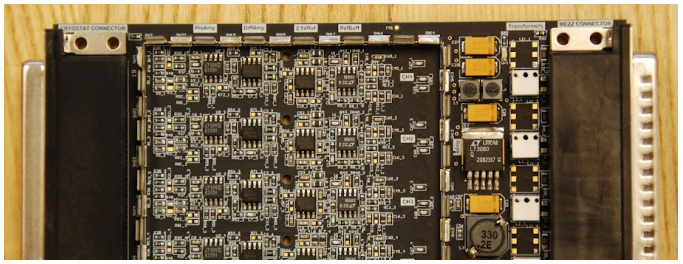


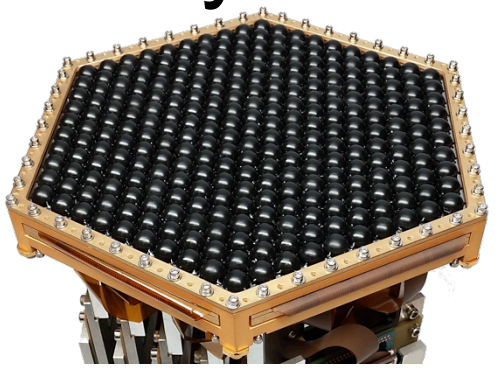


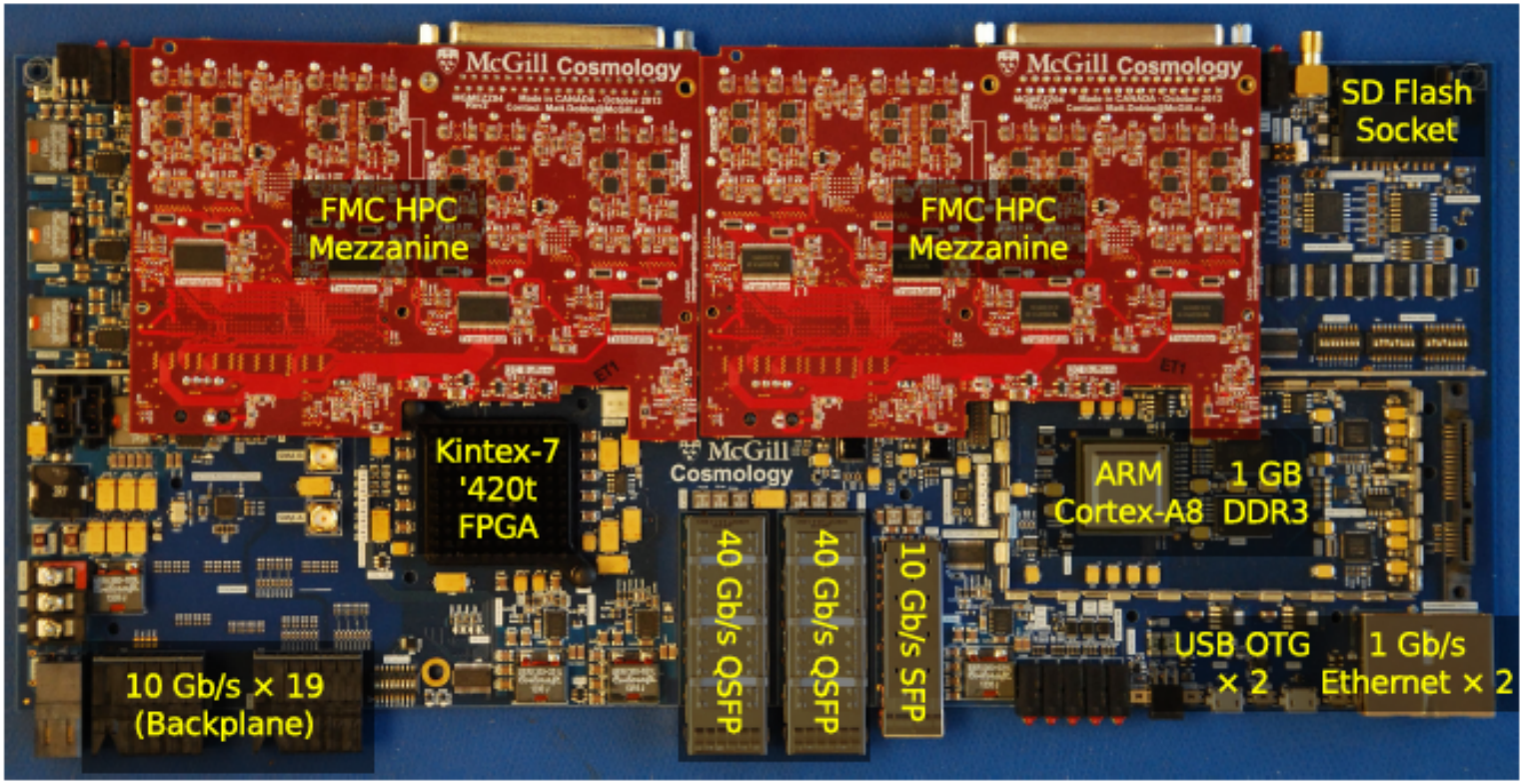


DfMux Readout: Ground-based System









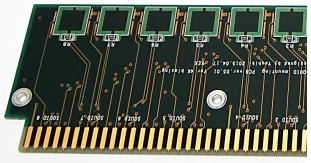
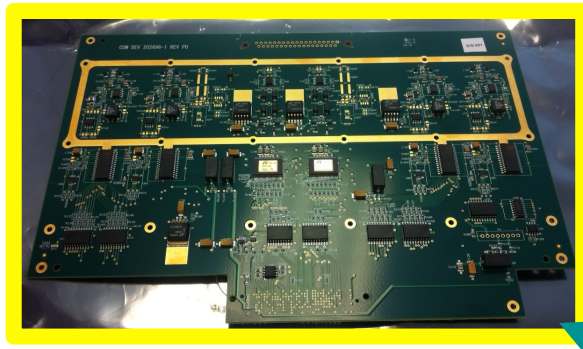
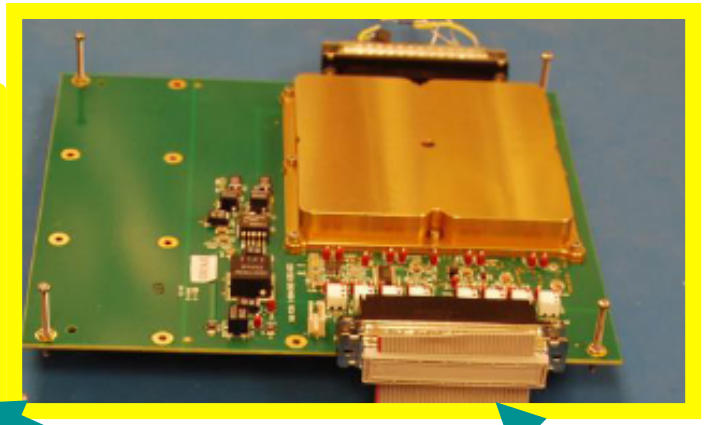
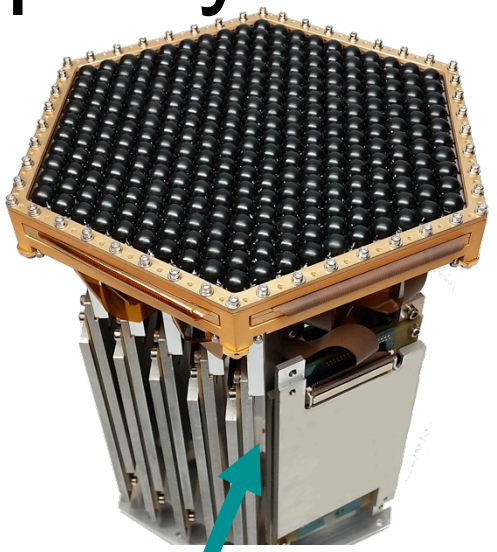


Figure 3. The ICE motherboard, McGill's new FPGA platform. The black heat sink covers the FPGA; the CPU, DDR3 RAM, and Ethernet PHYs are visible on the right. The red mezzanines are two FMC-compliant high-speed data-acquisition boards.

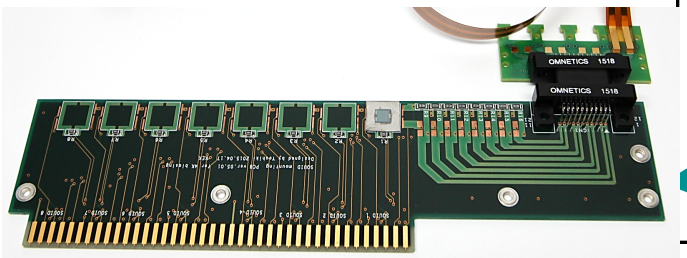
DfMux Readout: Flight Rep. System

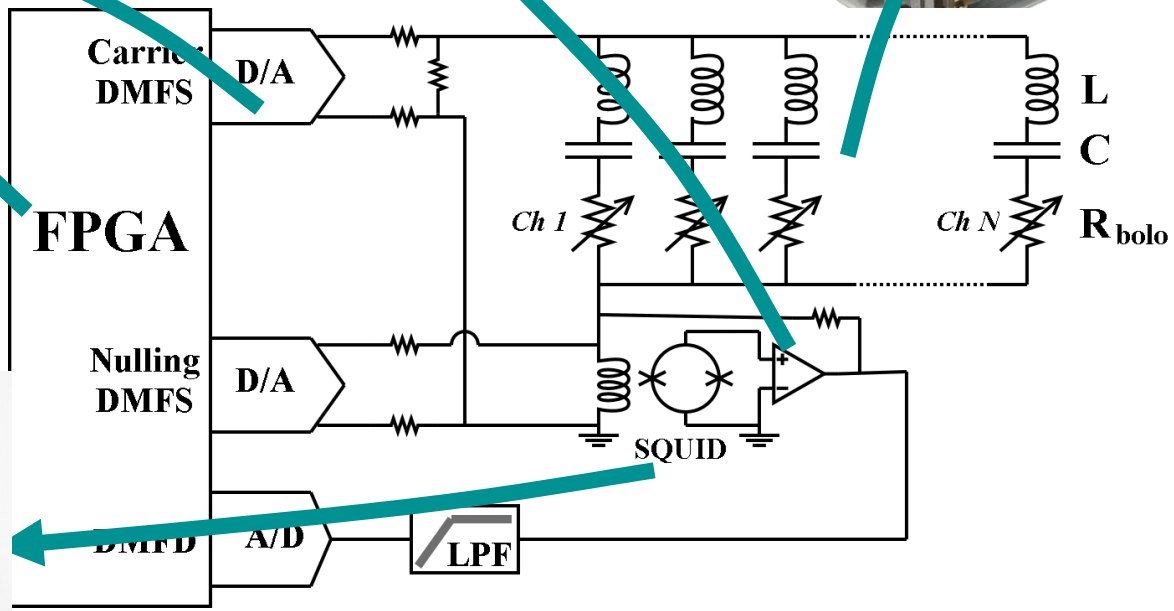




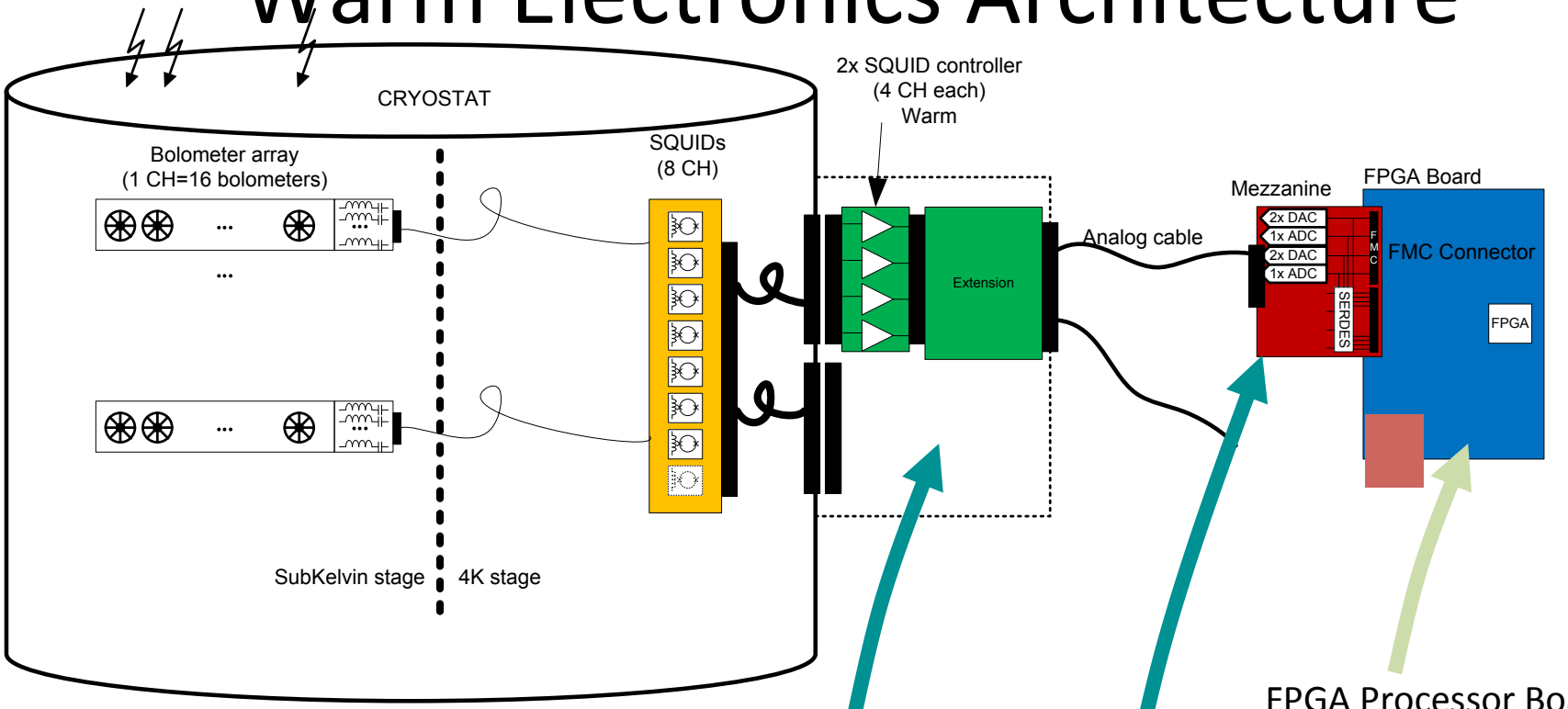


FPGA Motherboard
→ Project scope did not include FPGA board. Technology changing too fast to pin down this early.





Warm Electronics Architecture



SQUID Controller board (4 SQUIDs)

Amplifies the SQUID output and send it to the mezzanine board

FPGA Processor Board

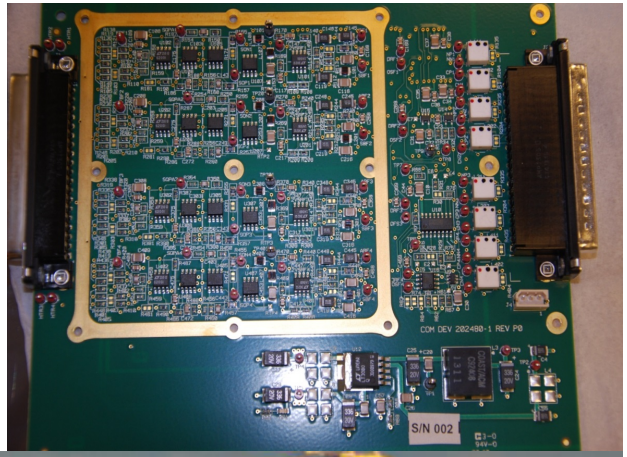
- Signal Processing and Digital Interface

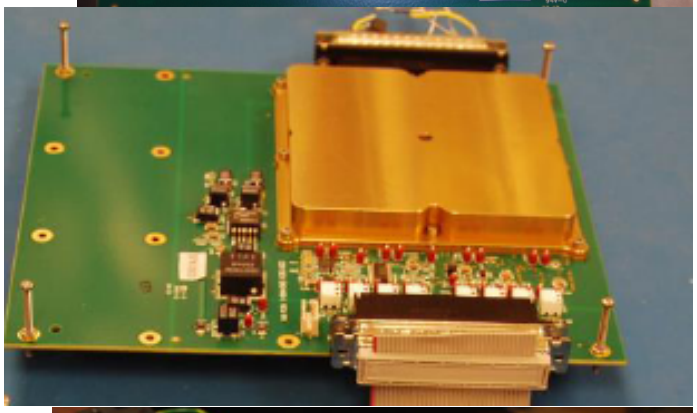
Mezzanine Digitizer (2 SQUIDs)

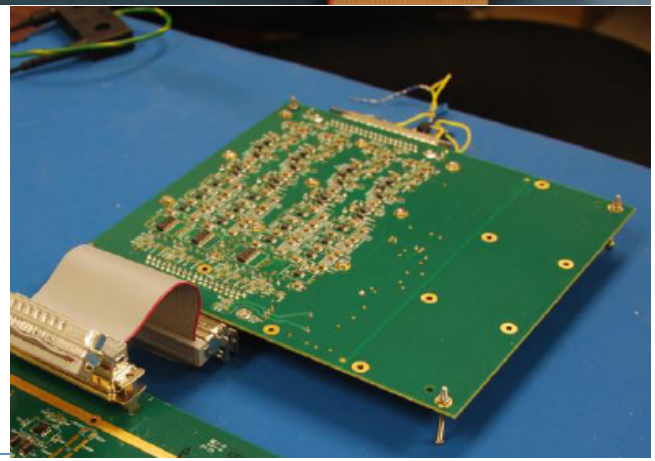
- Generate Carrier bias and nuller and send it to SQUID controller & cryostat

Flight Rep. SQUID Controller

- Flight qualified PCB design and qualified rad-hard components.
- Control and Analog Signals for 4 SQUIDs.
  - 1 nV/√Hz first stage amplifier noise.
  - 10 MHz bandwidth
- Flux locked loop:
  - low frequency: flux locked loop integrator
  - High frequency: DAN
- Power: 170 mA at 5.5V (single rail)
  - 246 mW/SQUID
- Size: 18.1 x 18.6 x 1.7 cm, 220 g.
- Location: inside cryostat RF cage, mated directly to cryostat.
- Interface:
  - Simplified, space-friendly SPI interface.
  - DB37f to cryostat, DB37 to Mezz.
  - Compatible with ground based “ICE” electronics

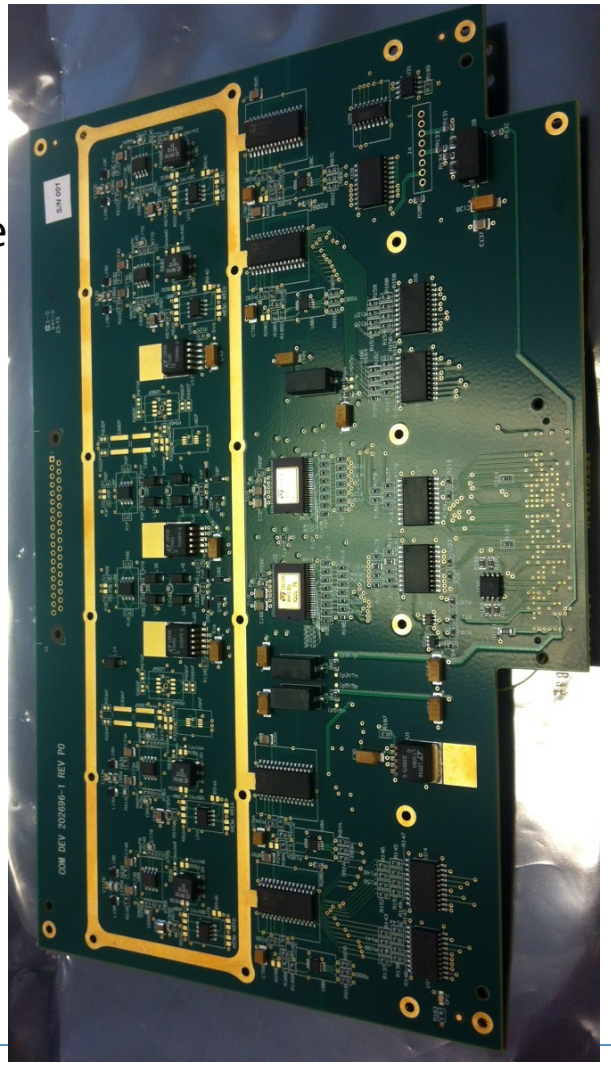






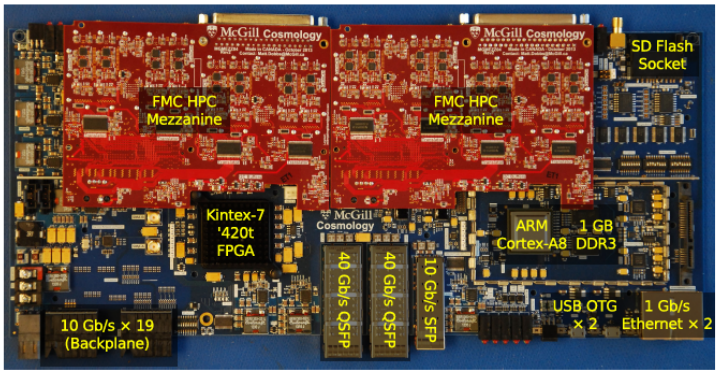
Flight Rep. Digitizer/ Synthesizer Mezzanine

- Flight qualified PCB design and qualified rad-hard components.
- Control and Analog Signals for 2 SQUIDs Modules
  - Nuller/Carrier synthesis at 16 bits, 20 MHz ← drive system performance.
  - Demodulator at 12 bits, 20 MHz.
- Power: 3.2W
  - 1.6 W/SQUID
  - Could reduce power further by qualifying lower power DAC.
- Size: 26.6 x 17.8 x 1.9 cm, 310 g.
- Location: anywhere within few meters of SQUID controller, within thin aluminum shielding.
- Interface:
  - Connects directly to FPGA/DSP motherboard.
  - DB37 to SQUID Controller
  - Compatible with ground based “ICE” electronics



NEXT: FPGA/DSP Motherboard

- Handles DSP, system setup, and data offload.
- Interfaces to Synth/Digitizer Mezz
- DSP takes about half of system power.
- Candidate technology:
  - Xiphos Q7
    - FPGA with radiation hardness by design
    - Size: 7.8 x 4.3 x 1.9 cm, 24 g.
  - Custom ASIC on custom board.
    - Mission-agnostic investigation underway with APC.
- Location: anywhere within few meters of SQUID controller, within thin aluminum shielding.
- Interface:
  - Connects directly to Mezz.
  - fast serial duplex communications
  - 10 MHz clock, timestamp.



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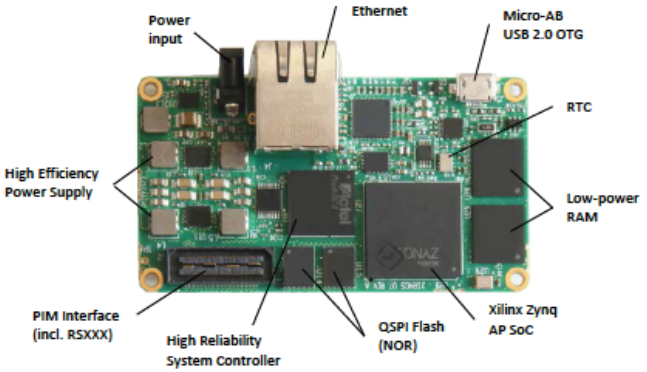
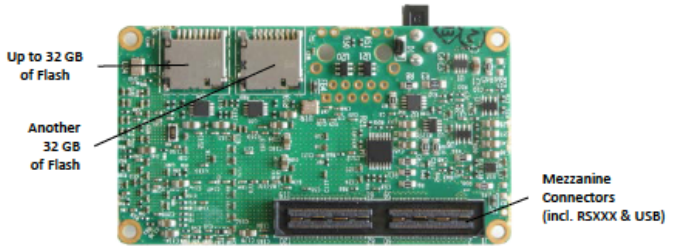


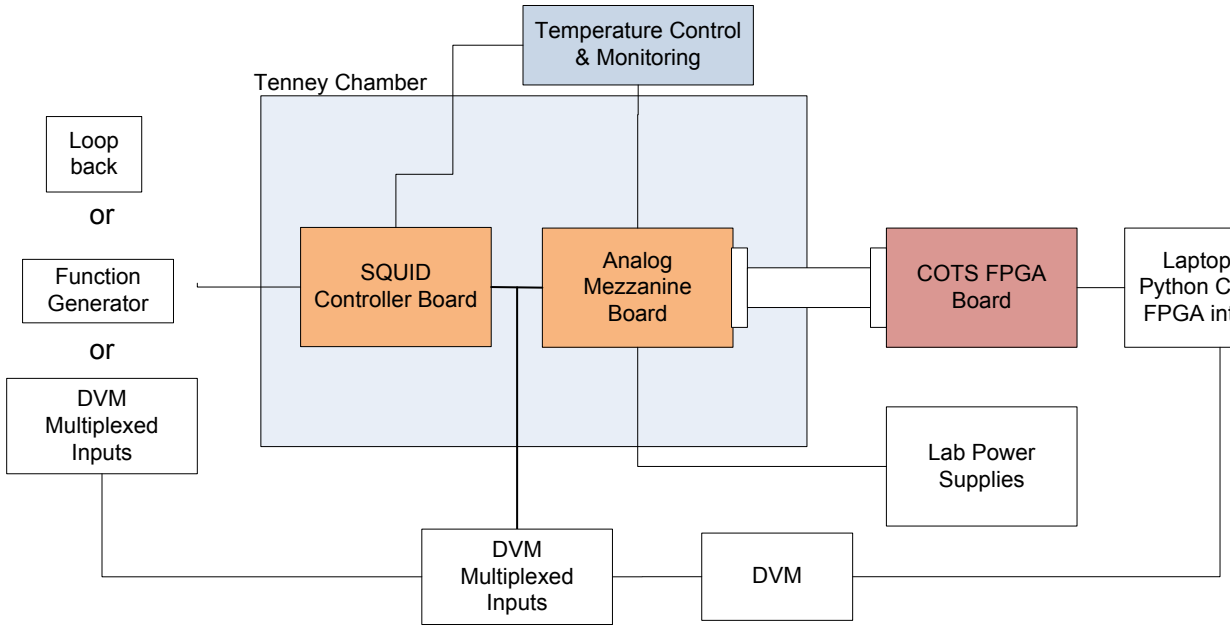


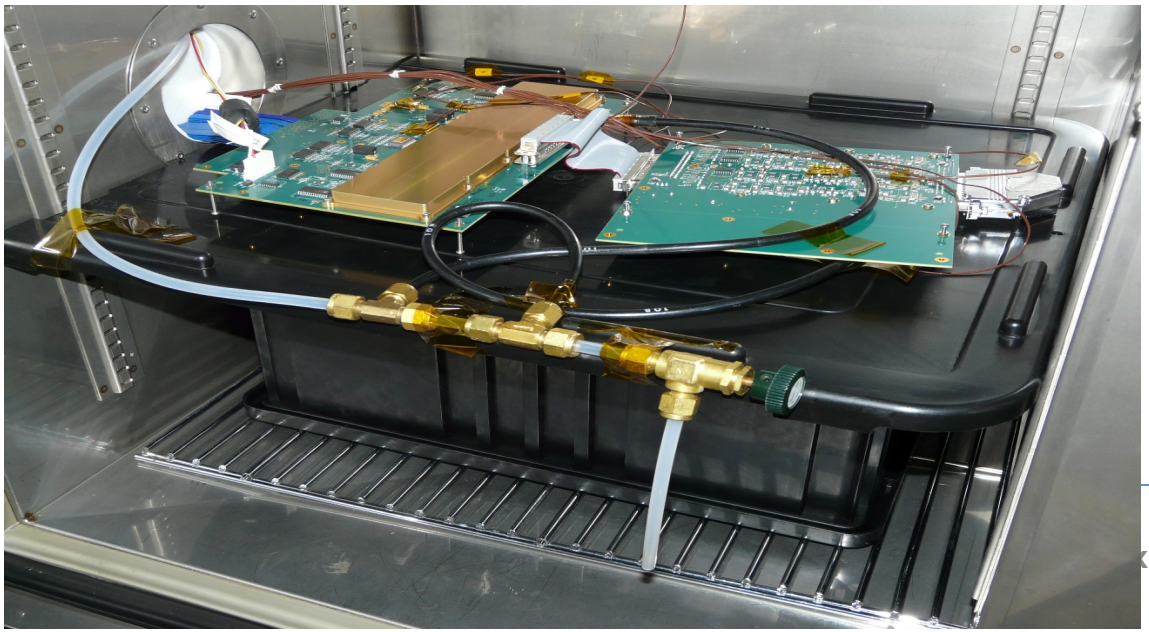
Xiphos specializes in flight-qual FPGAs.

- Q5 operated continuously in orbit since 2006.
- Q6 flown in 2011.

System-level Test Results

Flight Rep Thermal Testing





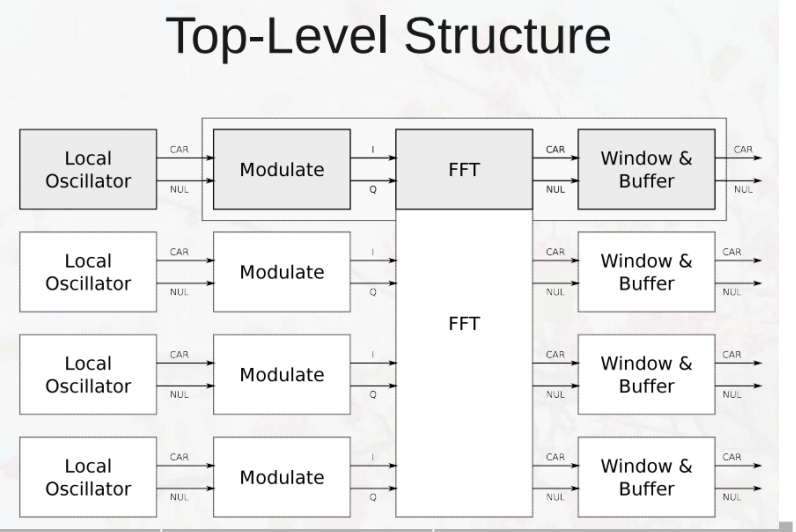
- Noise decreases by about 10% going from 40 C to -20 C
- Power consumption decreases by about 10% going from 40 C to -20 C
- Bias current DC changes are very small with temperature and do not affect system operation.
- low and high frequency roll-offs change by a few percent and do not affect system operation.

- ***Overall, the system performs well across full temperature range*** and minor improvements can be realized by operating the electronics below 0 C.

Power Consumption with 64-ch firmware

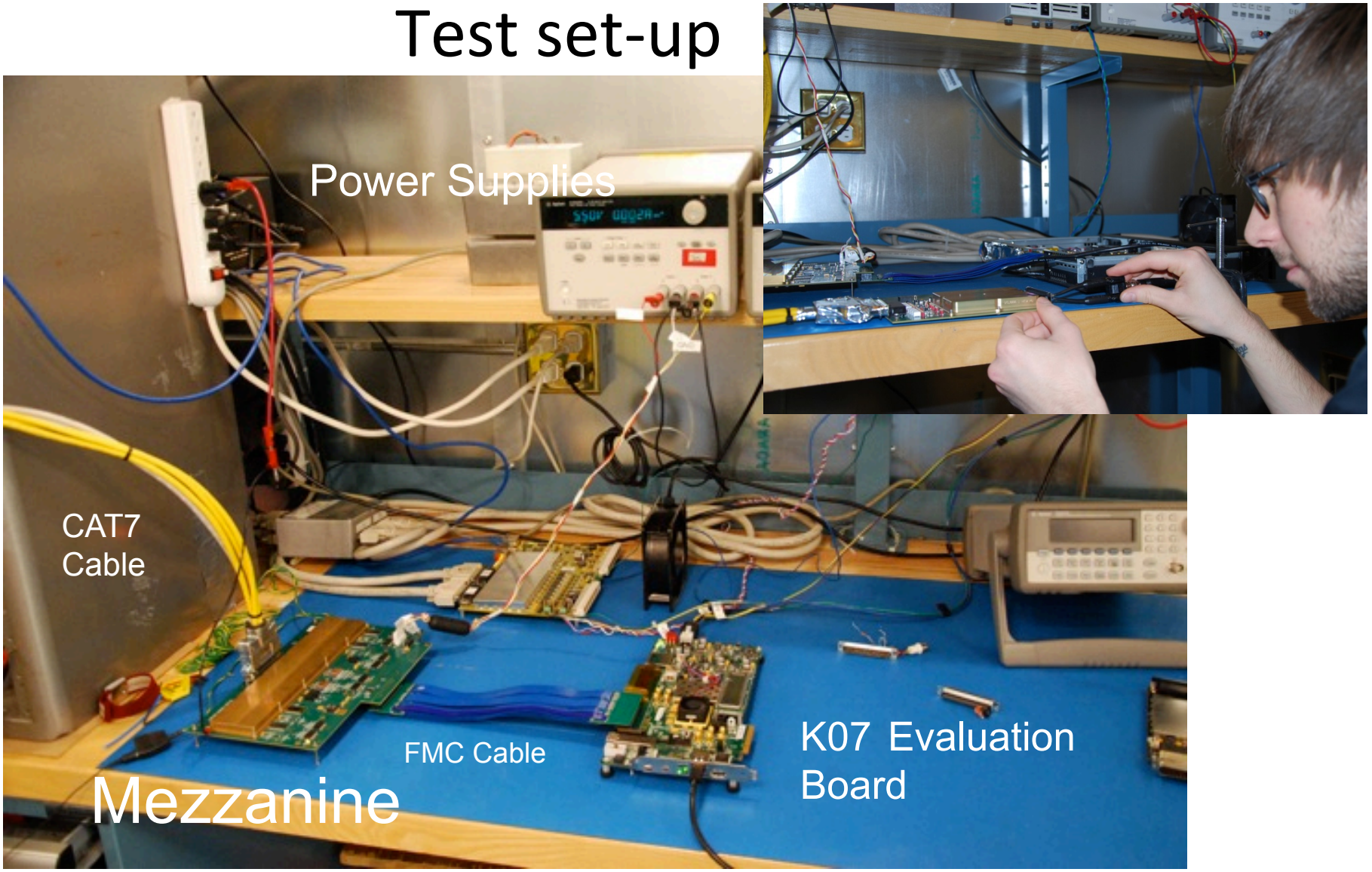
New, low power, DSP Architecture:

- Uses Polyphase filter Banks (PFB) followed by a inverse FFT to generate multiple carriers/nullers at once.



Design		Analog	Digital (Fixed)	Digital (Scaling)	Total
Current Design (M=16, N=4)	Total Per Bolo	6.6 W 100 mW	5.7 W 89 mW	3.4 W 53 mW	15.8 W 240 mW
Higher Mux Factor (M=64, N=4)	Total Per Bolo	6.6 W 26 mW	5.7 W 22 mW	6.5 W 25 mW	19.1 W 73 mW
With recent FPGA (Estimated)	Total Per Bolo	6.6 W 26 mW	2.8 W 11 mW	3.2 W 13 mW	12.6 W 50 mW
With KC705 and flight-rep mezz	Total Per Bolo	6.35 W 24.8 mW		6.17 W 24.1 mW	12.5 W **48.9 mW**

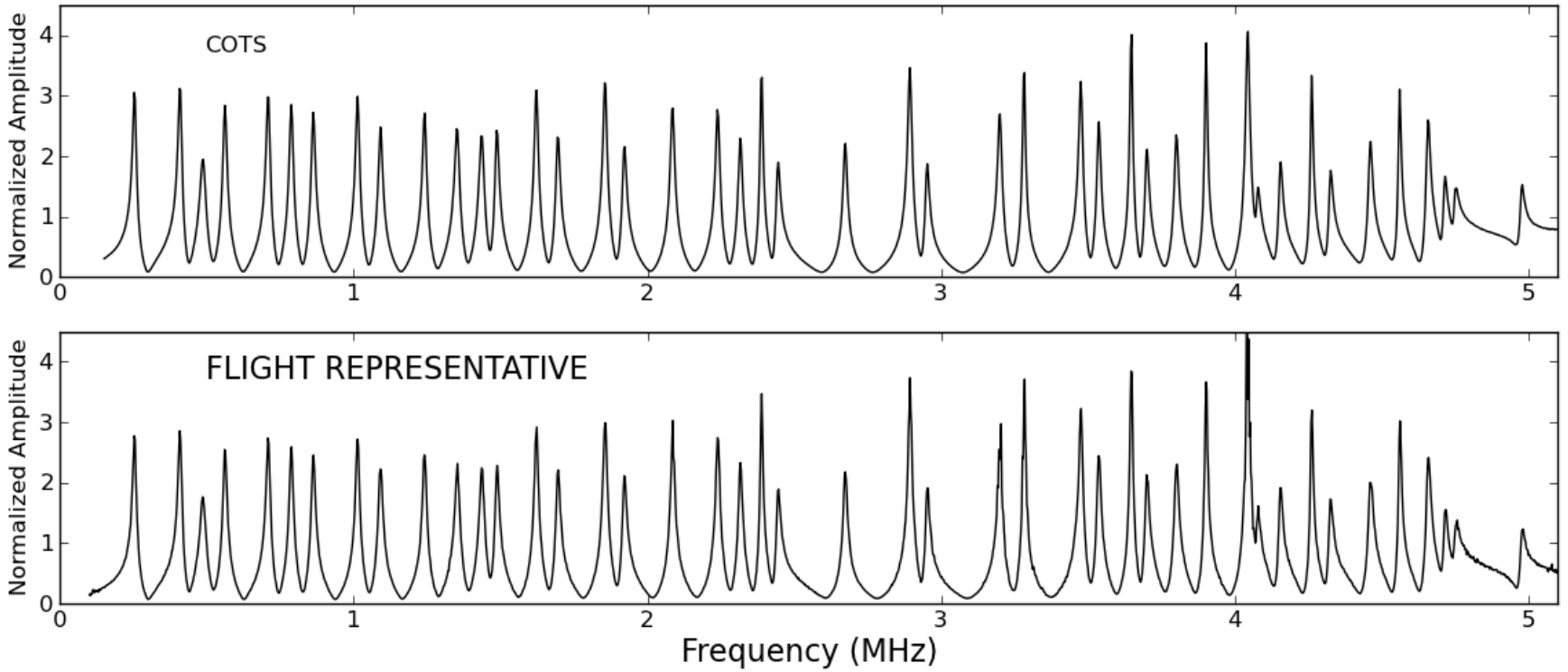
Flight Representative Mezzanine Test set-up



Cold Component Characterization

44 bolometers/resistors readout using a single SQUID.

Results are identical to COTS.

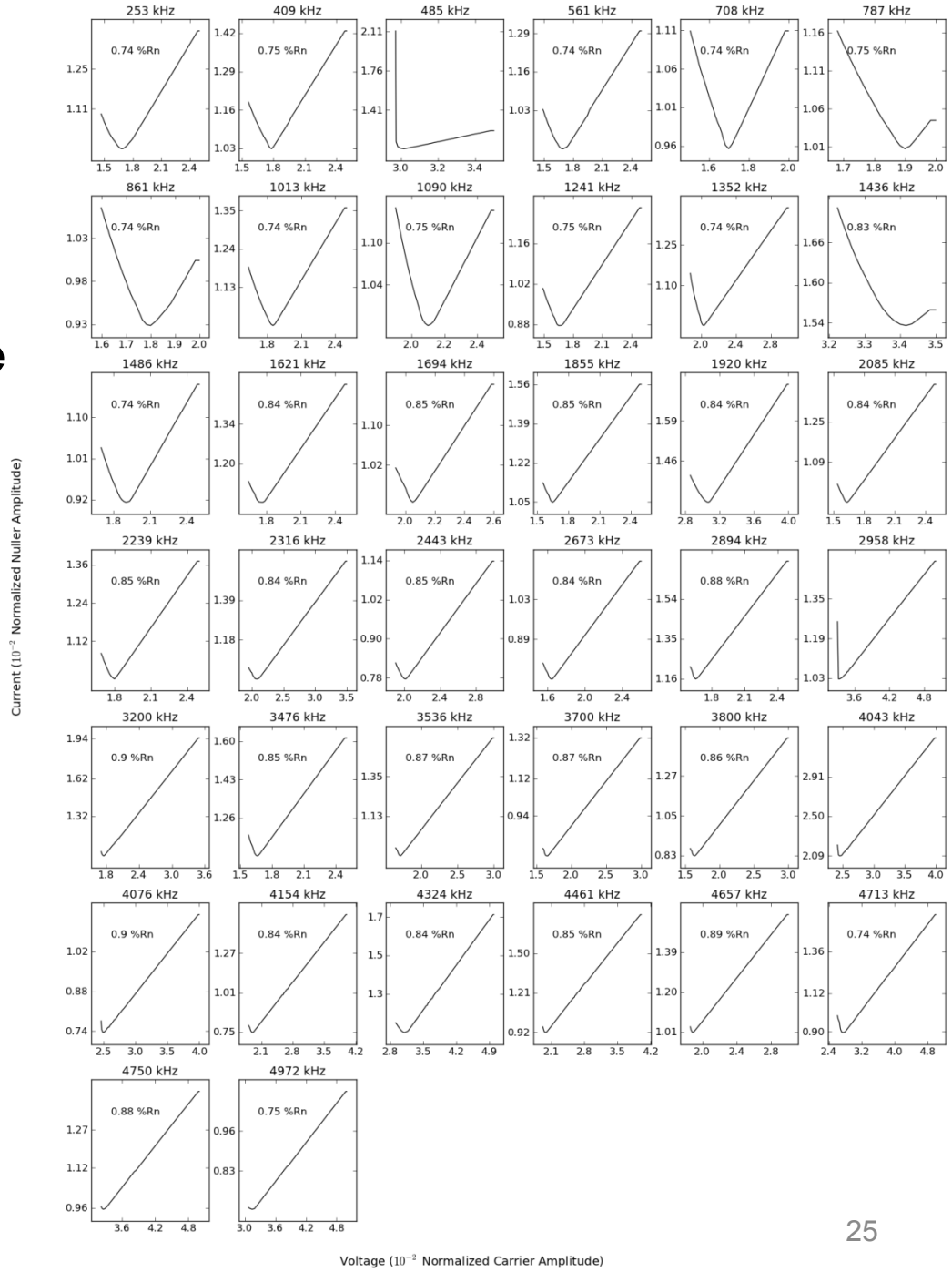


Bolometer Operation

Bolometers are operated in the superconducting transition.

Bolometers operate stably after characteristic turnaround in IV curves.

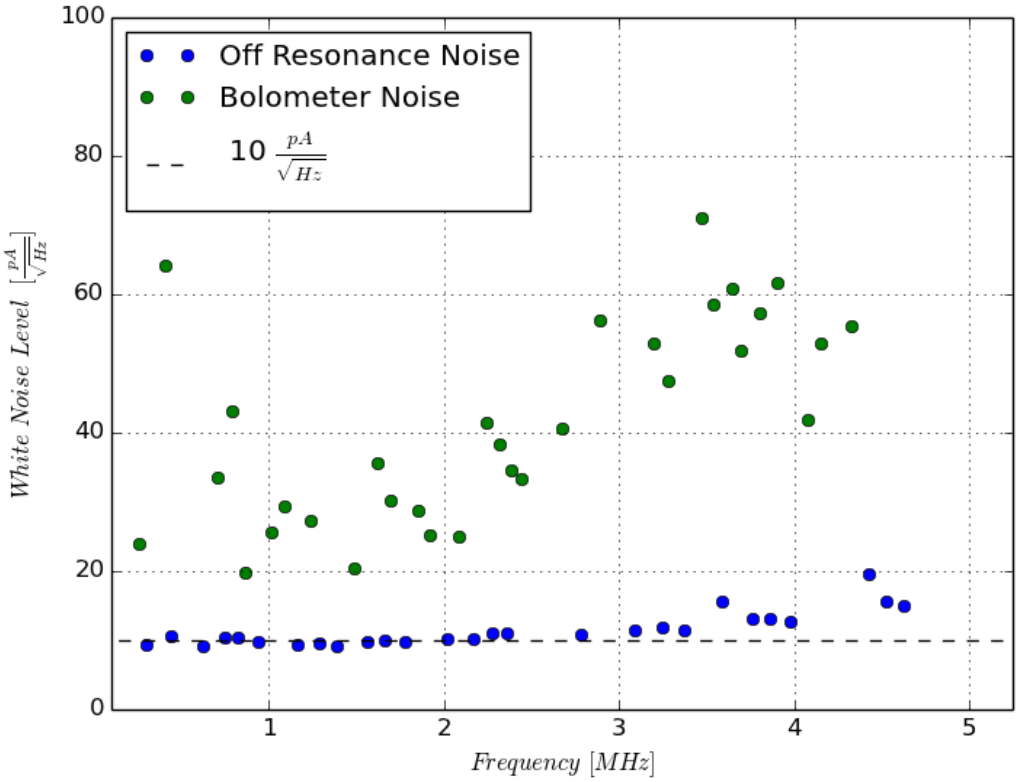
Bias points range from 0.75-0.9R_{total}.



Bolometer & Readout Noise

32 bolometers + 28 off-resonance channels operated simultaneously

- White noise level measured in 10-40 Hz band adjacent to the carrier
- Rise in bolo noise with frequency is due to parasitic-induced responsivity increases.



FMUX technology in flight: EBEX

EBEX stratospheric balloon telescope launched December 29, 2013 from McMurdo, Antarctica. The payload used the 16x DfMux readout.

The system functioned according to specifications – noise, power consumption, detector tuning, SQUIDs.

First demonstration of this technology in a space-like environment.

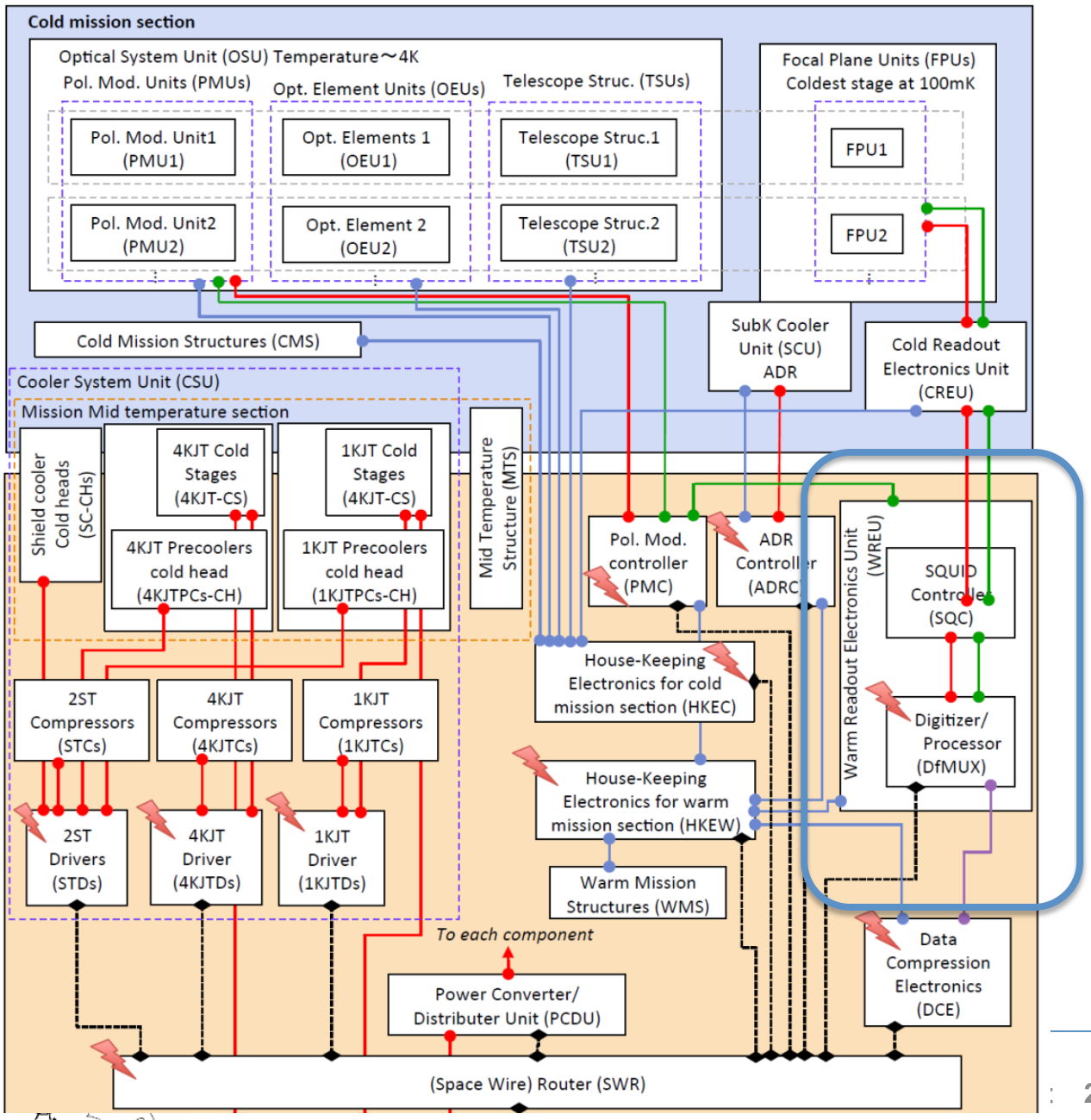
TRL Evaluation

	TRL-3	TRL-4	TRL-5	TRL-6
SQUID Controller Board (incorporating DAN)	Proof of concept test (modified EBEX board with cryo-bolometers)	a) Updated board design for digital active nulling components b) Phase 1 boards tested with bolometers	a) Update board designs with flight representative components b) Boards tested together over temperature c) Boards tested with representative cryo bolometers & cryo SQUID	System Demonstration with flight like boards, harnessing and flight like detector array & SQUIDs Temperature testing of boards (if required by TRL-5 results). Other environmental testing as required.
Analog Mezzanine Board (incorporating DAN)		a) Updated board design for digital active nulling components b) Phase 1 boards tested with bolometers		
FPGA Board *	EBEX Boards	FPGA flight like design (SEU mitigation in place)	Flight like boards tested with above.	
FPGA VHDL Code *	EBEX VHDL Code	VHDL code modified for DAN	SEU monitoring to be demonstrated on EBEX flight	
SQUIDs & Cryogenic Board	Partner Contributions			
Bolometer Array				
Cryogenic Harnessing				

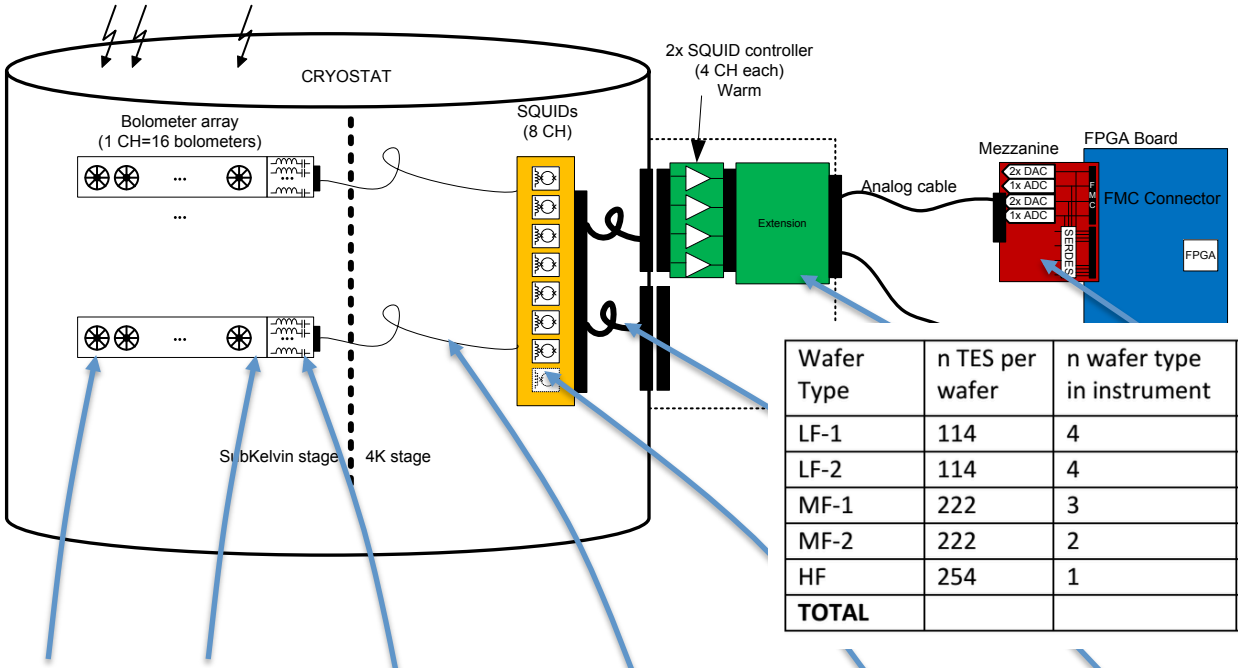
Legend:
- EBEX Heritage
- This proposal
- Future Development
- Partner Contribution

LiteBIRD block diagram ver.3 (in TES option)

2015-12-1 v1.1e



Warm Electronics Architecture



Wafer Type	n TES per wafer	n wafer type in instrument	n TESs per wafer type	n SQUIDs per wafer	**n SQUIDs per wafer type**	optical mux factor
LF-1	114	4	456	2	**8**	57
LF-2	114	4	456	2	**8**	57
MF-1	222	3	666	4	**12**	55.5
MF-2	222	2	444	4	**8**	55.5
HF	254	1	254	4	**4**	63.5
TOTAL			**2276**		**40**	

TES	TES-LC Wires	LC Modules	LC-SQUID Wires	SQUIDs	SQUID-warm wires	SQUID Contr.	2ch Mezz.	
2276	4552	40 (55-64x)	80 0.25-4K	40	250 4K→300K	10	20	125.4W
2276	4552	20 (111-127x)	40 subKelvin	20 Cold!	250 subK→300K	5	10	~75W

Aggressive → not suitable as baseline.

High, because wafer numerology does not allow full use of 64x.

Next Steps

- Develop FPGA or ASIC motherboard for DSP
  - Still too early? This technology changes very fast.
  - Early stages of investigation in collaboration with APC Paris for EBEX.
  - Commercial solution, Xiphos X7 has ISS demonstration, could be suitable baseline.
- Is a better DAC rad hard?
  - Minor power savings possible by switching to LT1668 DAC (drives system performance)
  - Tested in beam at KEK November 2015 – will test performance at McGill.
- Warm electronics supports 128x or higher.
  - High mux factor puts heavy constraints on LC components, wiring strays.
  - Requires high bolometer uniformity.
  - → Joint bolometer/cold readout study needed.
- SQUID and Wiring:
  - Moving SQUID to sub-Kelvin renders problematic wiring strays negligible.
  - Requires 6-wires per SQUID (but they can be long).
  - Minor gains to be made by achieving higher SQUID transimpedance (>500 ohms)
  - Need to determine specification / constraints on SQUID-out wiring and SQUID dynamic impedance.
  - → joint SQUID/cryogenic study needed.

Interface and Packaging

- Interface:
  - Each board requires:
    1. communications (fast-serial duplex, such as ethernet)
    2. 10 MHz clock
    3. timestamp.
  - Bolo interface: 2 wires, see Cold MUX.
  - Cryostat interface: see Cold MUX.
- Packaging
  - Each board requires thin aluminum shielding.
  - Electronics boards are modular, and can be distributed across payload thermal regions payload for good radiative coupling and thermal performance.

Conclusions

- Flight representative models key readout electronics exist. Tested for performance and environment.
  - Further power improvements possible.
- FPGA/DSP motherboard is next development.
  - Candidate FPGA solution needs testing.
  - ASIC solution, but R&D expensive.
- Need also to invest politically for CSA role.
  - (Canadian astronomy long range plan draft emphasizes CMBpol as mid-scale priority for Canada)