TRIUMF

ハイパーカミオカンデ
Hyper-Kamiokande

Signal Digitization for Hyper-Kamiokande

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For Hyper-K DAQ and Electronics Group

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Outline

- Cover two options for 20” PMT signal digitization
  - QTC + TDC
  - FADC
- Remember requirements!

~ Some parameters ~

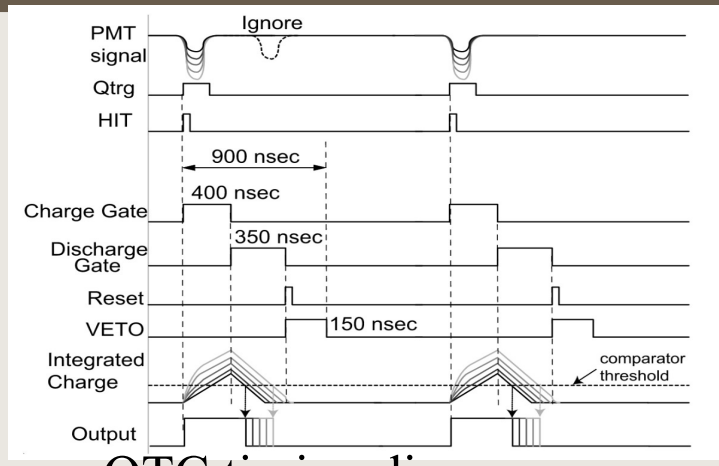
- Self triggering for each channel
- High Sensitivity for single p.e.
  - Discriminator threshold
    ~ ¼ p.e. *) (well below 1 p.e.)
- Processing speed/hit (channel dead-time
  ~ 1 μsec / hit
- Charge dynamic range
  0.1 ~ 1250 p.e. (0.2 ~ 2500 pC)
- Charge resolution
  ~ 0.05p.e. (< 25 p.e.) in RMS
- Timing LSB
  ~ 0.52 ns
- Timing resolution
  0.3ns (@1 p.e.) in RMS
  0.2ns (> 5 p.e.) in RMS

*) C

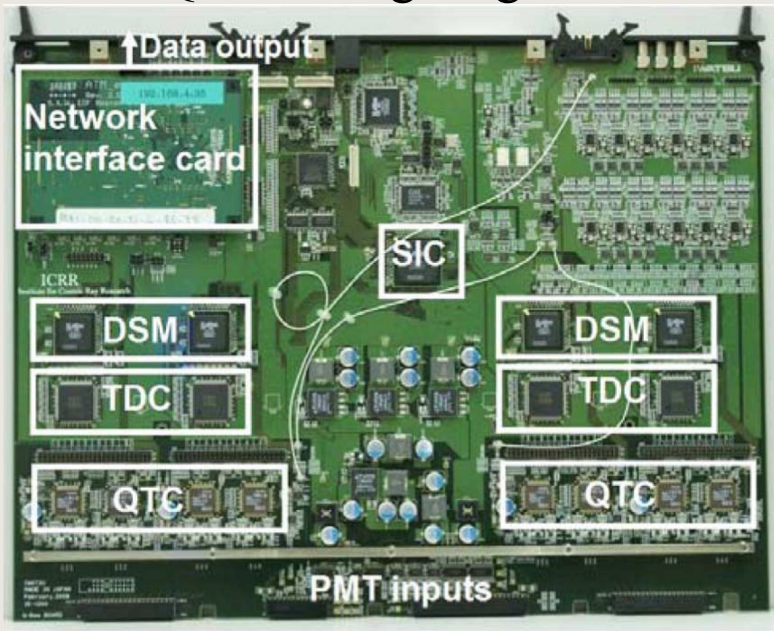
Also: ~1-2W per channel for electronics overall.

Super-K QTC/TDC board

- Very successfully QBEE board for Super-K IV.
- Based on QTC ASIC developed for Super-K.
- QTC:
  - Hit threshold at ~0.25pe
  - Digitial output pulse:
    - pulse length gives charge
    - leading edge gives time
- QTC Digital signal read out with TDC chip.



QTC timing diagram



Super-K QBEE board

Nishino et al, 2009
Yamada et al, 2010

QTC/TDC digitization for Hyper-K

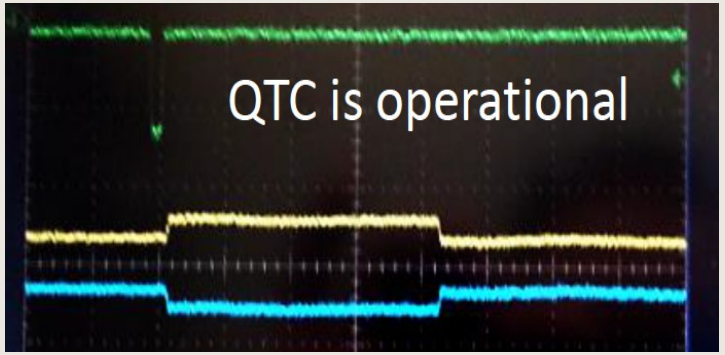
- Can use QTC/TDC type electronics for Hyper-K.
- Not enough existing QTC chips.
- Process rule of QTC is CMOS 0.35 mm; still possible to reproduce the same chip.

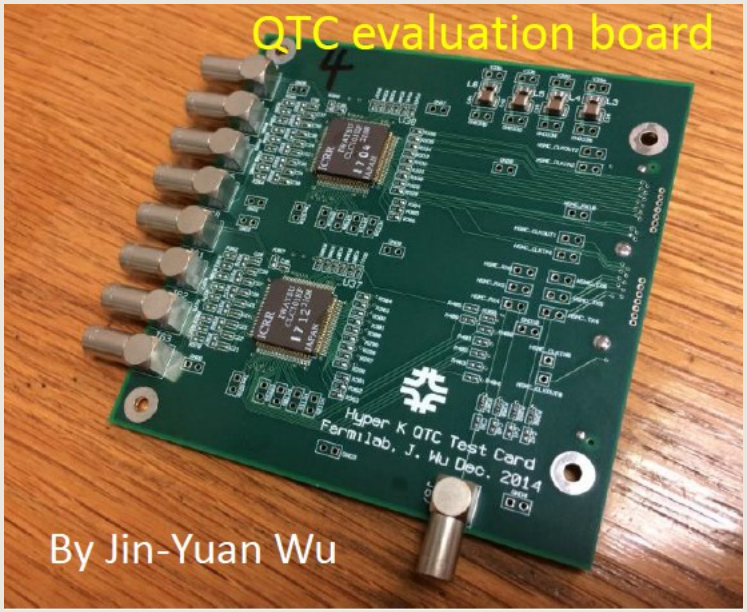
TDC Options

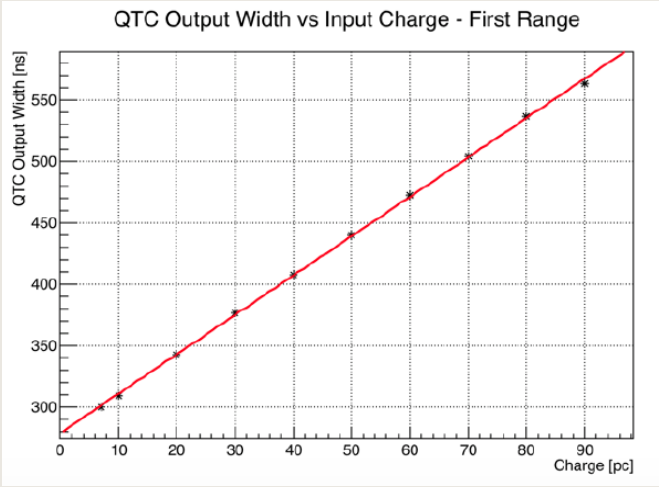
- TDC chip used for SK QBEE board is discontinued (AMT3)
- Options for new TDC chip:
  - FPGA based TDC
    - Recent low cost FPGA is reported to have sufficient performance. (FPGA-based “Wave Union” TDC *by Jin-Yuan Wu, Fermilab)*
    - *32 ch.TDC* was implemented in *$75 FPGA* chip.
  - CERN developing new TDC chip
    https://indico.cern.ch/event/366097/
    https://indico.cern.ch/event/548960/
    - 3ps time bins; overkill for Hyper-K.
    - 64 channels, ~600mW power.
- Need to ensure that TDCs can be adequately synchronized.

QTC evaluation board

- QTC evaulation board (2 QTCs = 6 ch inputs) was designed and fabricated (by FNAL/BU).
- This board will with FPGA board. Tests of the FPGA-TDC have been started.

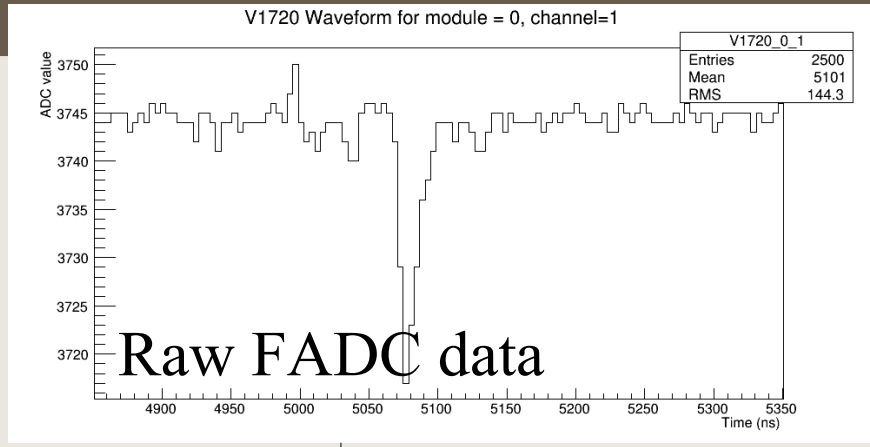


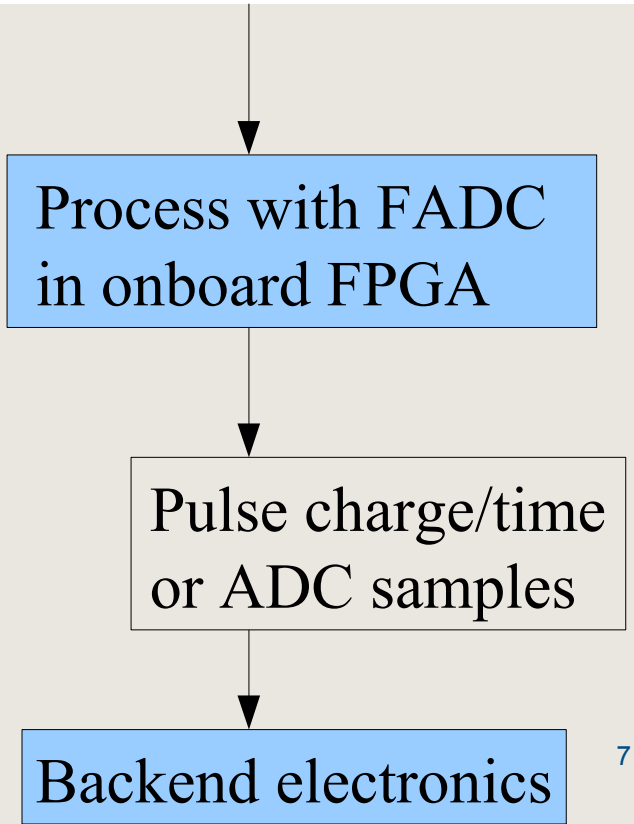




FADC Digitization

- Alternate proposal is to use FADC (Flash ADC) instead of TDC/ADC.
  - Something like 125-500 MHz sampling, 12-16 bit resolution.
- FADC data is continuously processed using FPGA on front-end board; firmware finds hits and only send pulse summary to backend.
  - Pulse summary is either just Q/T (for small pulses) or a set of ADC samples (for large pulses).





FADC Option - Overview

Pros

- More information on charge distribution 1us after first pulse.
- Can use firmware processing to subtract off periodic EMI noise.

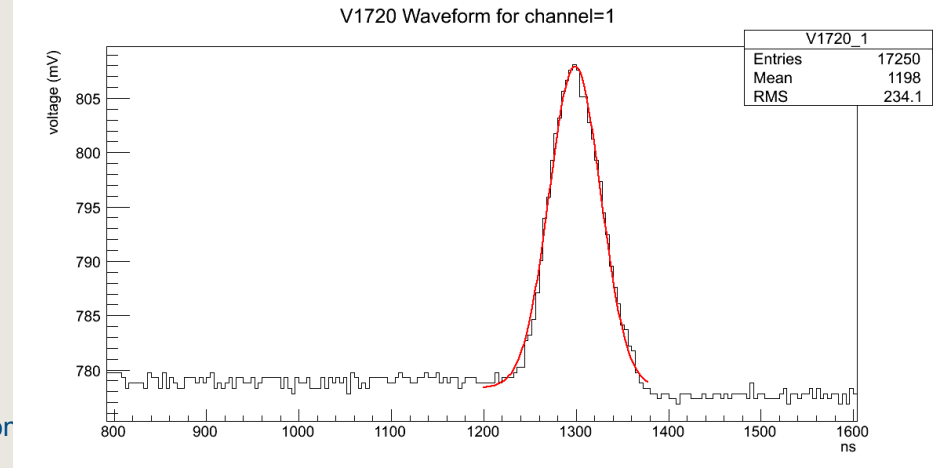
Cons:

- Higher power (?) and cost (?)
- More complex: pulse processing in firmware.
- Can we meet timing resolution + dynamic range requirements?

(reminder: 0.3ns resolution, 0.05-1250 PE range)
Focus of this talk is tests of timing resolution for different FADC designs.

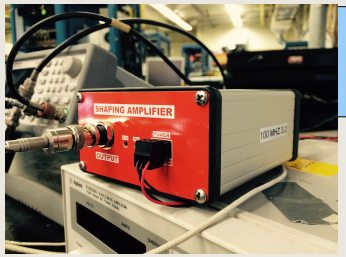
Time Measurements with digital waveform

- Extracting precise time from FADC pulse depends on many factors:
  - Low electronics noise
  - Optimal number of samples on leading and falling edge.
    - Need to shape pulse if not enough samples
  - Precision of ADC
    - Higher precision ADC (14 bit vs 12 bit) can help, but only if noise is small
  - Frequency of ADC
    - Faster ADC is better (but higher power, more expensive)



FADC Test Setup

- Use arbitrary waveform generator (AWG) to create input pulses.
  - AWG has negligible pulse jitter (unlike PMTs) so can probe directly the timing resolution of electronics.
- Shaper designed by Marcin Ziembicki, built at TRIUMF.
- Have on hand 100MHz, 250MHz and 500MHz digitizers.

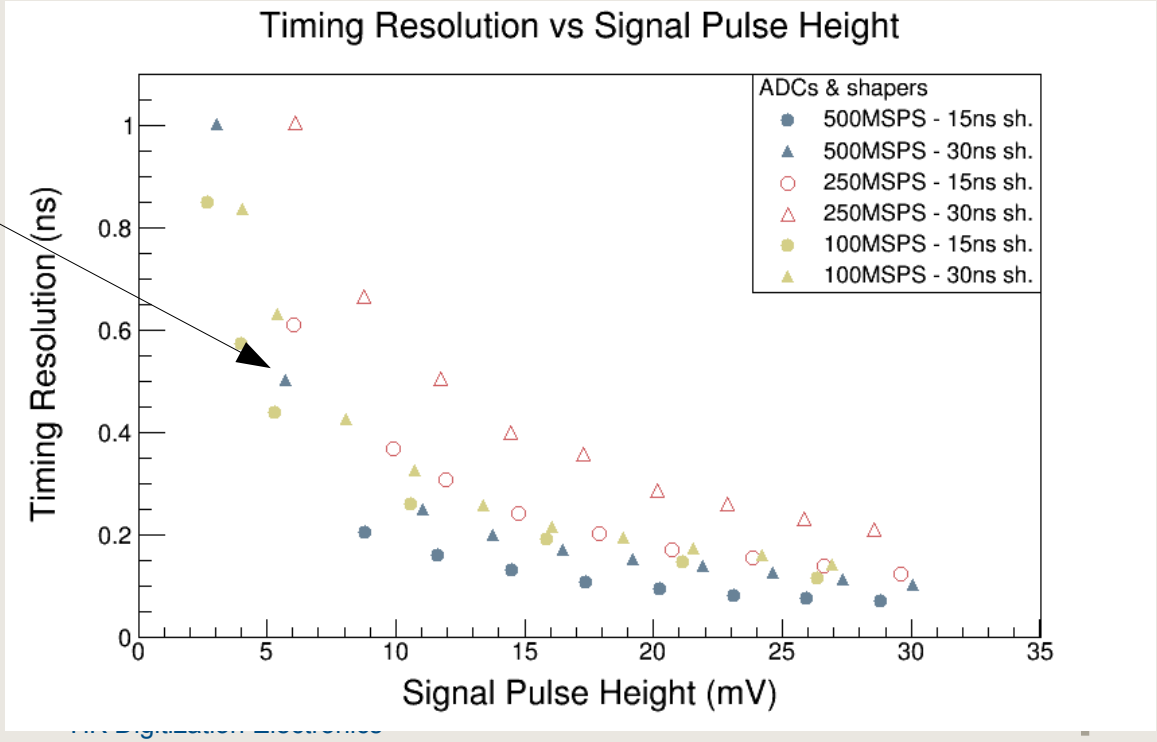


DT5724
100MHz

FADC Timing Results

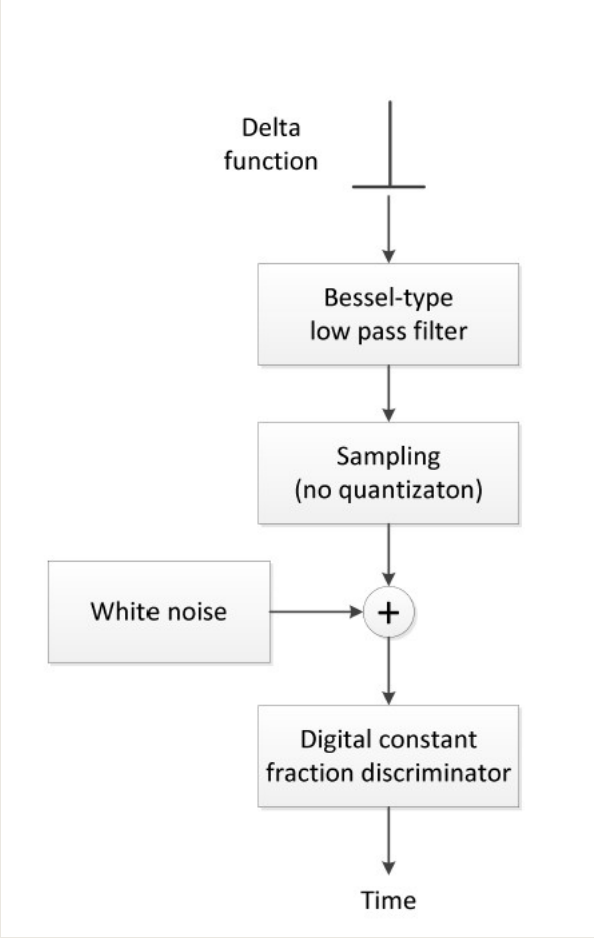
- Extract hit time with least square fit to waveform.
- Plot show timing resolution as function of pulse height, digitizer and shaper.
- Using 100MHz digitizer, could achieve 0.5ns timing resolution if we make 1PE pulse = ~5mV. Implies dynamic range of ~0-400PE.
- This is promising, though doesn't entirely satisfy dynamic range requirements (wanted 0-1250PE range).

100MHz digitizer would be cheaper and lower power than other FADC.



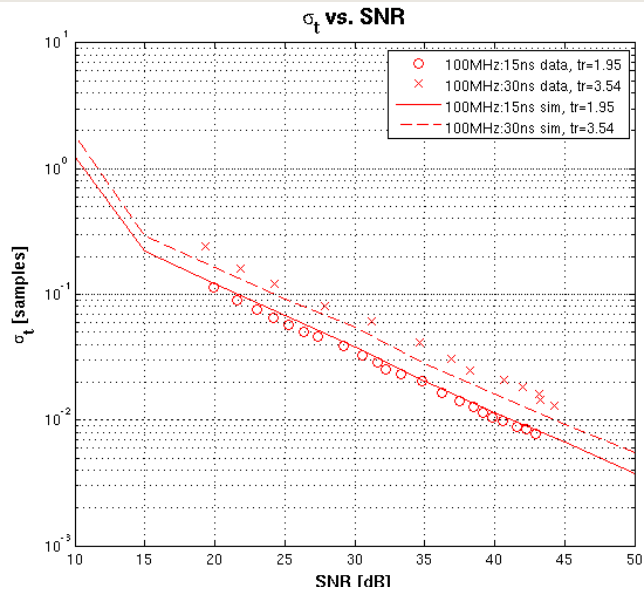
Simulation vs Data

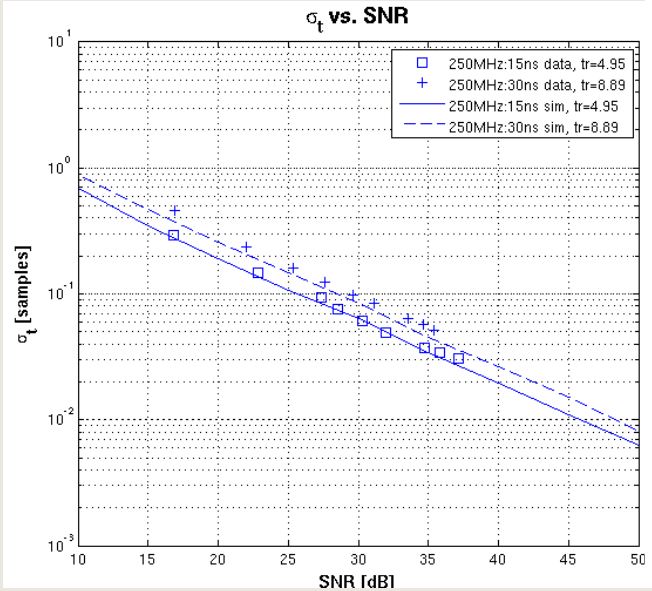
- Marcin Ziembicki did detailed simulation of expected timing resolution: SPICE + MATLAB. This allows:
  - Optimize ADC, signal shaping and signal processing
  - Determine minimum requirements for the system
  - Test various DSP methods for timing and charge estimation.
- Goal: develop and validate models of the electronics. With good models it is relatively easy to try multiple variants of the electronics.

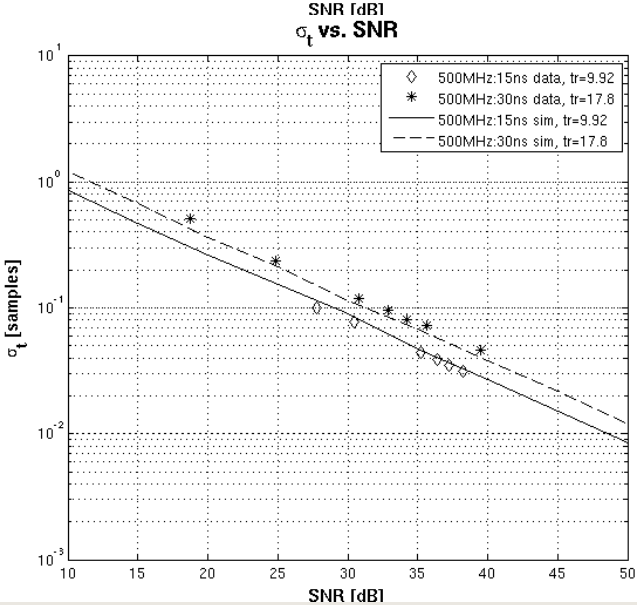


Simulated vs Measured Timing Resolution

- Plots show measured and simulated timing resolution for different digitizers, using fits to waveform.
- Agreement between data and model is pretty good.
  - So models can be used to guide further prototype development.



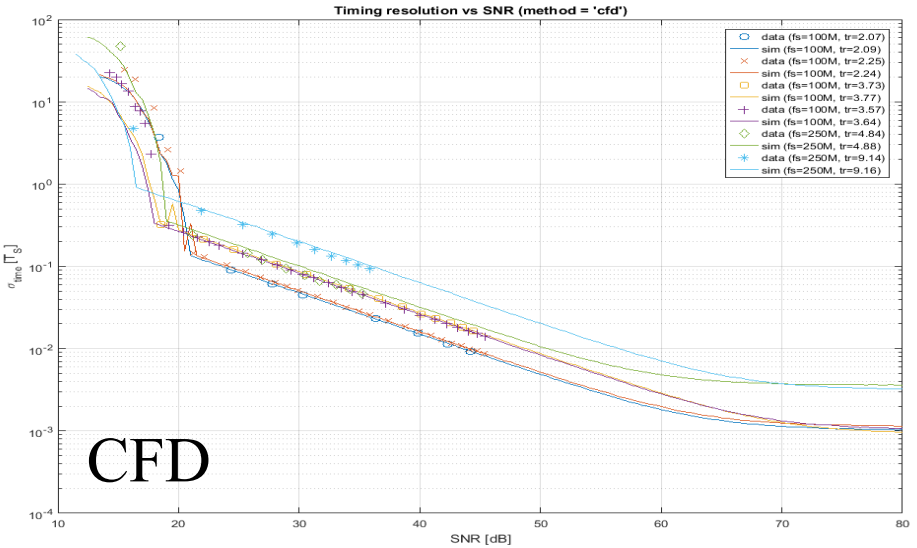


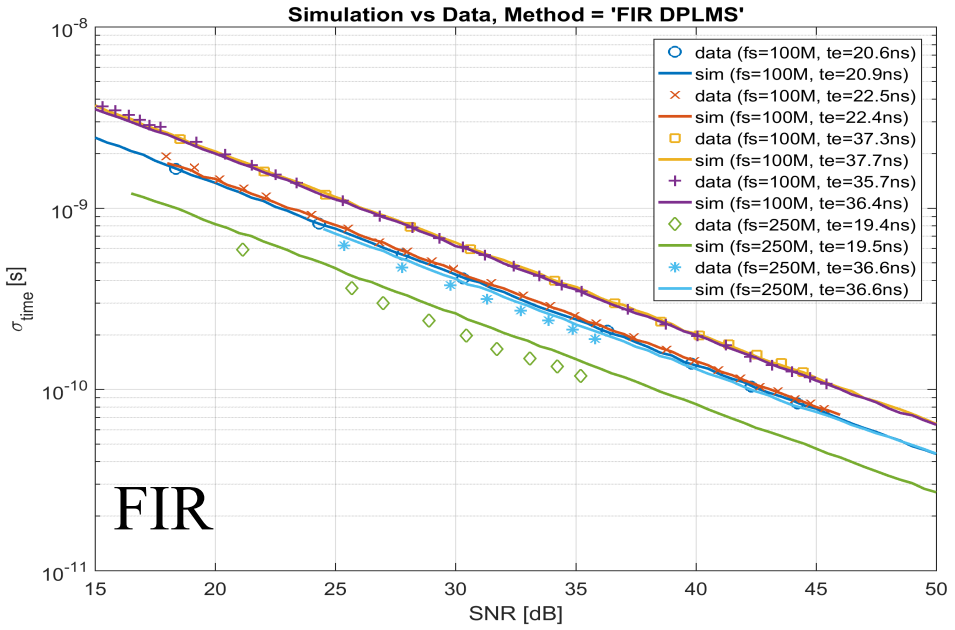


Note different axes;
- timing resolution of 0.1 in samples means 0.2 ns for the 500MHz digitizer.
- SNR is calculated using pulse height (for signal) and RMS of baseline (for noise)

Simulated vs Measured Timing Resolution

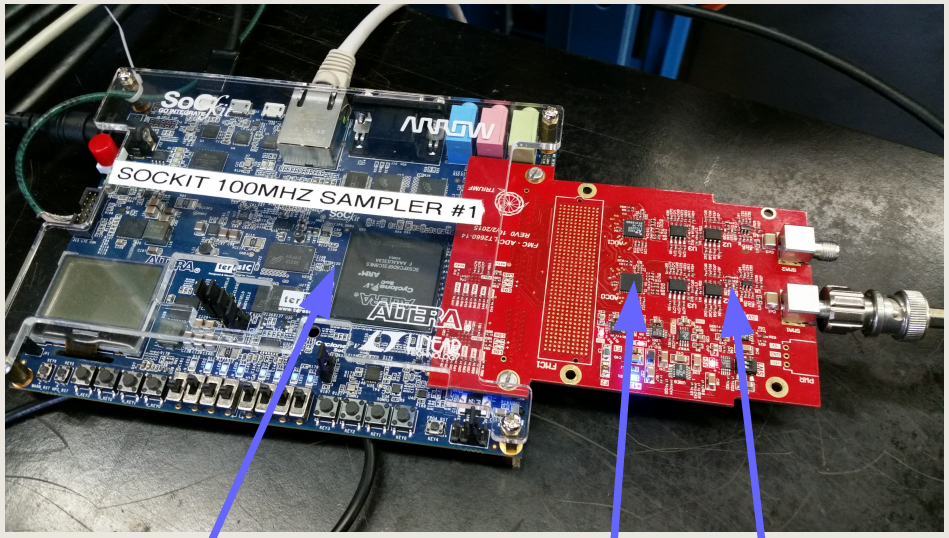
- Our models also seem to work for different time extraction.
  - Digital constant fraction discriminator
  - Finite impulse response filtering





100MSPS FADC prototype

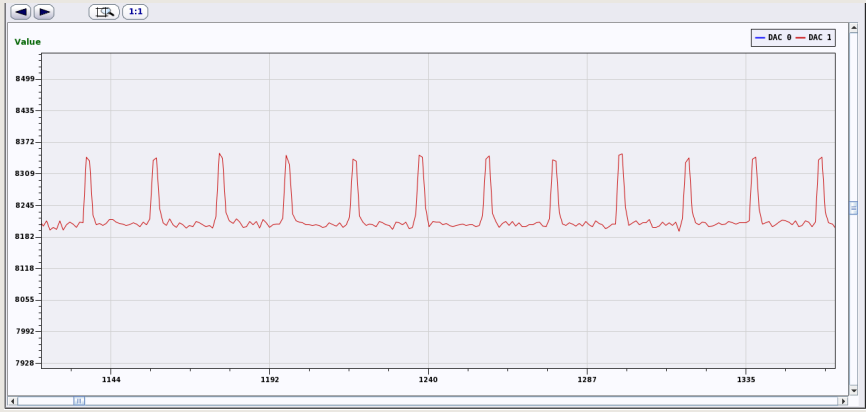
- Design/built version of the 100MSPS shaper + FADC prototype.
- This is low power FADC for HK 20” PMTs
  - This version uses 0.55W per channel (no FPGA included), but should be possible to get it down to 0.4W with better power rails.
- Will start analysis of this data soon.



Altera Cyclone V SoC evaluation card

LT2260 ADC

shaper



Sample waveform with periodic pulses

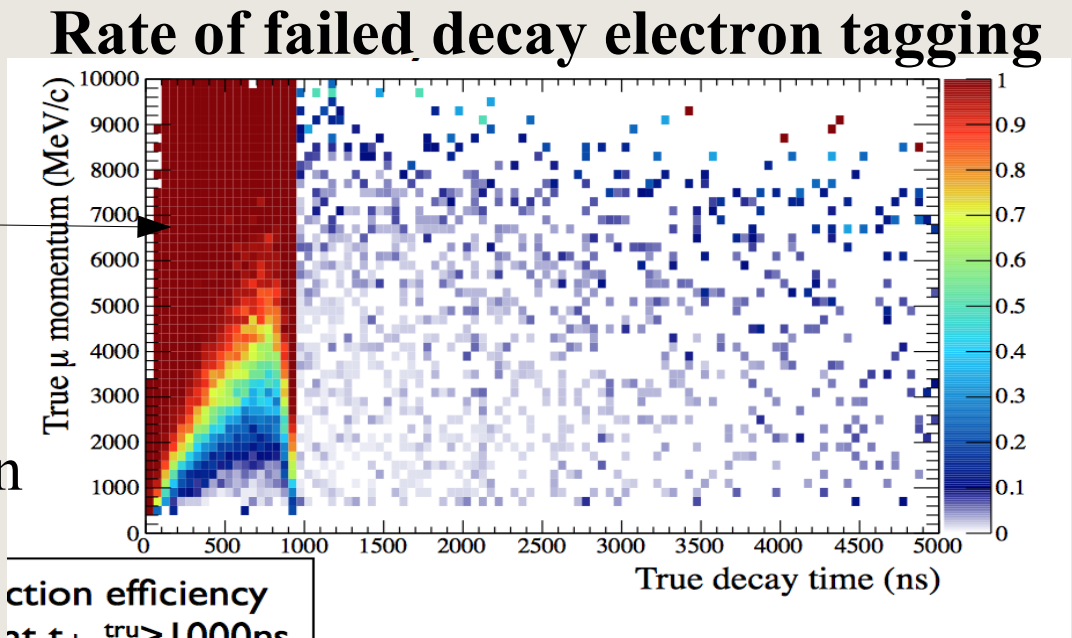
Cyclone V SoC = Cyclone V FPGA + Cortex-A9 ARM processor

Decay Electron Tagging

- One possible advantage of FADC digitization is better ability to tag decay electrons that occur at short decay times and high muon energies.
- S. Tobayama shows decay electron tagging for SKDetSim + fitqun
- Ongoing study to reproduce same plot for Hyper-K, then investigate benefits of different digitization schemes.

High failure rate
for high energy muons
-> kills most PMTs
for 1us

SKDetSim simulation
Of stopping muons

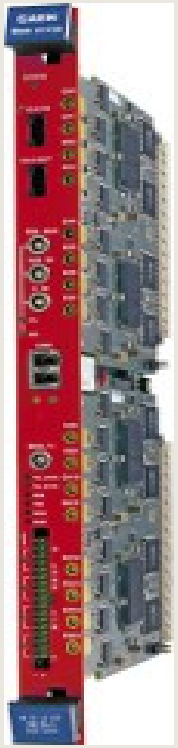


Conclusion / Future Work

- Work progressing on two digitization options.
- Default plan of using QTC+TDC has QTC prototype board.
  - New QTC board works.
  - FGPA-TDC development in progess
- Alternate scheme of continuous FADC digitization
  - 100MSPS prototype board being tested now.

Backup

CAEN Digitizers



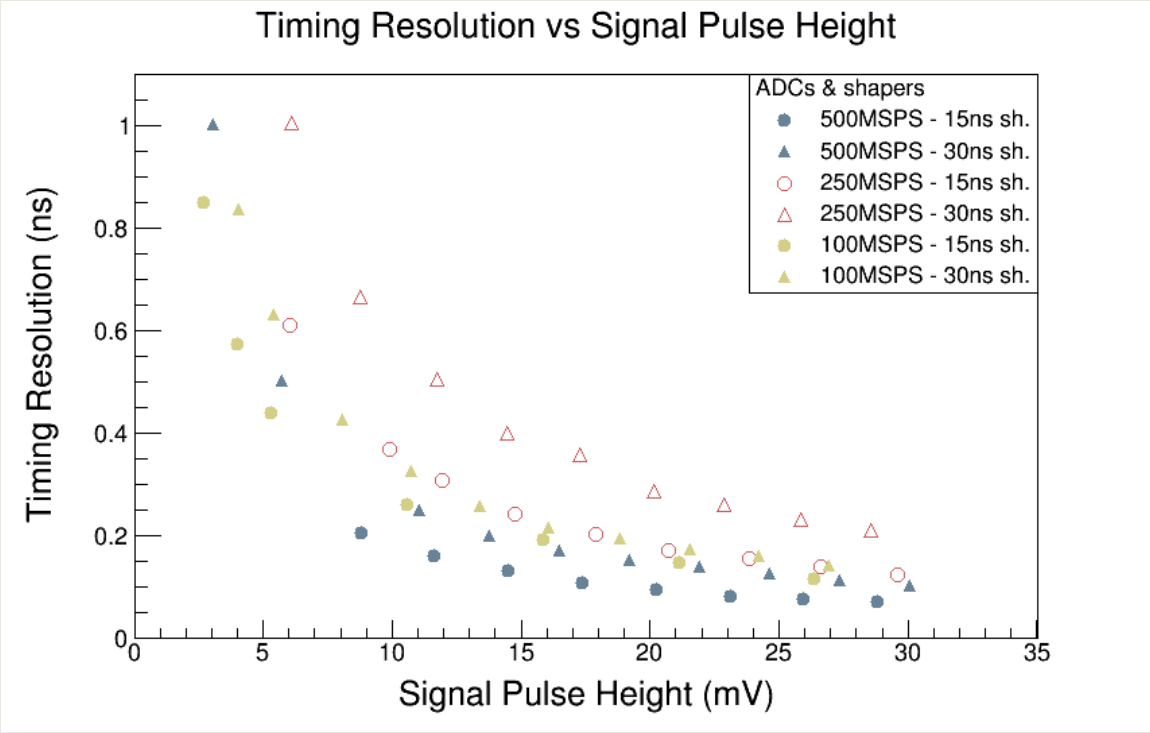
V1730
500MHz

V1720
250MHz

DT5724
100MHz

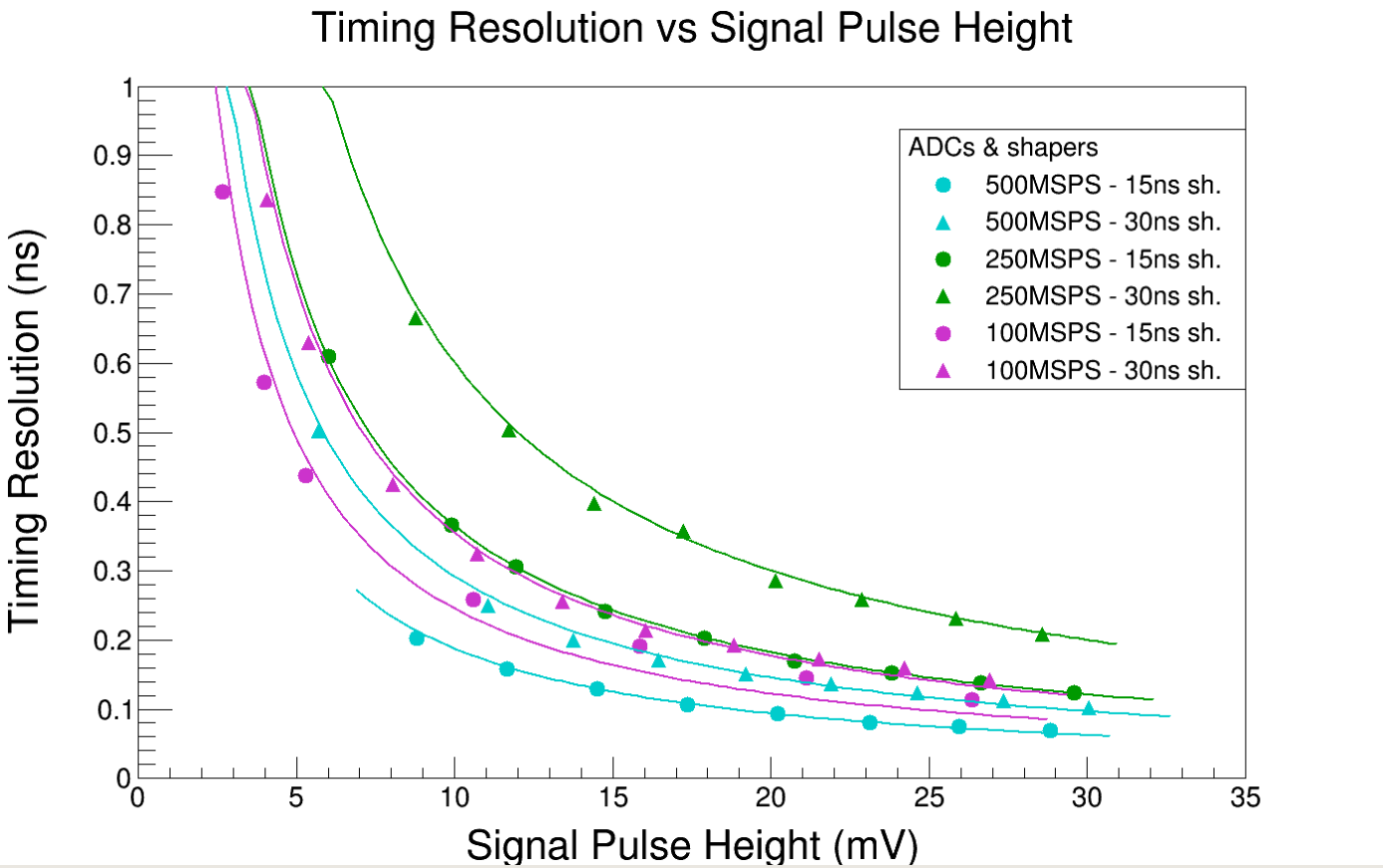
FADC Timing Results

- Plot show timing resolution as function of pulse height, digitizer and shaper.
- 250MSPS digitizer is 12 bit ADC (and lower ENOB), whereas 100MSPS and 500MSPS are 14bit ADCs.



Timing Resolution Functional Form

- Timing resolution vs pulse height follows 1/x curve, as expected.



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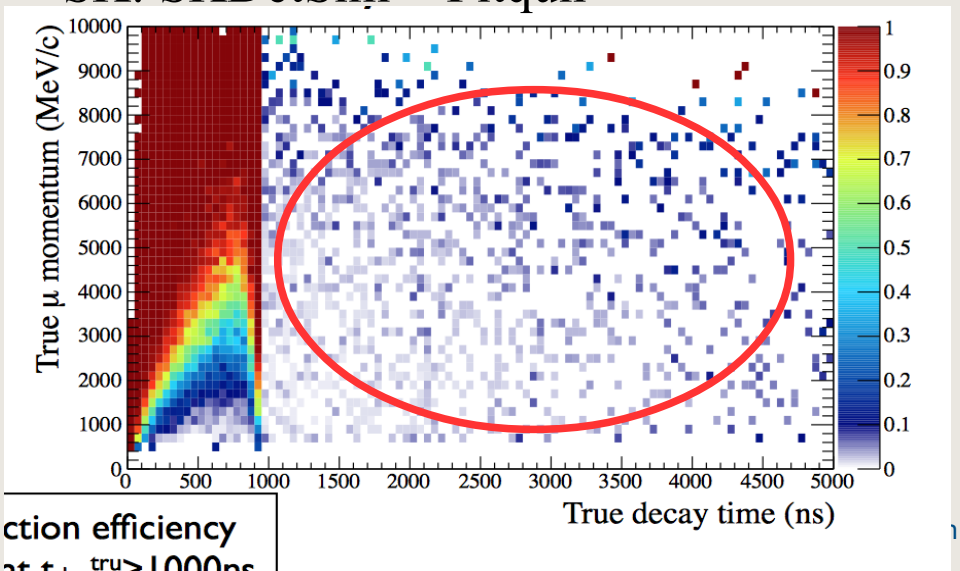
Decay Electron Tagging Study

- Using new baseline HK geometry, WCSim 1.4 and fitqun
- Some clear problems; much higher rate of failures to find decay electron for >1us decay times.
- Needs more work...

SK: SKDetSim + Fitqun



Hyper-K: WCSim + Fitqun