OMEGA readout chips for neutrino experiments

Selma CONFORTI, Frederic DULUCQ, Christophe de LA TAILLE,
Gisèle MARTIN-CHASSARD

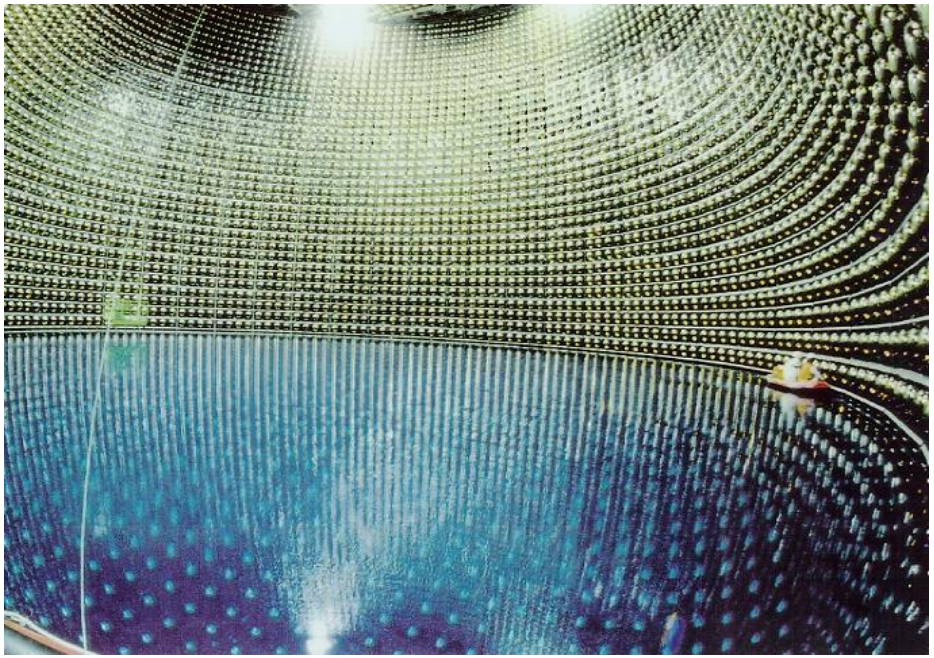
OMEGA microelectronics group
Ecole Polytechnique & CNRS IN2P3
http://omega.in2p3.fr

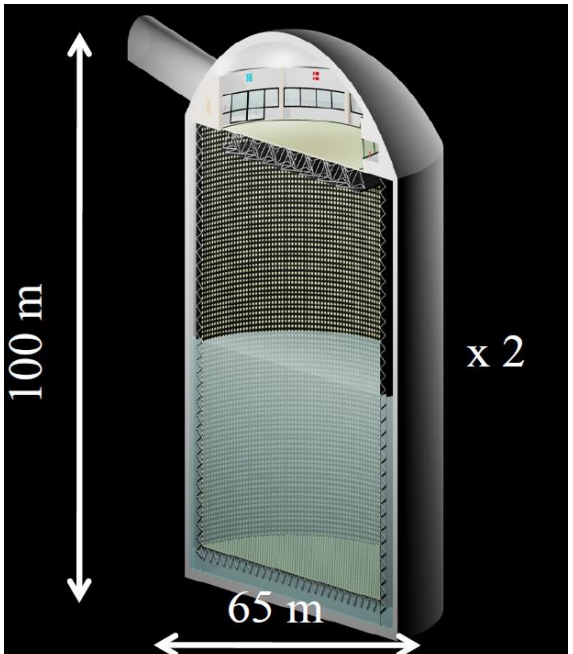
weeroc

Organization for Micro-Electronics desiGn and Applications

Introduction

- New constraints with ever larger detectors
  - Cost
  - Simplicity
  - Power dissipation
  - Harsh environment
  - Reliability
- Large area detectors
  - PMTs, MCP, RPCs…
- Performance
  - Sub-ns timing
  - Charge measurement
  - Cryogenic operation





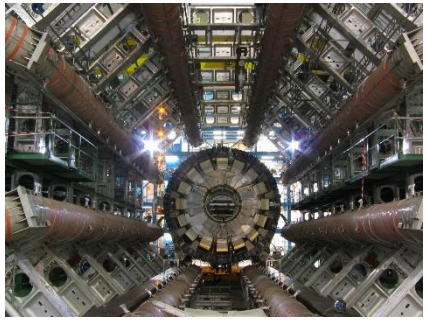
Readout electronics

- Waveform digitizers
  - ~1 GHz analog bandwidth, 1-10 GS/s
  - Detailed waveform, allows digital processing
  - Lots of data, power hungry
  - Examples : SAM, DRS4, PECS4…

- Dedicated ASICs
  - GHz bandwidth amplifiers/discriminators
  - High speed TDCs (CERN, IPNL…)
  - Measure time and/or charge
  - Low power ~mW/ch
  - Examples : NINO, PETA4, PETIROC…

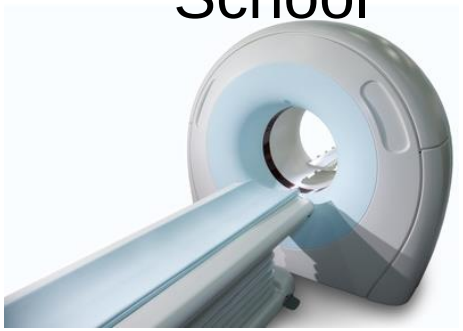
Omega microelectronics lab

- Mutualized ASIC design team created in 2006, UMS in 2013
- 10 research engineers (3 IR0, 6 IR2, 2 AI)
- Importance of critical mass for more and more complex circuits
- Cross-fertilization between projects
- Projets selection by IN2P3 management
- Technology transfer via startup WEEROC



Research, Institute

Education, School



Industry, company

OMEGA ROC chips

- Use of Silicon Germanium 0.35 µm BiCMOS technology since 2004
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

Chip	detector	ch	DR (C)
MAROC	PMT	64	-2f-50p
SPIROC	SiPM	36	+10f-200p
SKIROC	Si	64	+0.3f-10p
HARDROC	RPC	64	-2f-10p
PARISROC	PM	16	-5f-50p
SPACIROC	PMT	64	-5f-15p
MICROROC	µMegas	64	-0.2f-0.5p
CATIROC	PM	16	50fC-300pC

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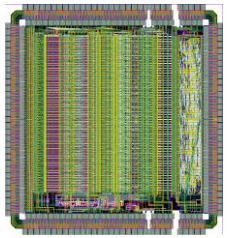
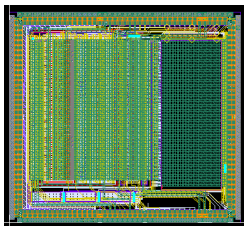
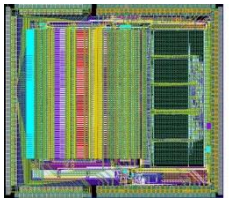
MAROC3



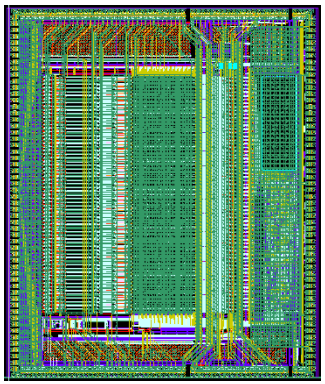
HARDROC2



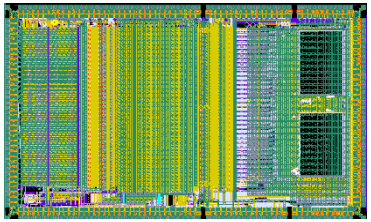
MICROROC1



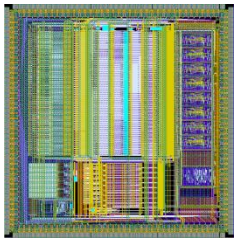
SKIROC2



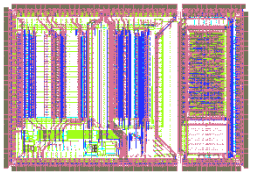
SPIROC2



SPACIROC

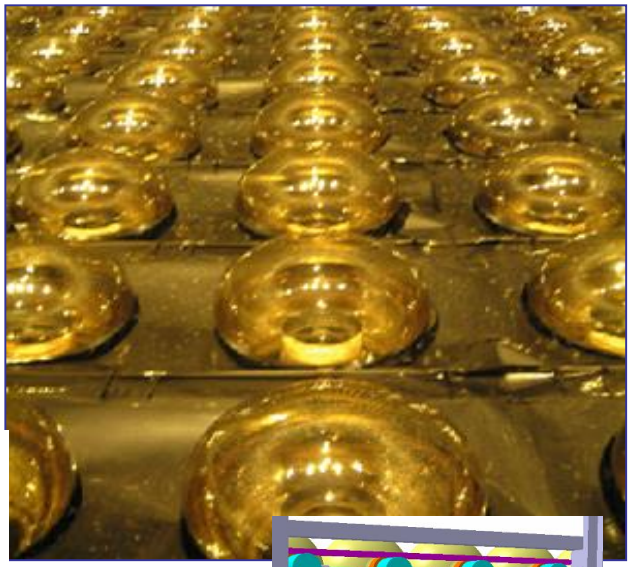


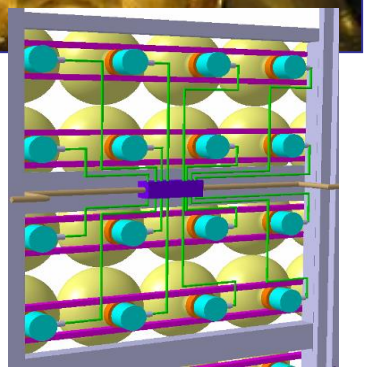
PARISROC2

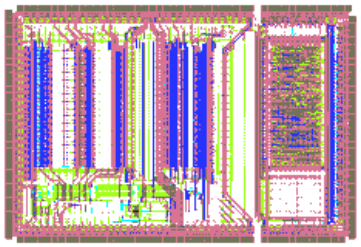


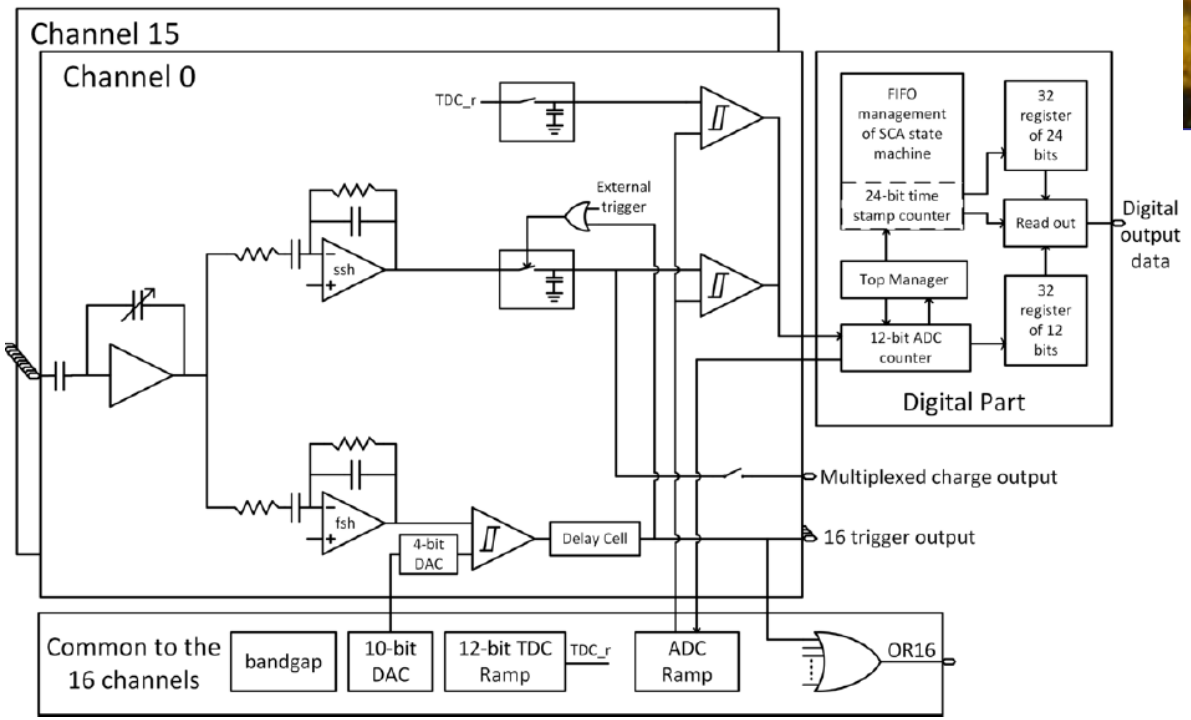
PARiSROC for PMm²

- Photomultiplier ARray Integrated SiGe ROC
  - « Large area PMT array » with centralized ASIC
  - Auto-trigger at 1/3 p.e.
  - Charge and time measurement (10-12 bits)
  - Data driven : « One cheap wire out »

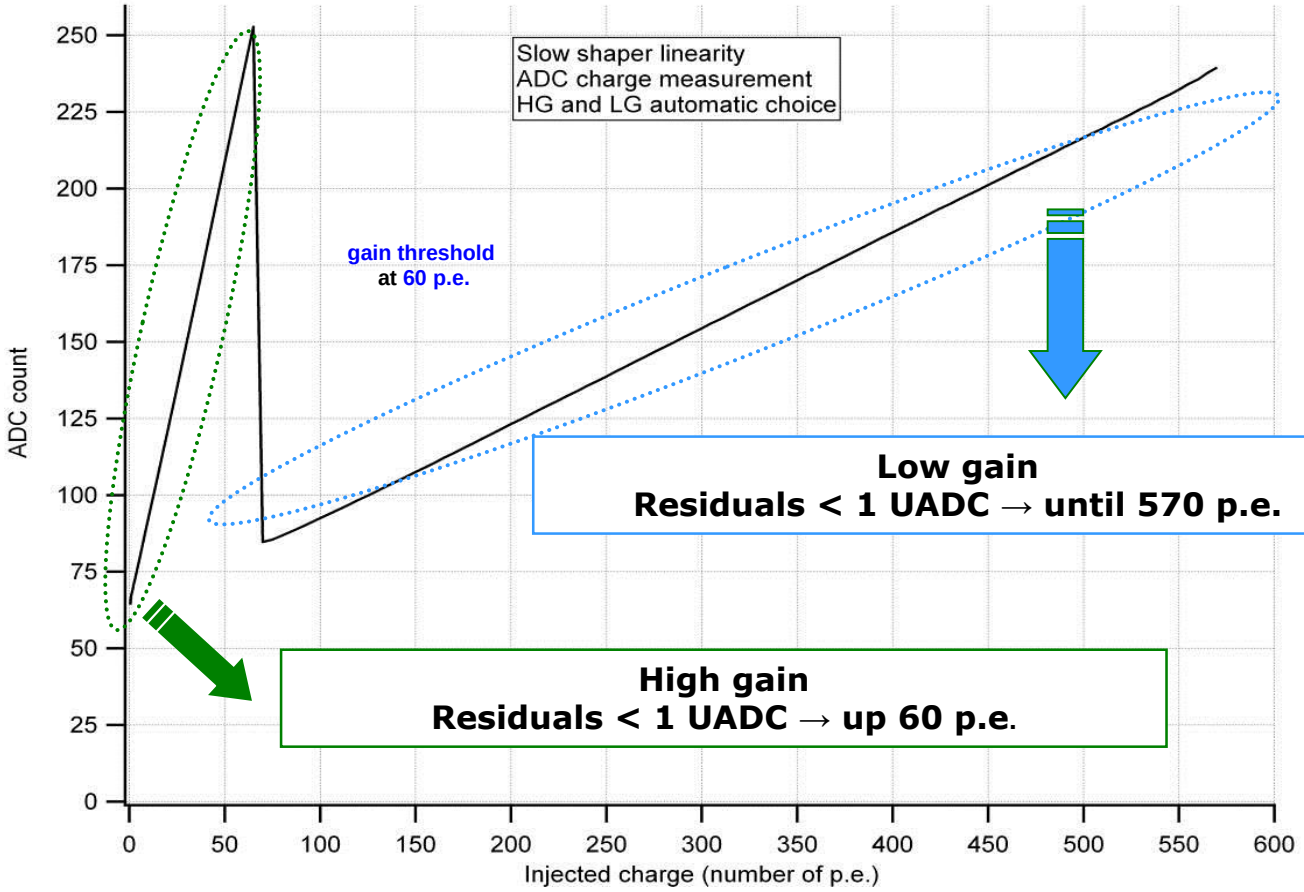


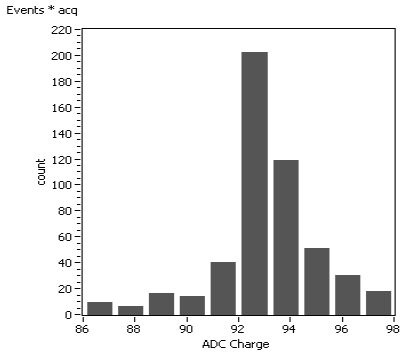






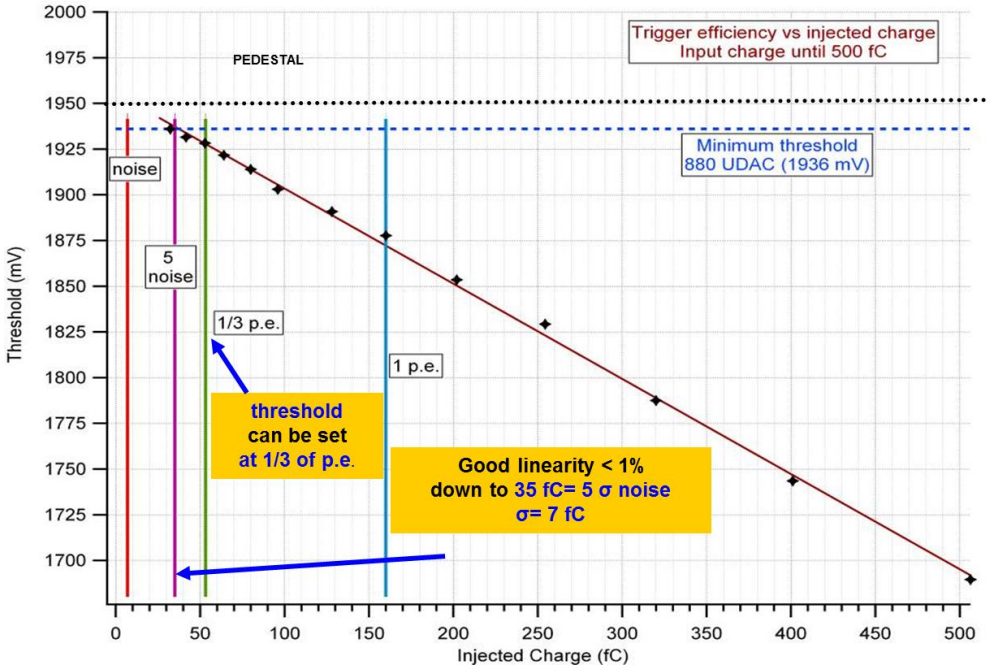
Charge measurement

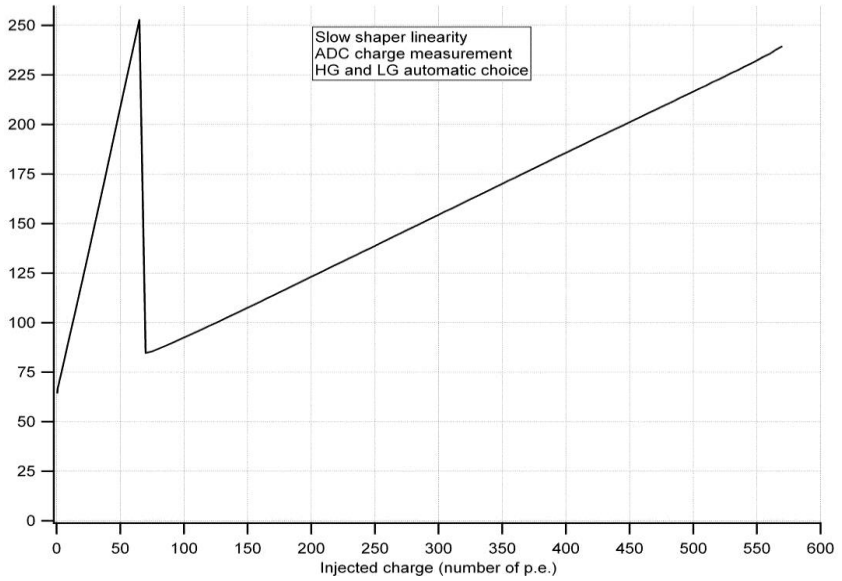


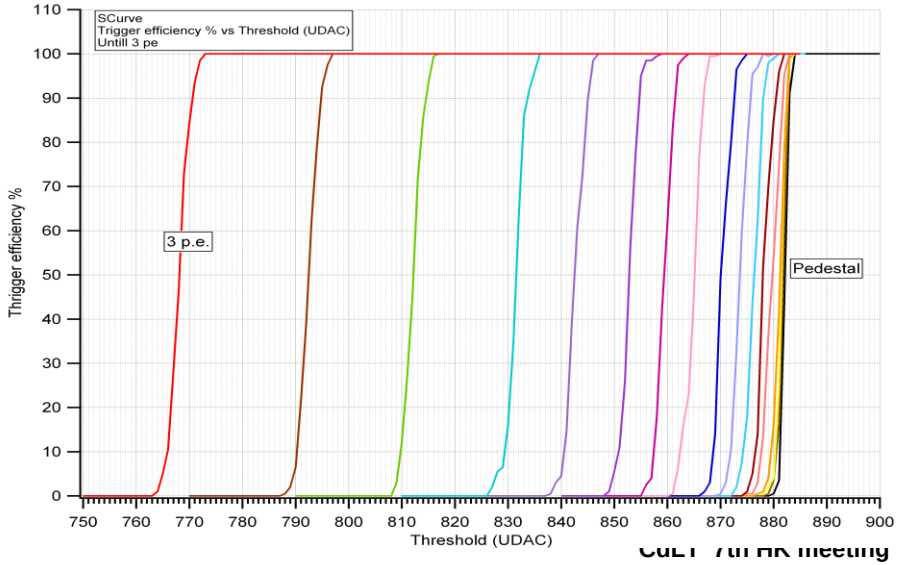


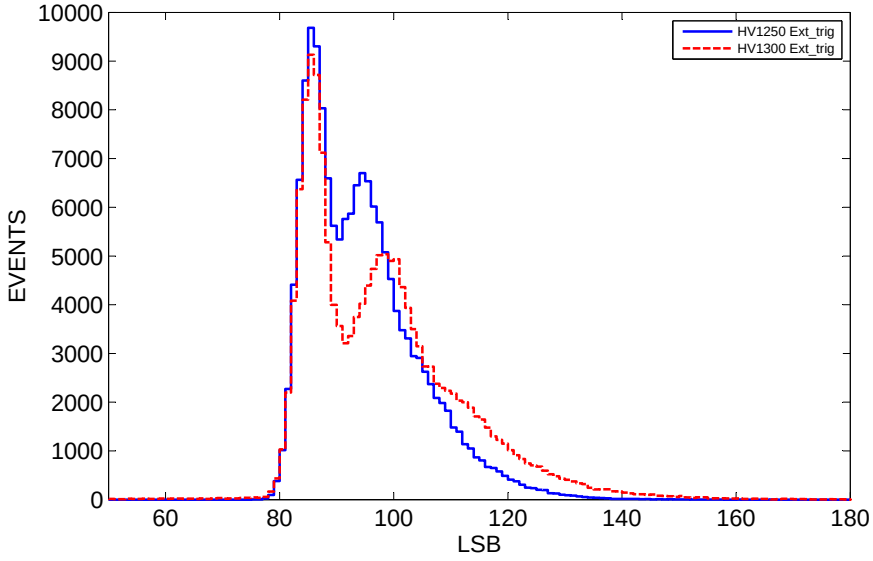
1 pe charge measurement by 10-bit ADC
Average= 93.02 UADC,
sigma= 2.02 UADC,
range= 12UADC.

Performance



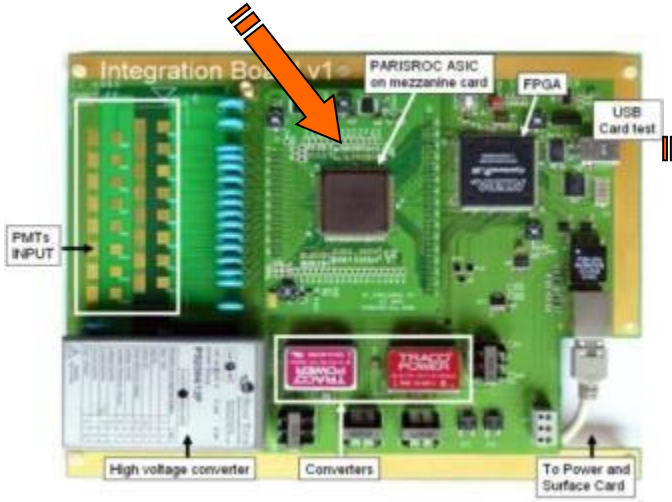






PMm² demonstrator

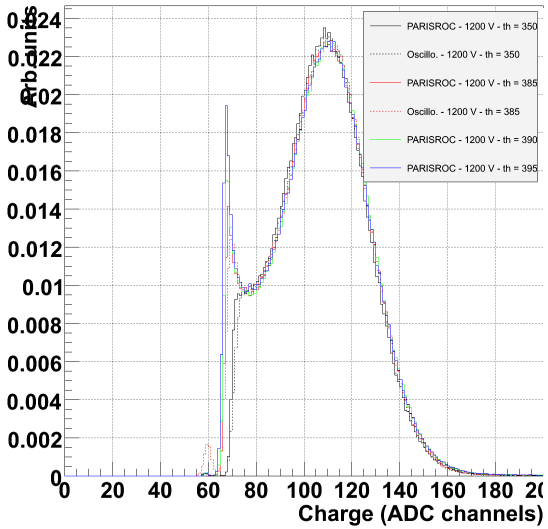
PARISROC2 chip



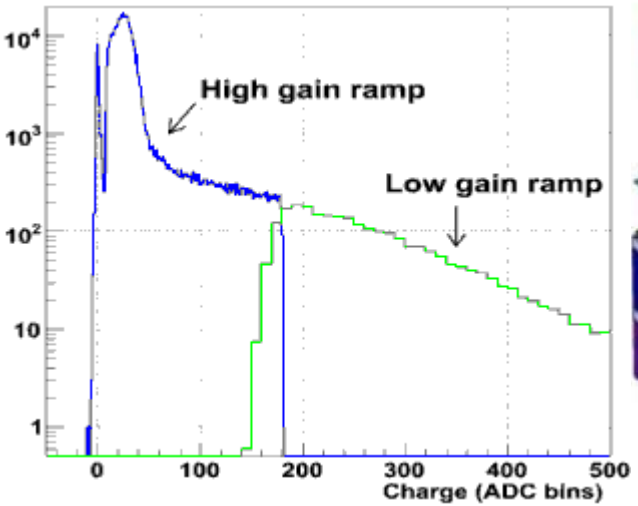
Watertight box

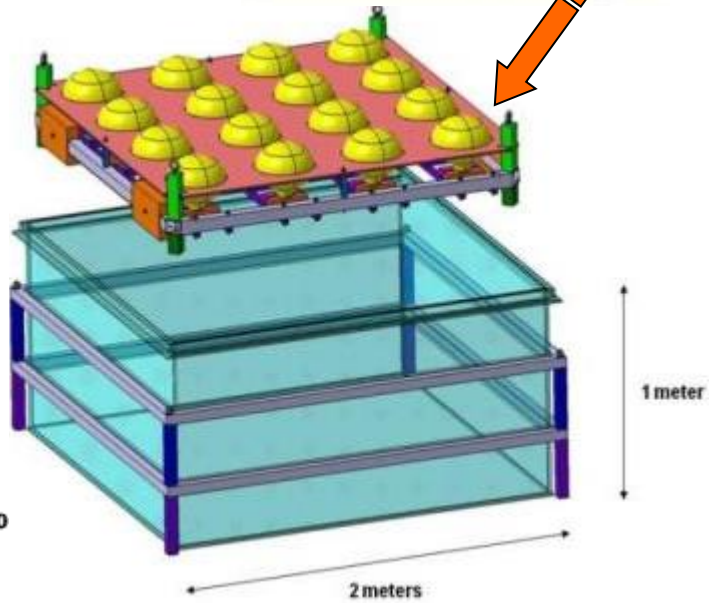
2m x 2m array

1-in (XP3102) single p.e. noise spectrum.



8-in (Hamamatsu R5912)
Single p.e. noise spectrum.

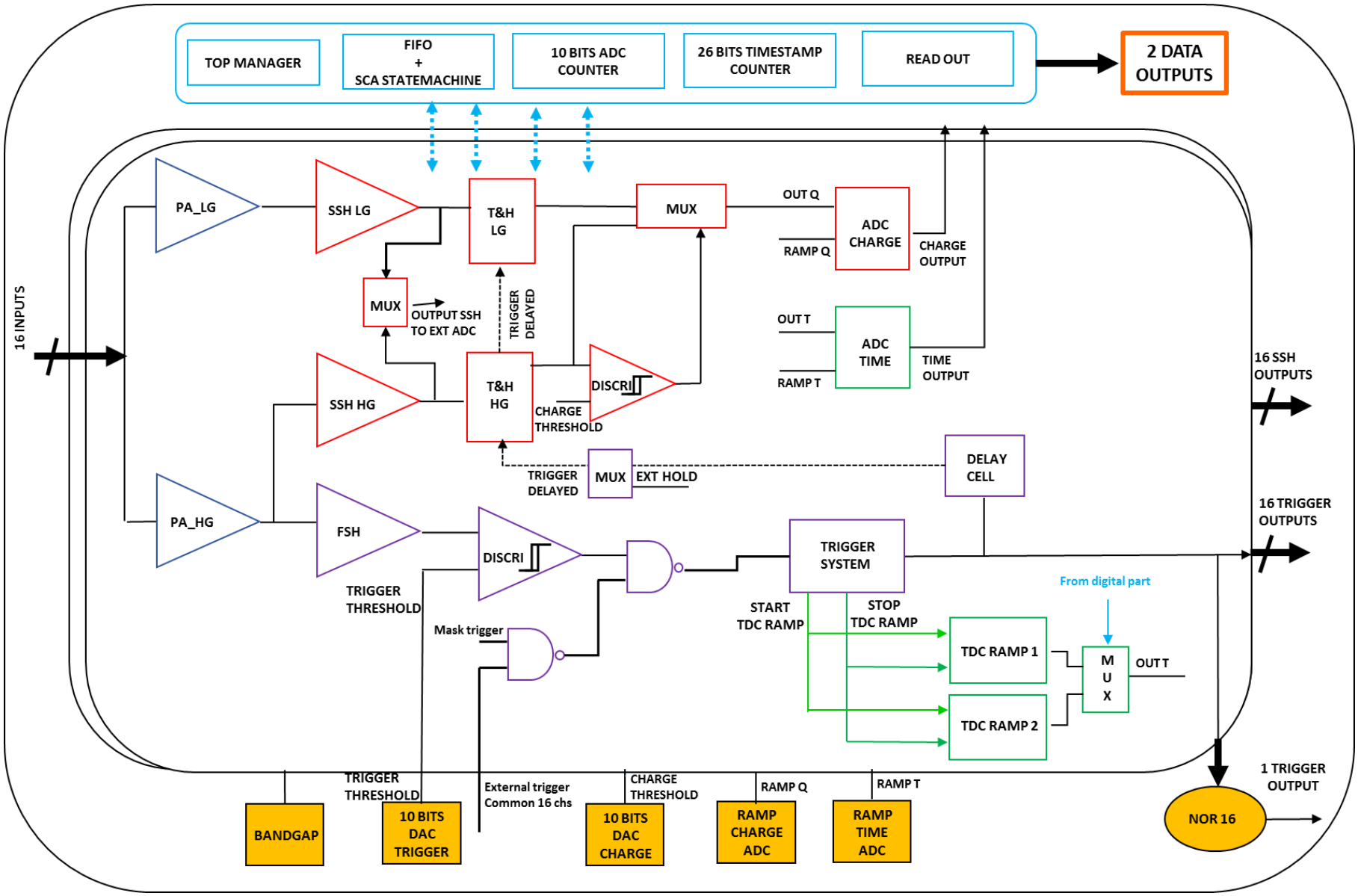




Successor : CATIROC

Detector Read-Out	PMTs
Number of Channels	16
Signal Polarity	negative
Sensitivity	voltage
Timing	**Time stamp: 26 bits counter @ 40 MHz** **Fine time**: resolution < 100 ps (simulation) **A TDC ramp for each channel**
Charge Dynamic Range	160 fC up to 100pC
Trigger	**Triggerless acquisition** Noise= 5 fC; Minimum threshold= 25 fC (5σ)
Digital	**Conversion: 10 bits** ADC at **160 MHz** **Two Read out: 80 MHz** Read out frame: **50 bits** 2 frames of (29+21) bits 1st frame/8chs: Ch nb= 3; coarse time= 26 2nd frame/8chs: Gain used= 1; Charge converted= 10, Fine time converted= 10
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) die : 3.3 mm x 4 mm
Power Consumption	30 mW/channel
Outputs	16 trigger outputs NOR16 16 slow shaper outputs Charge measurement over 10 bits Time measurement over 10 bits
Main Internal Programmable Features	Variable preamplifier gain Shaping time of the charge shaper (variable shaping and gain) Common trigger threshold adjustment Common gain threshold adjustment

CATIROC schematic

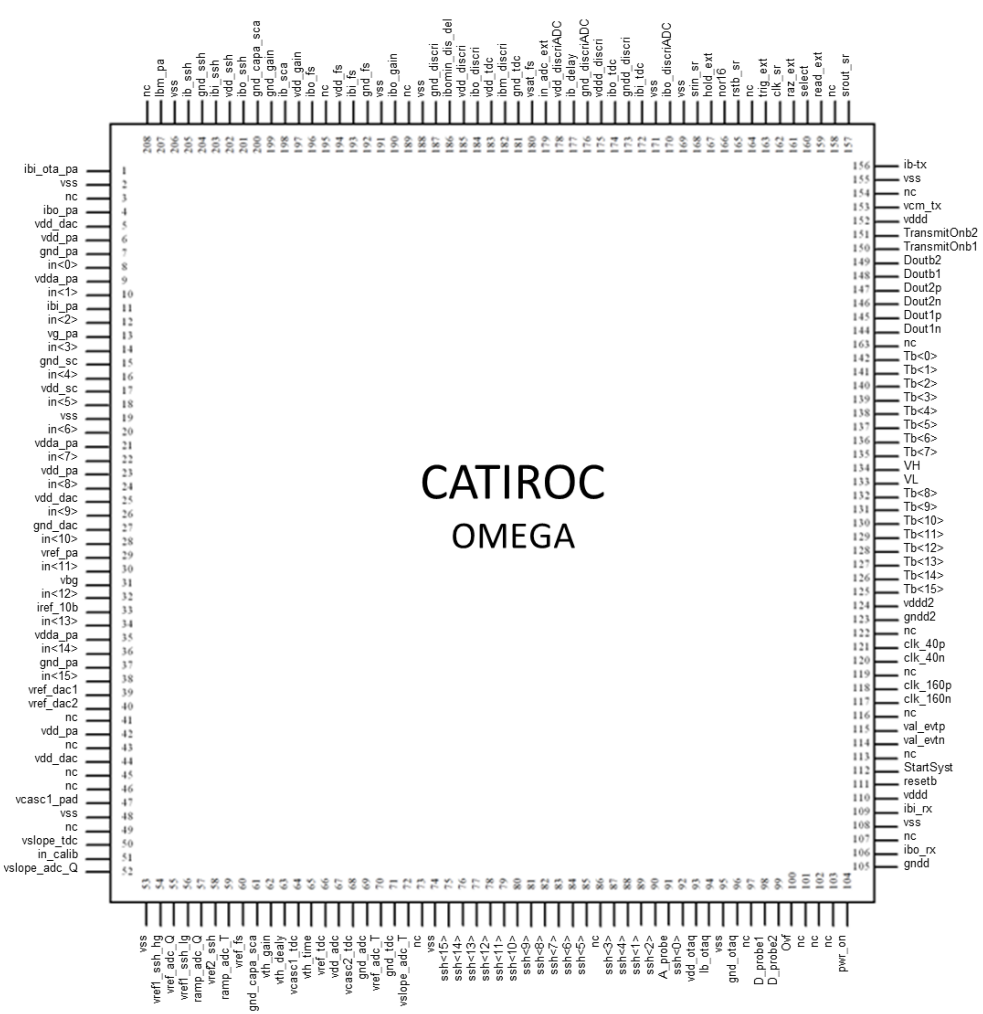


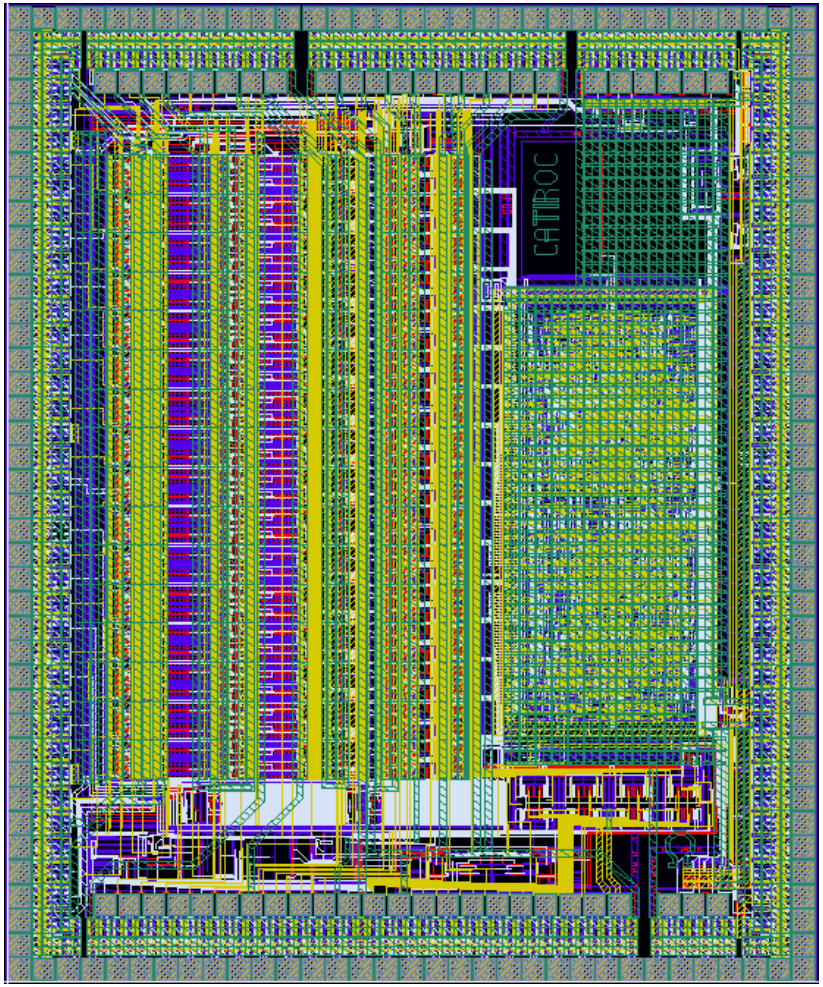
CATIROC overwiev

Technology: **AMS SiGe 0.35 µm**

Surface: **13.2 mm²**

Package: **TQFP208**



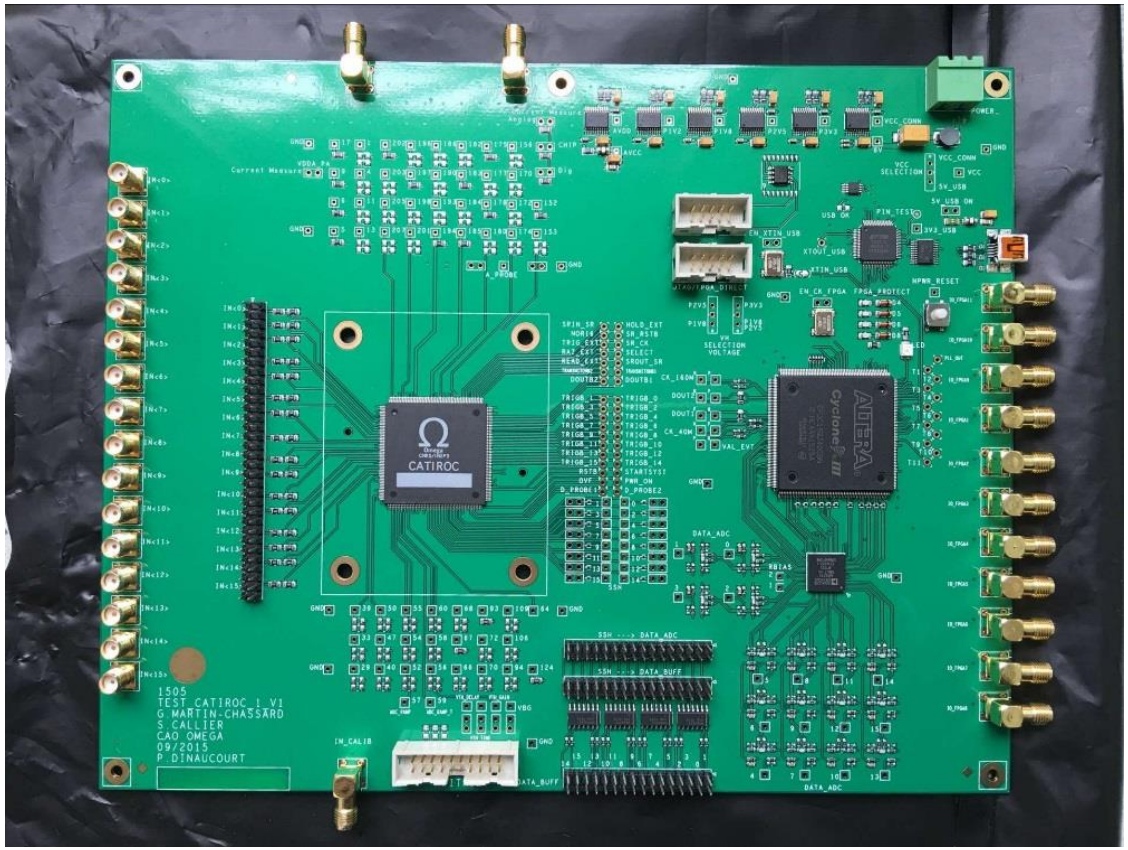


CATIROC Test Board

Test Board with:

- 16 SMA connector input
- ASIC test pins
- 16 trigger outputs
- 16 ssh outputs
- An external 14-bit 16 channel ADC (ANALOG DEVICES)
- An FPGA Cyclone3
- USB interface
- Power supply
- ASIC CATIROC:
  - 328 slow control bits
  - Various digital signals

Test started in January



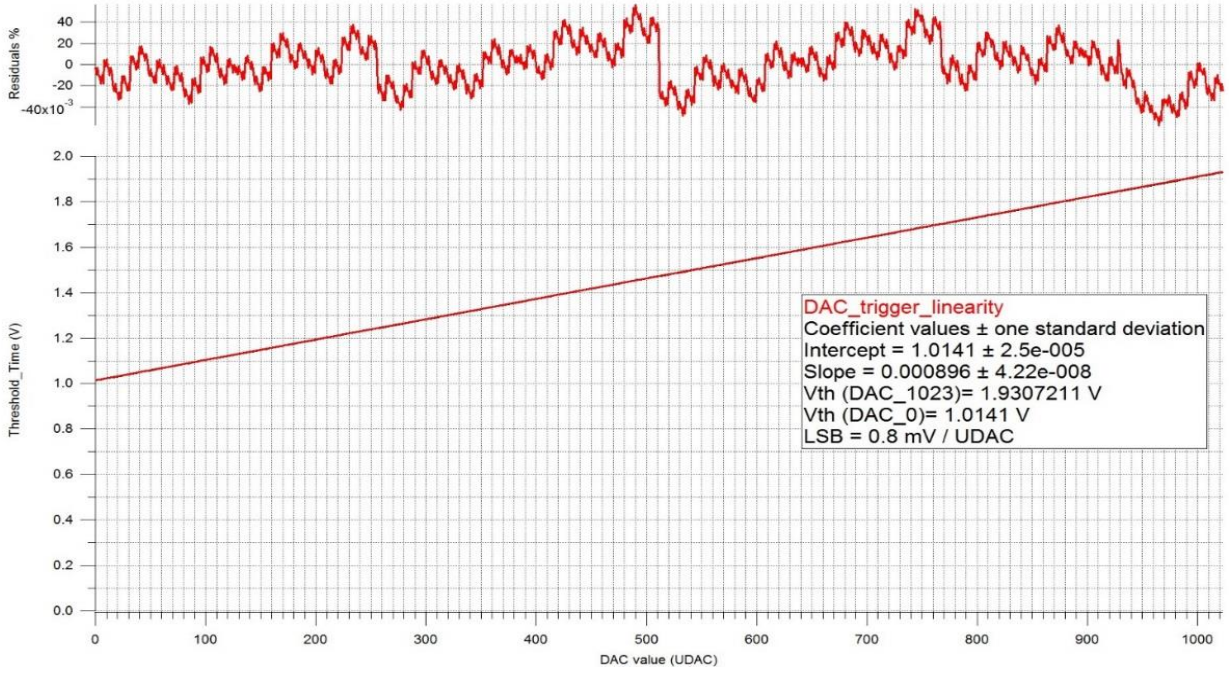
CATIROC measurements

General test:

- power dissipation per channel : 10 mW WC +25 mW ext ADC drivers
- Analog signals:

	V_{max} (at 160 fC)	V_{max} (at 1.6 pC)	Rms_noise	SNR	T_{peak}	T_{tot}
Preamplifier HG	10 mV		550 µV	18		
Preamplifier LG		11 mV	410 µV			
Slow Shaper HG	14 mV		1 mV	14	33 ns	400 ns
Slow Shaper LG		14 mV	670 µV		33 ns	400 ns
Fast Shaper	-75 mV		2.3 mV	33		

- DAC linearity:

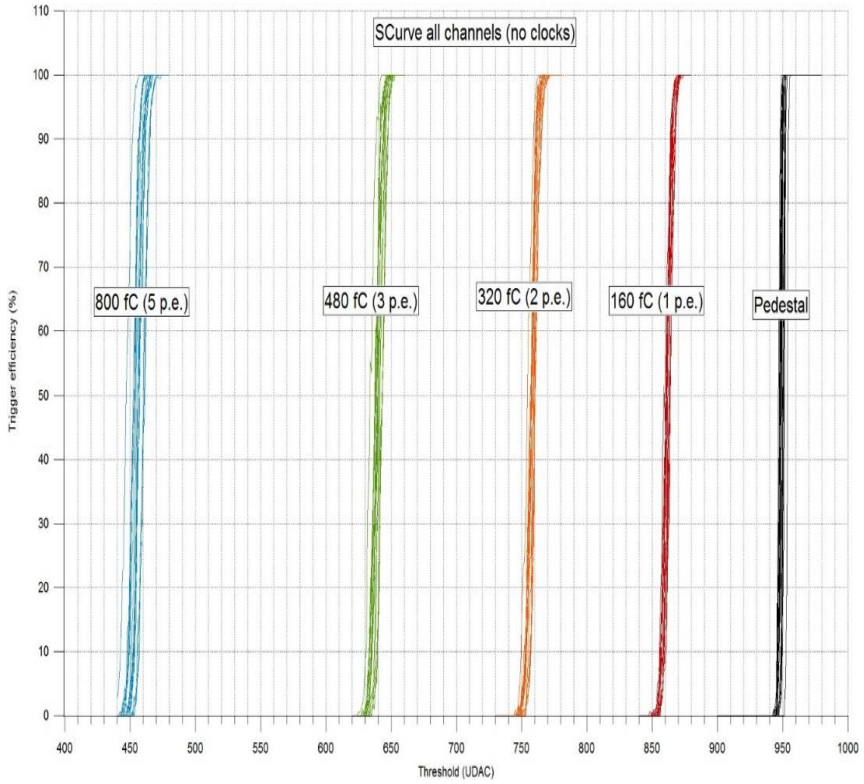


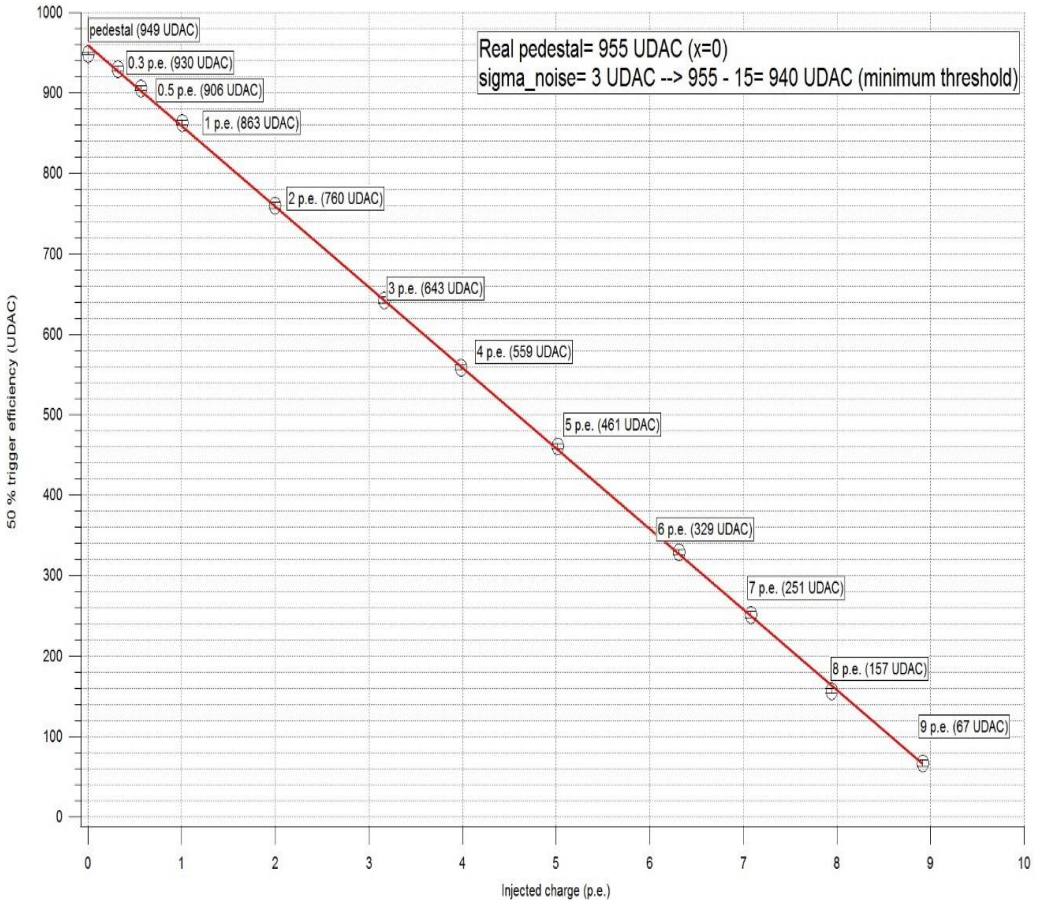
SCurve

- S curve : trigger efficiency versus threshold at various injected charges

For every channel of Catiroc

- S curve : 50 % trigger efficiency versus injected charge for channel 0

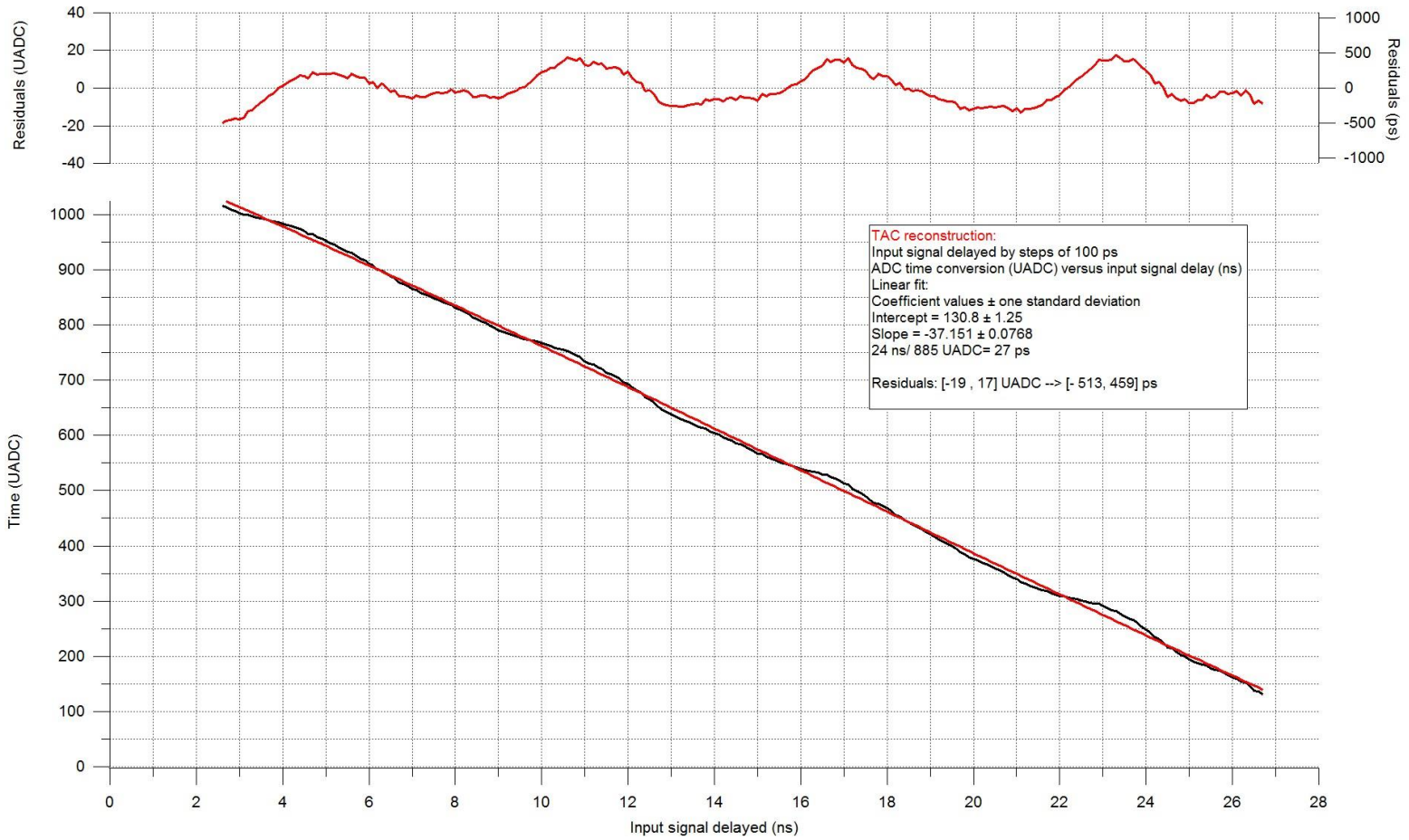




TAC

- 160MHz clock seen on the TDC (residuals)
- Rms of the histogram of the residuals: 2.7 ADC Unit

⇒ Time resolution: 2.7x27ps (step)= 73 ps rms



Conclusions

- CATIROC produced in 2015
- New generation ROC
  - Auto-triggered
  - Single photoelectron sensitive
  - Charge up to ~100 pe
  - Time to a few hundreds ps
  - 16 independant channels
  - Data driven
- Good candidate for JUNO SPMT

OMEGA ROCs

http://omega.in2p3.fr/ http://www.weeroc.com/

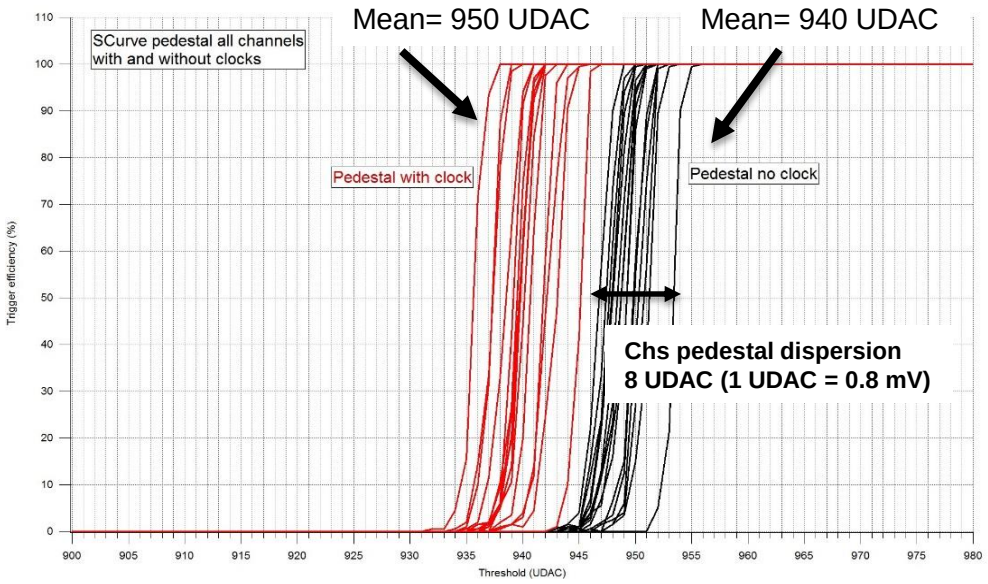
Chip	Detector	Ch	Polarity	Dyn Range	Specificities
MAROC	PM	64	<0	5 fC - 5 pC	64 trig outputs, internal 8/10/12-bit ADC (for charge measurment)
SPACIROC	PM	64	<0	2 pC- 220 pC	Fast photon counting (50MHz)
PARISROC	PM	16	<0	50 fC - 100 pC	Internal TDC (<1ns), 16 trig outputs
HARDROC	RPC	64	<0	2 fC - 10 pC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
MICROROC	µMEGAS/GEM	64	<0	0.2 fC - 500 fC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
SKIROC	Si pin diodes	64	>0	0.3 f C - 10 pC	Internal 12-bit ADC for charge measurement
SPIROC	SiPM	36	>0	10 fC - 300 pC	36 HV SiPM tuning (8 bits), Internal 12-bit ADC for charge and time measurement
EASIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	<0	100fC – 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)
TRIROC	SiPM	64	Both	100 fC- 300 pC	64 HV SiPM tuning (8 bits), 64 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)

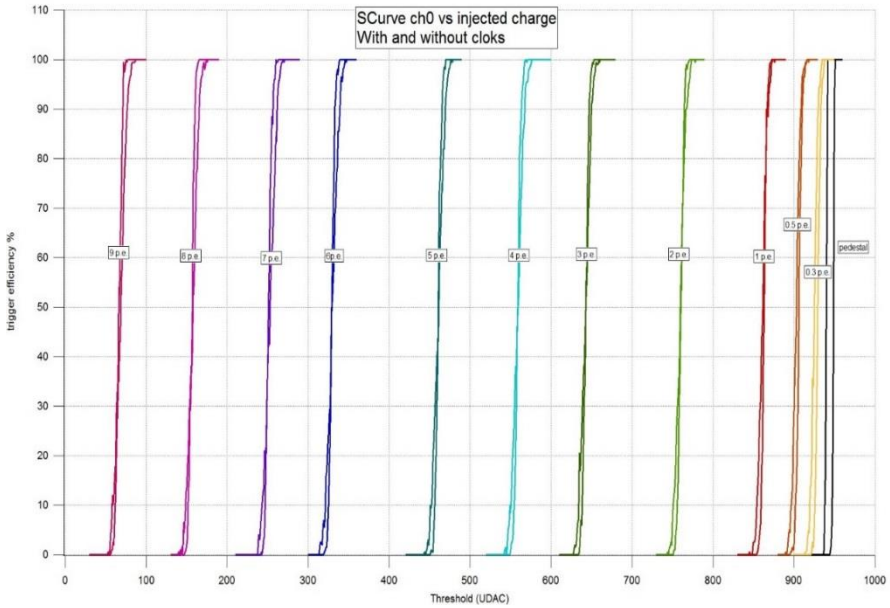
SCurve

- S curve : trigger efficiency versus threshold

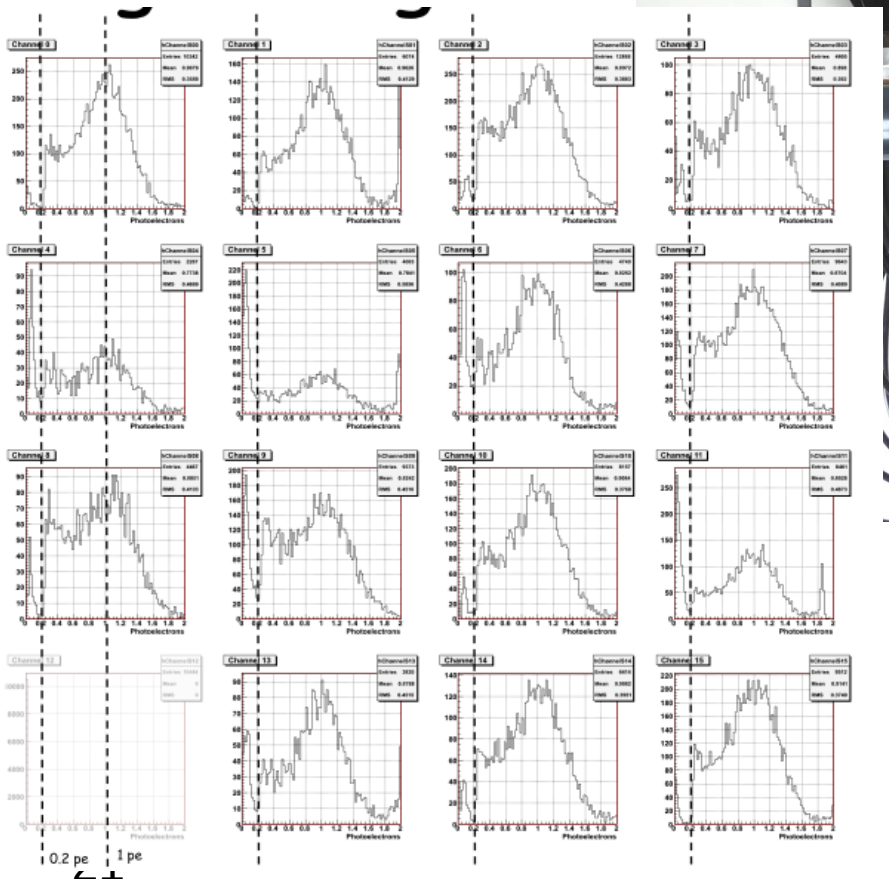
For every channel of Catiroc
Measurements with and without clocks for pedestal and injected charges up to 10 pe

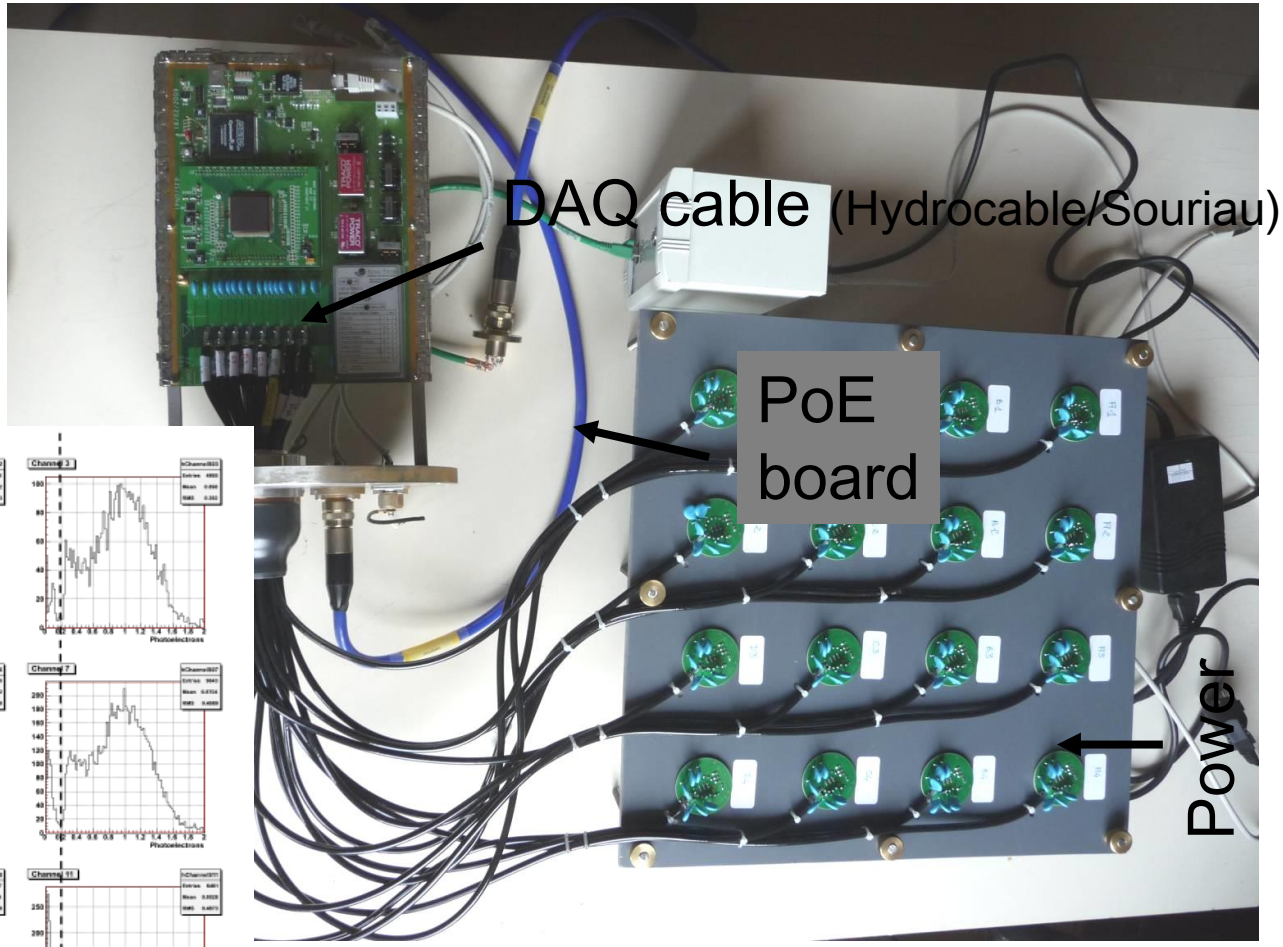
The pedestal mean value is around 940 UDAC without clocks and 950 UDAC with clocks with a shift of around 10 UDAC.





First full scale tests





IPNO+LAL+LAPP+ULB