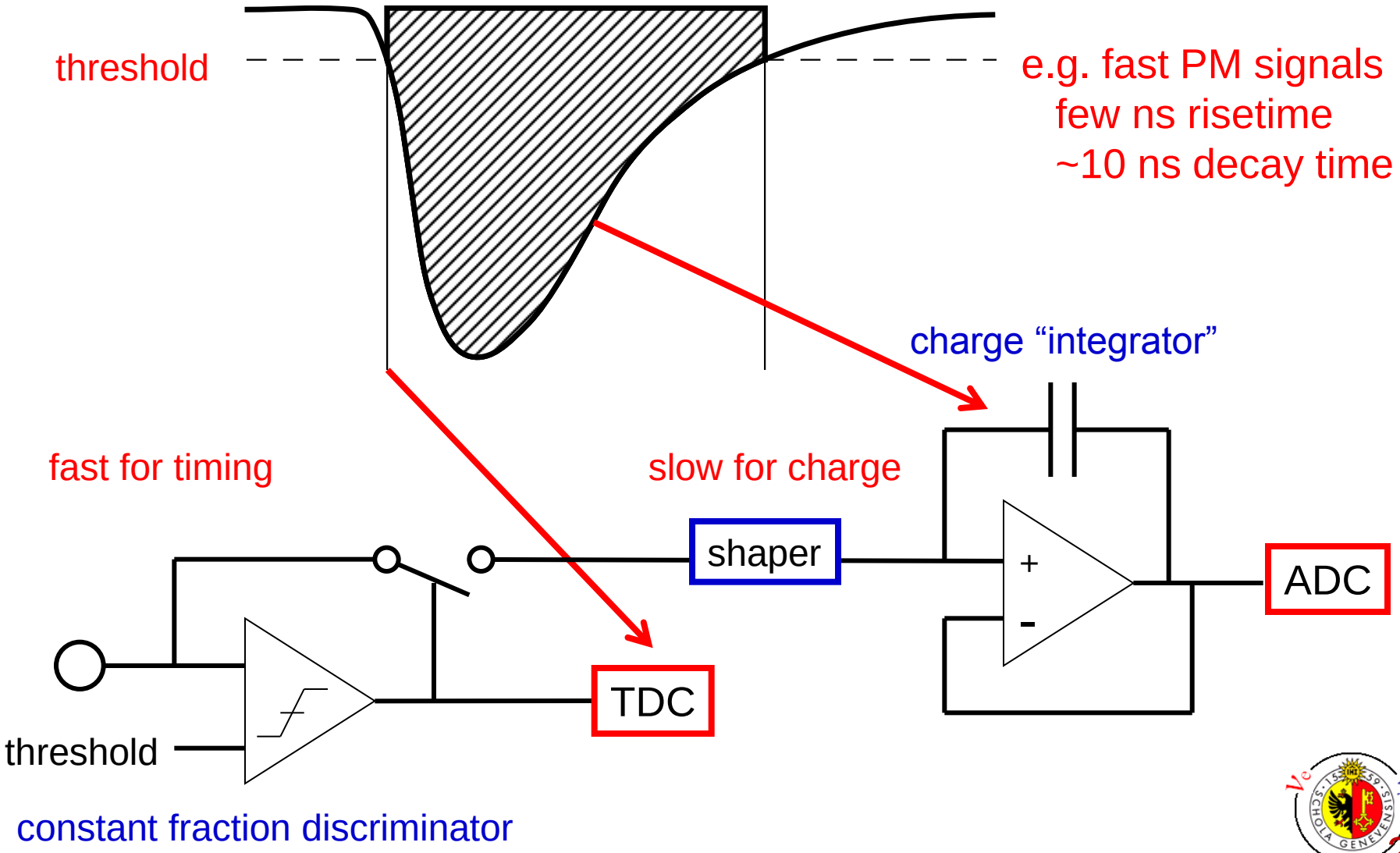
Digitizers Based on Capacitor Arrays

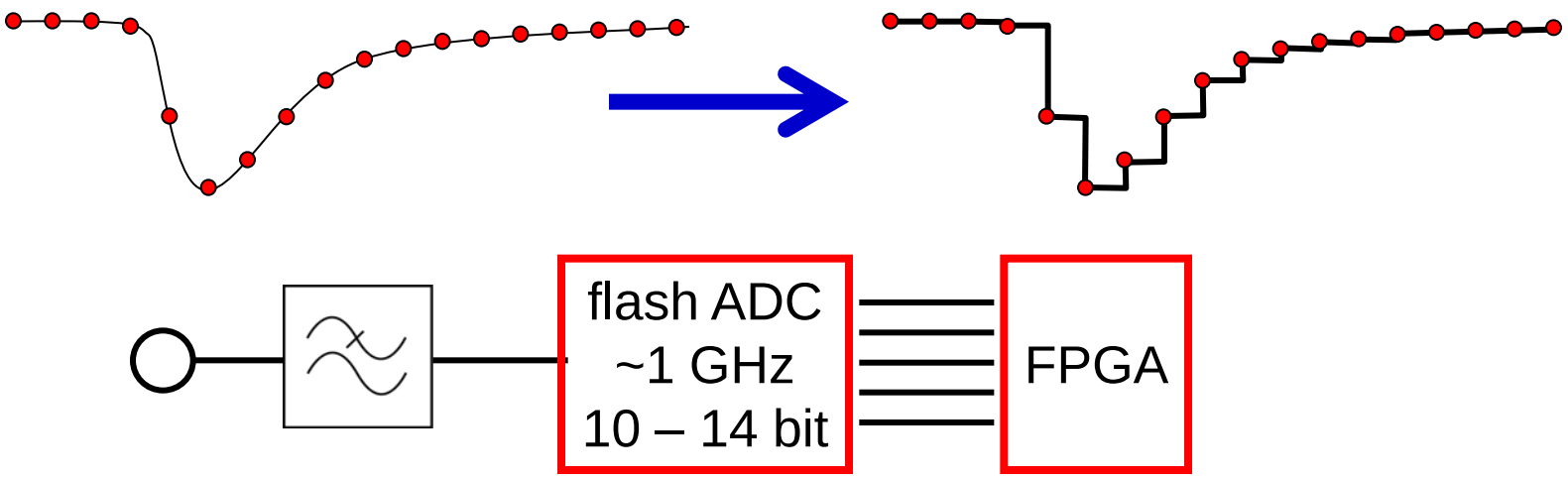
Hyper-K
11 July '16

Alessandro Bravar

How To Measure Best Timing / Energy "Traditional" Approach



How To Measure Best Timing / Energy Waveform Digitizer



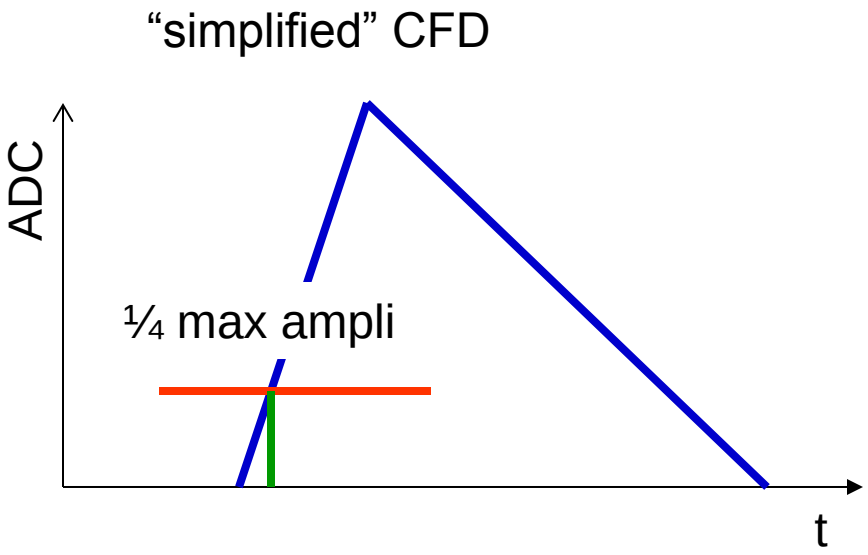
continuous waveform recording / processing

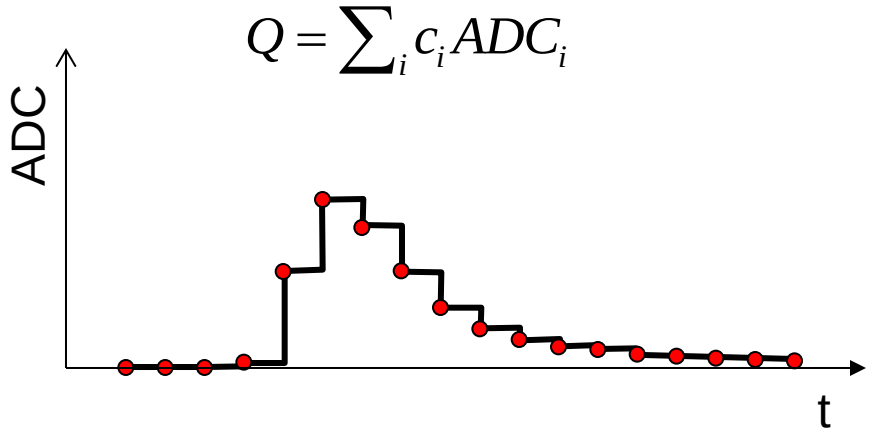
The waveform approach combines different functionalities with no dead time

general trend in signal processing

- less hardware, even “sloppy” amplifiers will work
- algorithms can be complex (and changed w/o changing hardware)
- triggerless, postpone decision
- storage of full waveforms allows for elaborate analysis (real time and offline)

Waveform Processing





Time resolution

1 GHz sampling

without doing anything
→ σ = 1000 ps / √12 ~ 300 ps

with "interpolation" can obtain
10 × better performance
→ σ < 50 ps

Charge resolution / dynamical range

12 bit over 1 V
→ σ = 0.25 mV

waveform sampled several times i.e. ~20 ×
"effective" # of bits: 12 bit + ½ $\log_2$ n → 14 bit
→ σ = 0.25 mV / √n < 0.1 mV
(10^4 dynamical range)

What Sampling Frequency?

My opinion: the electronics should be adapted to the detector characteristics (i.e. output) whenever possible and not the detector to the electronics

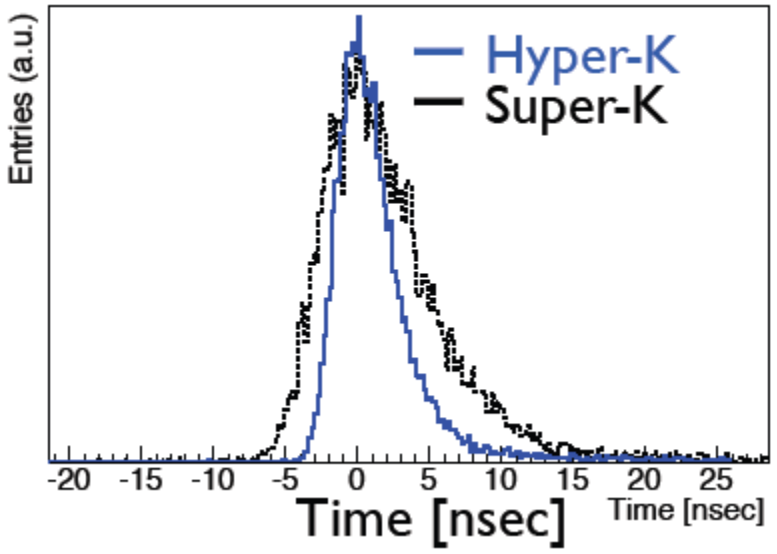
Good (optimal) performance requires ~5 samplings of the leading edge and ~10 of the trailing edge

(in total 15 to 20)

1 ns risetime $\rightarrow$ 5 GHz sampling

5 ns risetime $\rightarrow$ 1 GHz sampling

Typical HK 20" PMT signal
risetime < 5 ns



Waveform Processing

Undersampling:
acquisition of signals with sampling rates $\ll 2 \times$ highest frequency in signal

image processing

how many people do you see?

there is a limit to what one can do when starting with a poor resolution

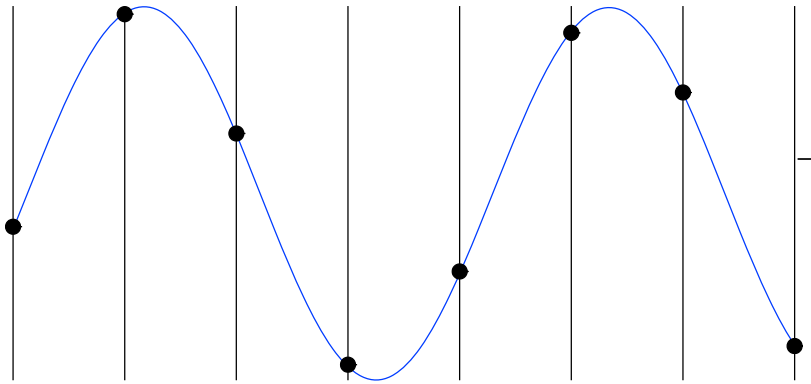
Nyquist-Shannon Sampling Theorem

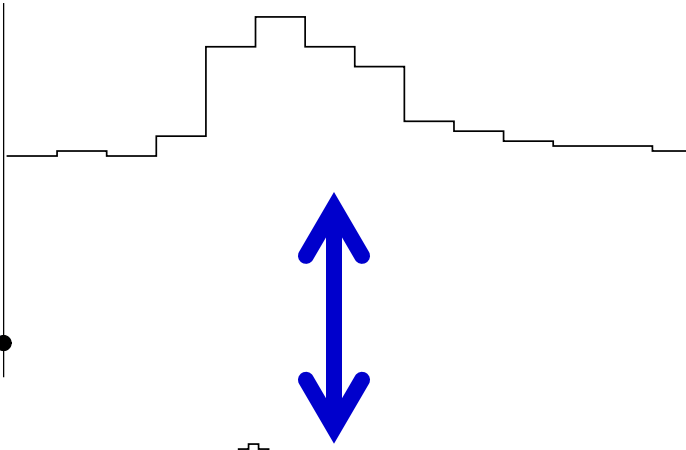
Q: How many pulses can be transmitted per second
and recovered through a channel of limited bandwidth?

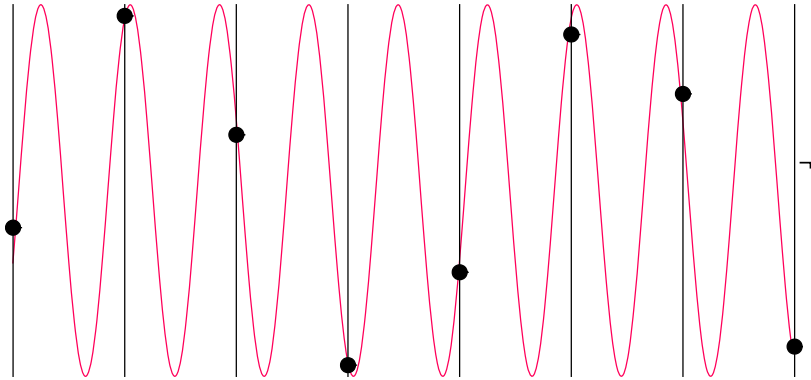
A: $f_{signal} < BW / 2$ $\quad BW \sim \pi / \tau_R$, $\quad \tau_R = 1$ ns $\rightarrow$ BW ~ 300 MHz

double pulse resolution possible, if pulses separated more than $2\tau_R \rightarrow f_{sampling} > 2 / \tau_R$

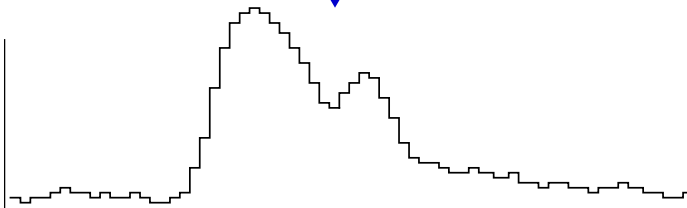
$f_{signal} < f_{sampling}/2$







$f_{signal} > f_{sampling}/2$



$f_{sampling} > 1 / \tau_R$

Waveform Processing

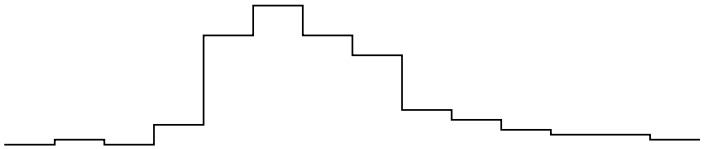
Optimal sampling:
(don't gain much with oversampling)

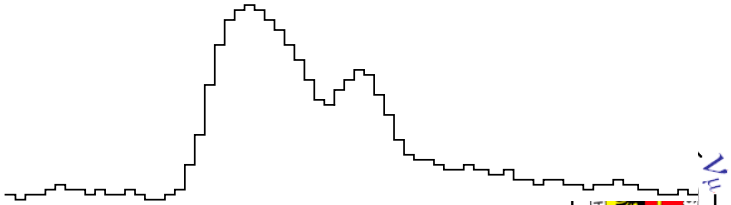
how many people do you see?

higher resolution

three

fast sampling





FlashADC + FPGA Design: Pros & Contras

Continuous waveform recording / processing
→ many advantages over “traditional approaches”
“self-triggering” i.e. decide after looking at the waveform

Based on commercially available components (telecommunication technology)
Different fADCs in GHz range commercially available from different vendors (not cheap !)

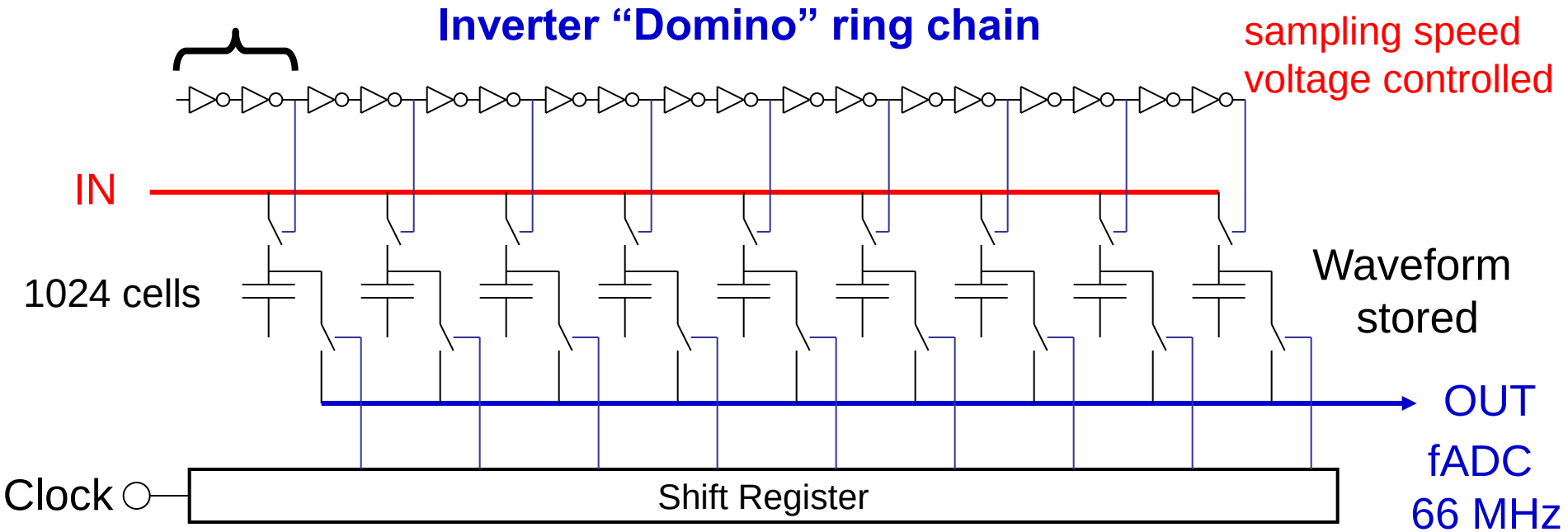
At high sampling rates (~GHz)
very expensive design (1000 CHF / ch.)
high-end FPGA
non trivial board design (GHz !)
high power consumption ~ 5 W / ch.

Solutions (many options)
waveform stretching: stretch the waveform and sample the signals at ~10 × lower rates
loose the advantages of high frequency sampling

use switched capacitor arrays: sample the signal at high rates, digitize at lower rates
no loss in performance
requires a lot of calibrations
dead time (there are various solution to circumvent this problem)
requires some kind of decision making (trigger)

Switched Capacitor Array (the DRS solution)

5 GHz – 0.8 GHz: 0.2 – 1.25 ns sampling → 200 to 1250 ns deep buffer



it works like a time stretcher, but with no deterioration of signal / loss of information:

sampling ~ 5 GHz range

digitization ~ 50 MHz range

☺ cheap design !

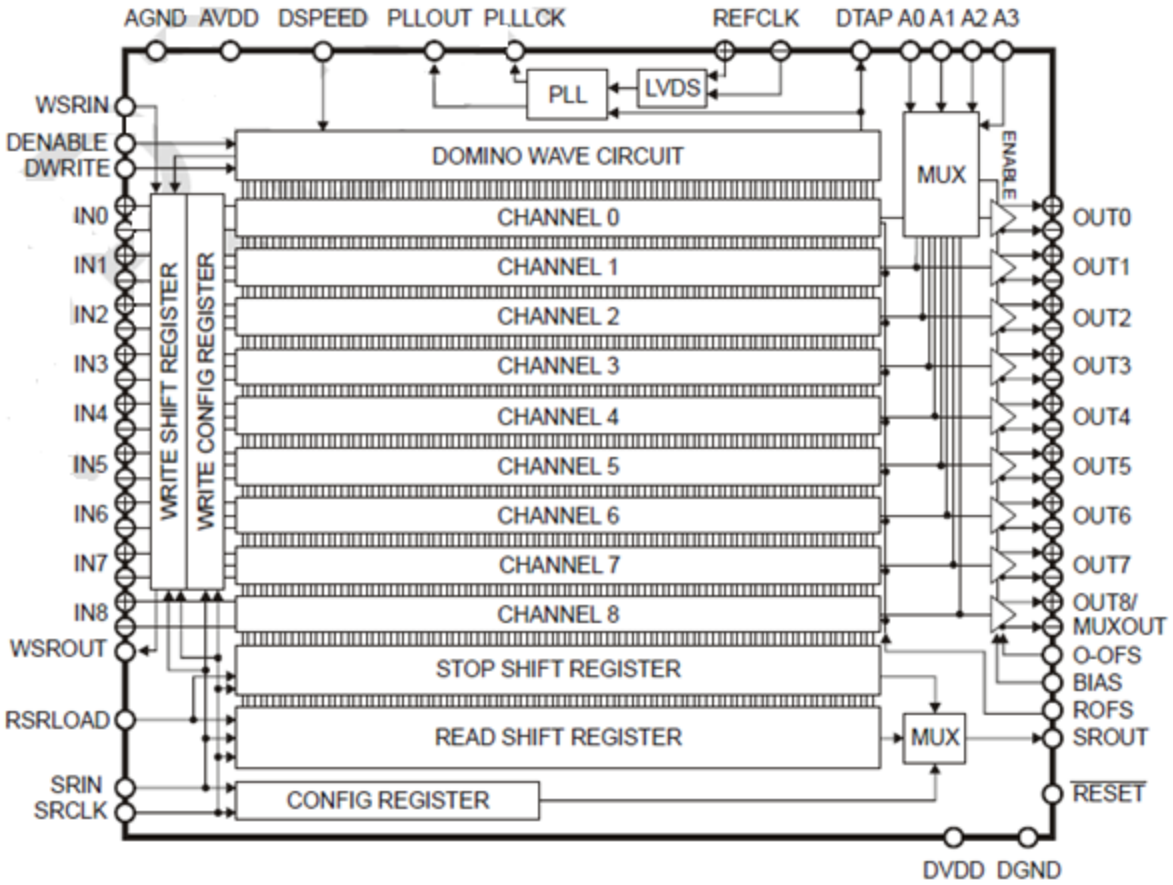
☺ low power !

☹ one single array cannot sample during readout

→ deadtime (can be made as short as 15 μs)!

The DRS Digitizer

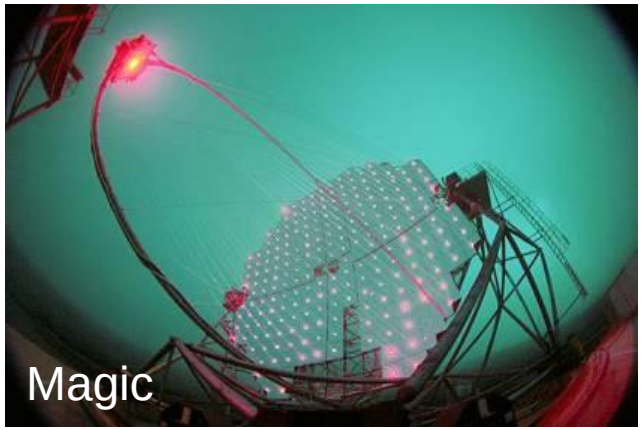
developed at PSI S. Ritt et al.
www.psi.ch/drs

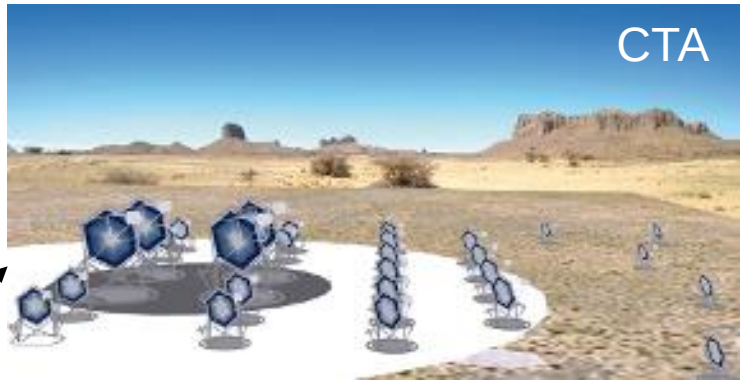


ASIC with 8 switched capacitor arrays (1024 caps / ch.)
- up to 5 GHz sampling speed (controlled by an internal digital delay line)
- 11.5 bit resolution
- various operation modes

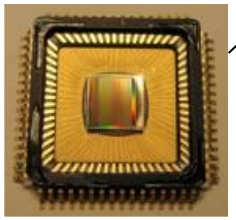
note: not the only capacitor array on the market, but I'm in Switzerland …
different arrays have different merits …

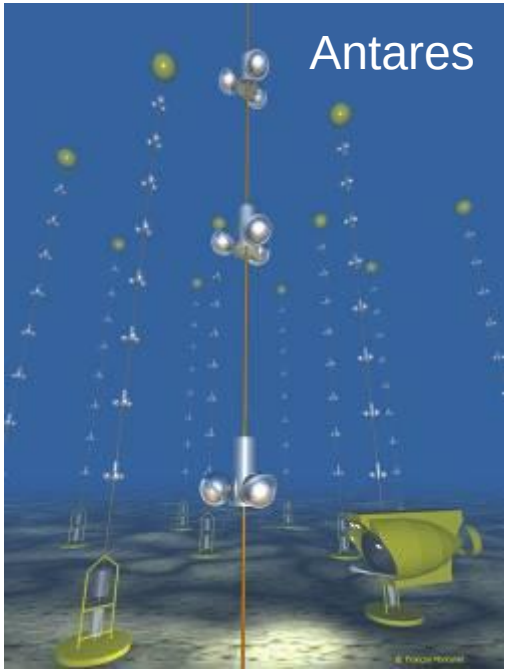
DRS4 "Users"

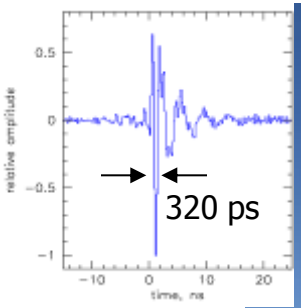


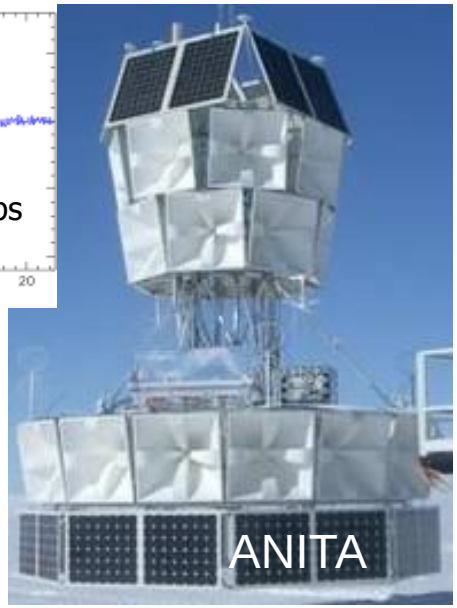


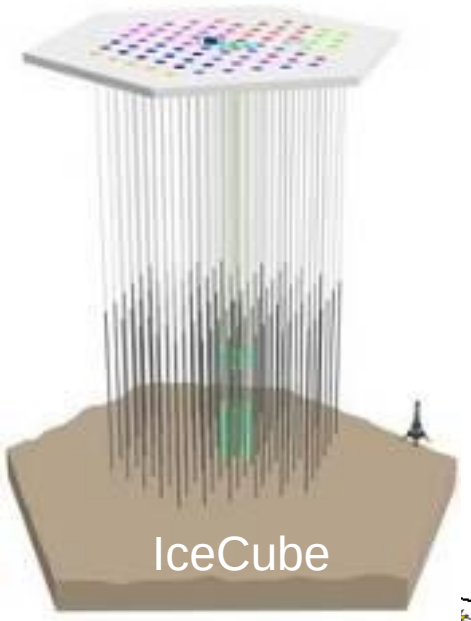
DRS4











and growing !

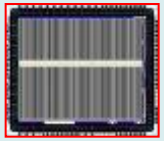
DRS Not the Only One

G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

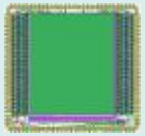
STRAW3 LABRADOR3 TARGET


- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

www.phys.hawaii.edu/~idlab/

AFTER SAM NECTAR0



- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

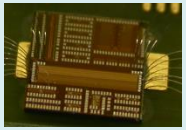
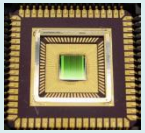
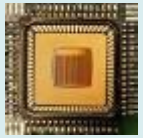
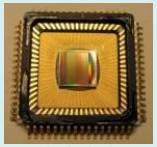
matacq.free.fr

PSEC1 - PSEC4

- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

psec.uchicago.edu

DRS1 DRS2 DRS3 DRS4

2002 2004 2007 2008

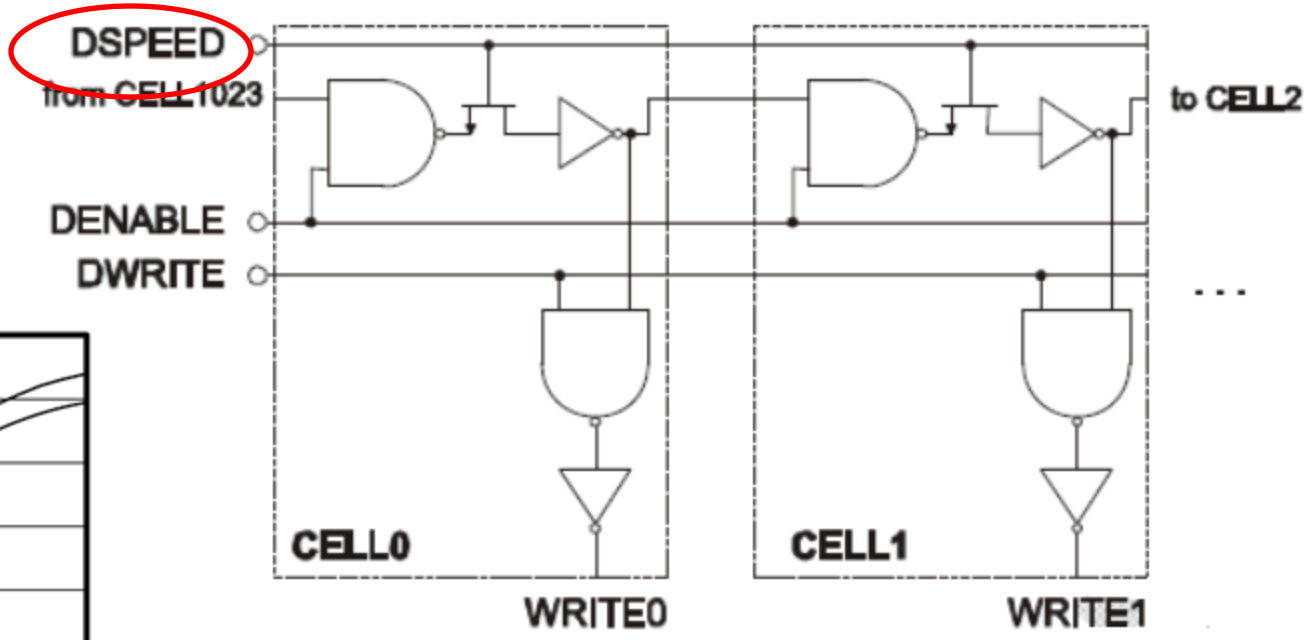
- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

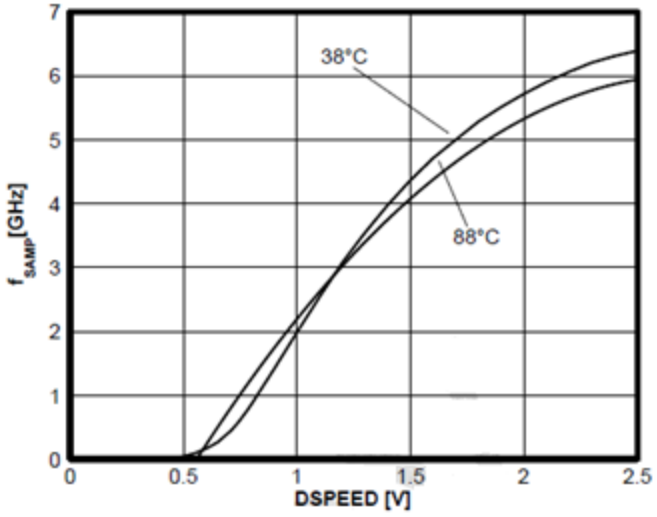
S. Ritt
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

Domino Wave Circuit (Digital Delay Line)

voltage regulated
via PLL locked to
internal or external
reference clock





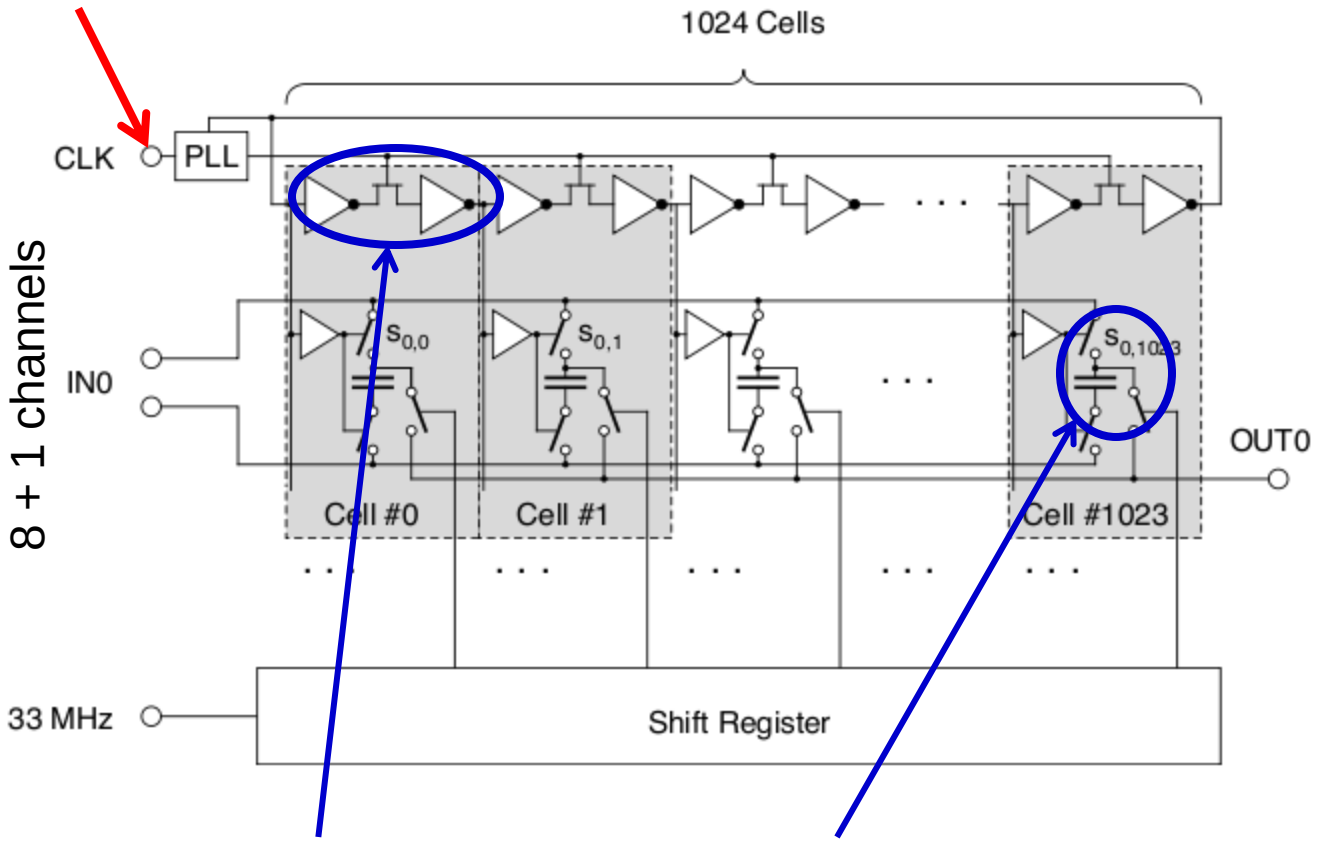
Once the domino wave starts,
It continues indefinitely

The speed of the DDL can be
varied with an external control
voltage (bias).

Domino Ring Sampler (DRS)

reference clock

sampling f / 2048 (@5GHz → 2.5 MHz)



5 GHz digitizer

11.5 bits

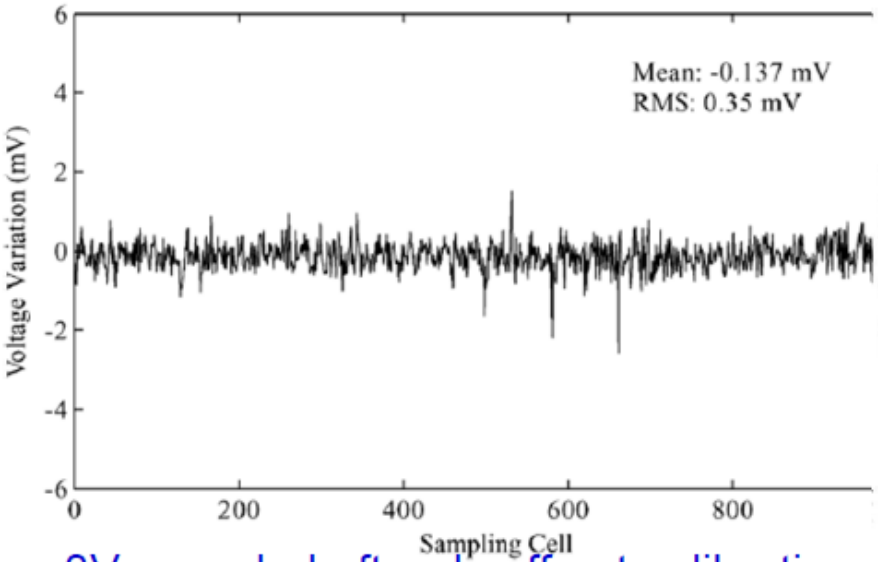
33 (66) MHz readout

30 (15) μs deadtime

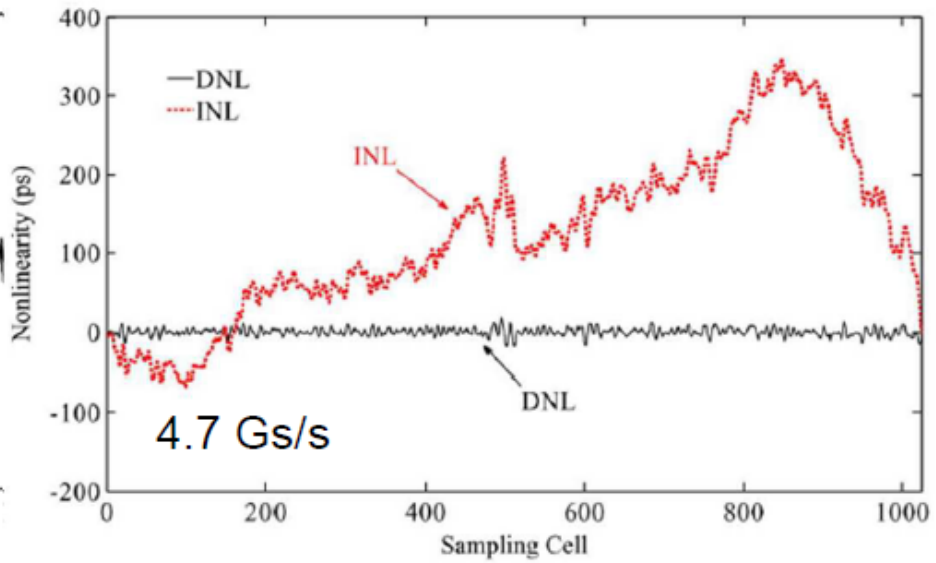
Requires time calibration, i.e. each cell has a different "time" width ΔT,
and "energy" calibration, i.e. each cell has a different capacitance → gain,
for each capacitor cell

→ large set of calibration data (4 k calibration constants / channel, feasible)

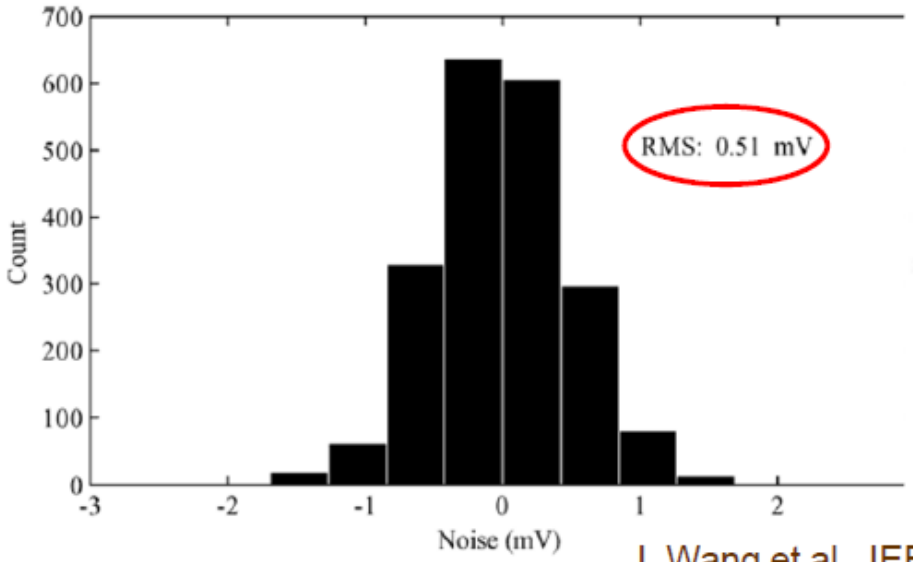
DRS NON-Linearity

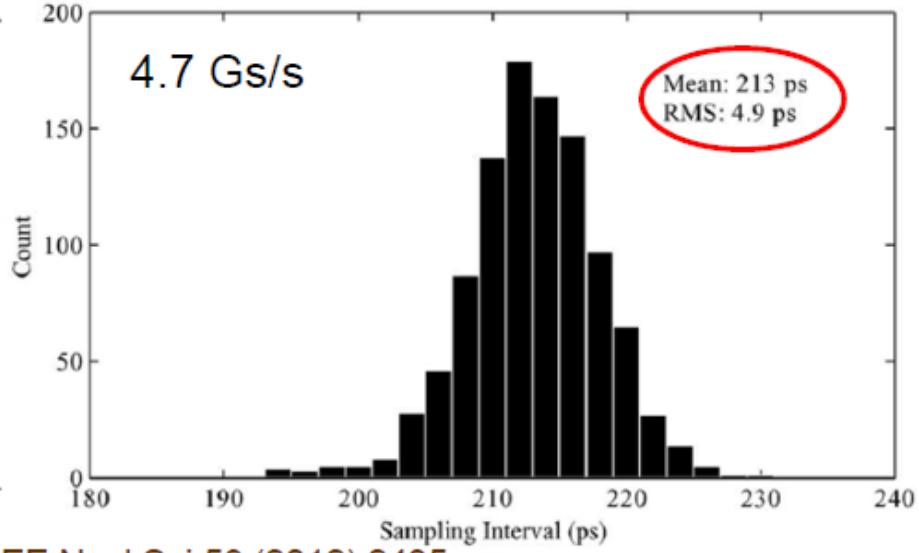


0V recorded after dc off-set calibration



timing nonlinearities





J. Wang et al., IEEE Nucl.Sci.59 (2012) 2435

UniGE DRS Prototype Board

development board for NA61 readout (overkill !) and future projects
test different operation modes of the DRS ASIC
calibration procedures
firmware development

features of the board:

4 + 1 input channels

analog Front-End stage
> 500 MHz BW

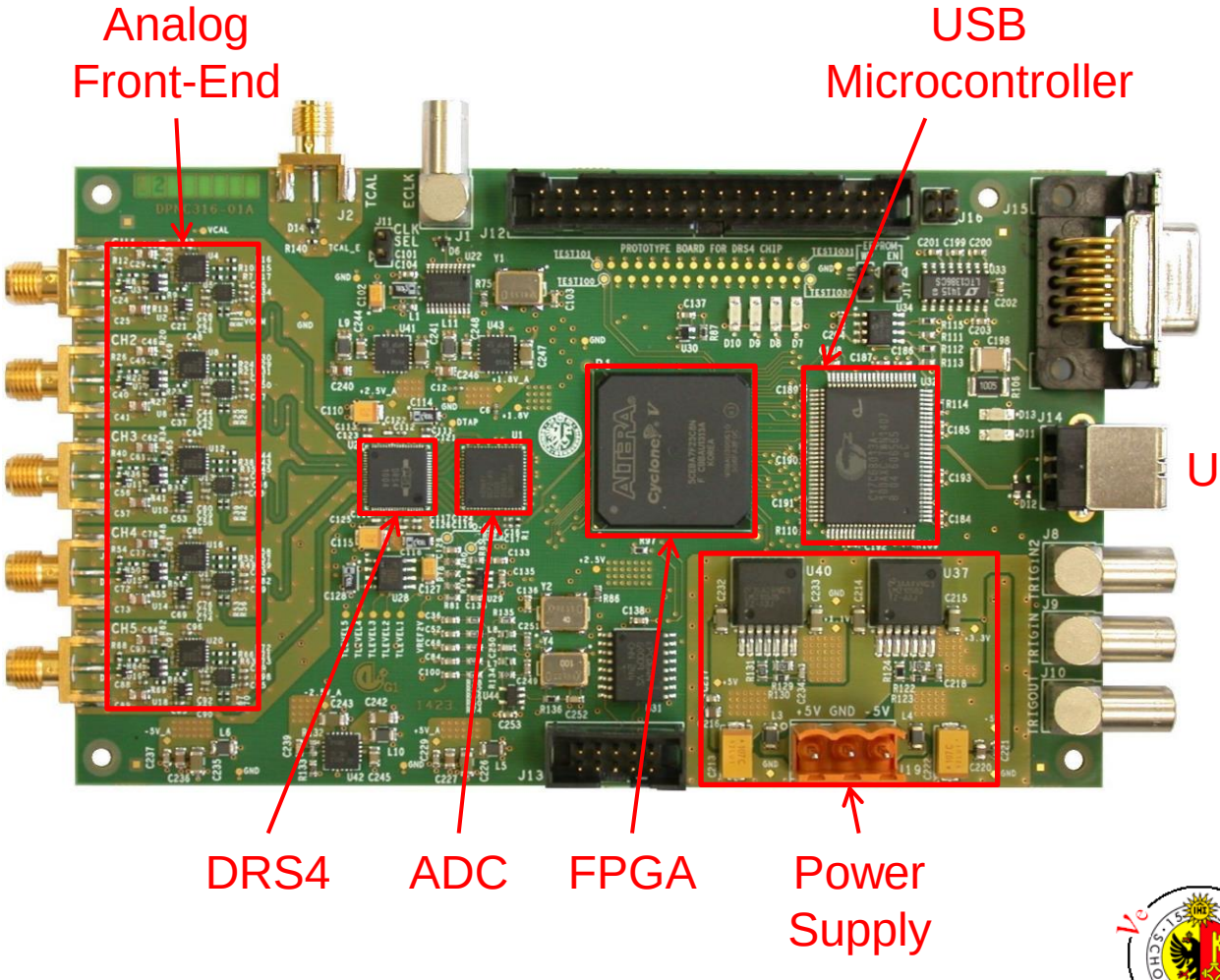
DRS4 ASIC

12-bit 8-channel ADC

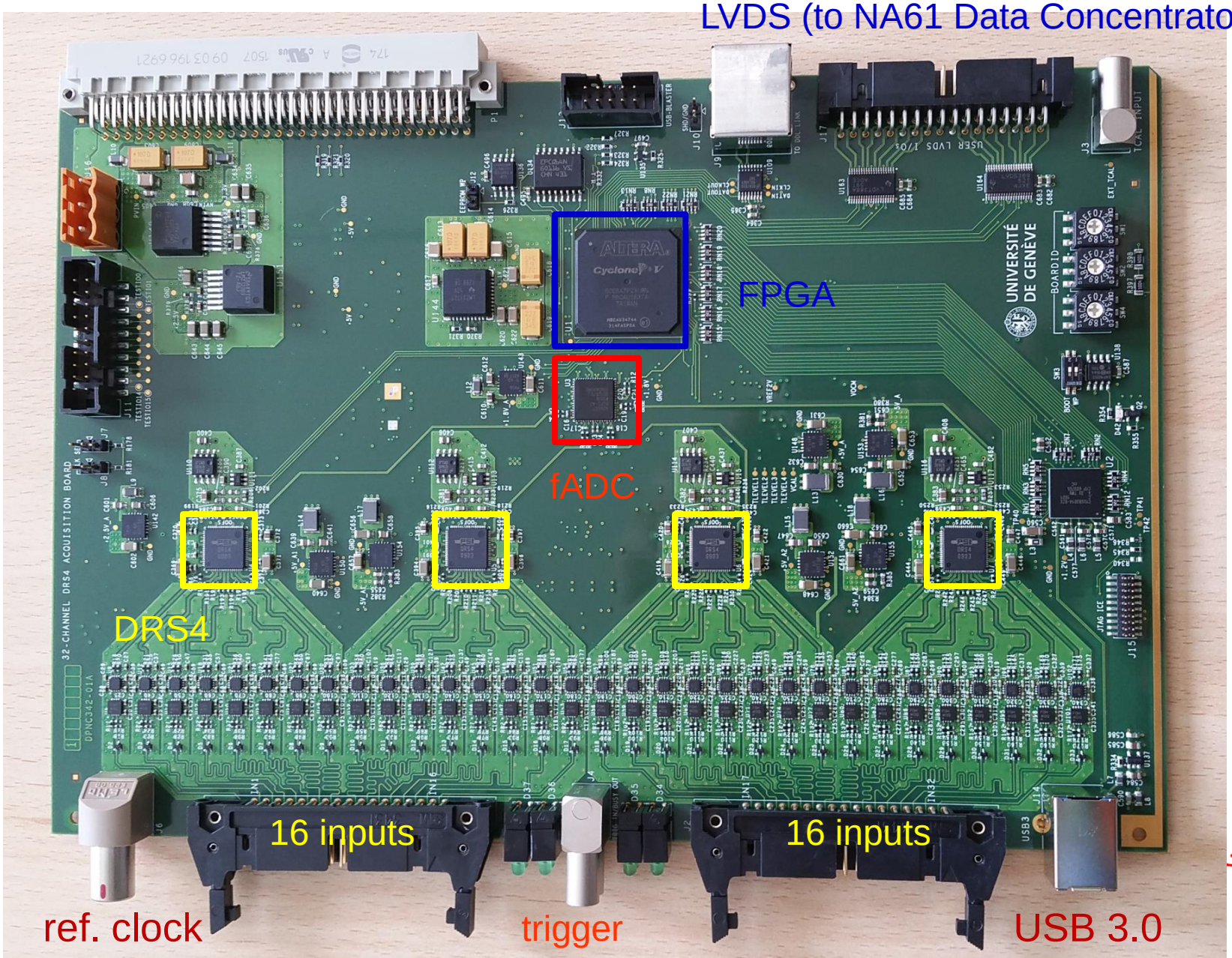
Altera Cyclone V FPGA

USB Microcontroller

on-Board timing and
voltage calibration



NA61 32 ch. DRS Board



NA61 Design

~4'000 channels

timing: few 10 ps resolution
calorimetry: 10^4 dynamical range from mip (1.5 GeV eq.) to 30 TeV (Pb)

DRS "operation" mode tailored to NA61 environment (also to minimize cost)
low rate: ~100 Hz today, ~1kHz after 2020

serial readout: 1 ADC channel per DRS chip (8 input channels)
important deadtime $\rightarrow$ 250 μs (4 kHz max rate)

64 kbyte / event (needs on board data reduction)

external trigger

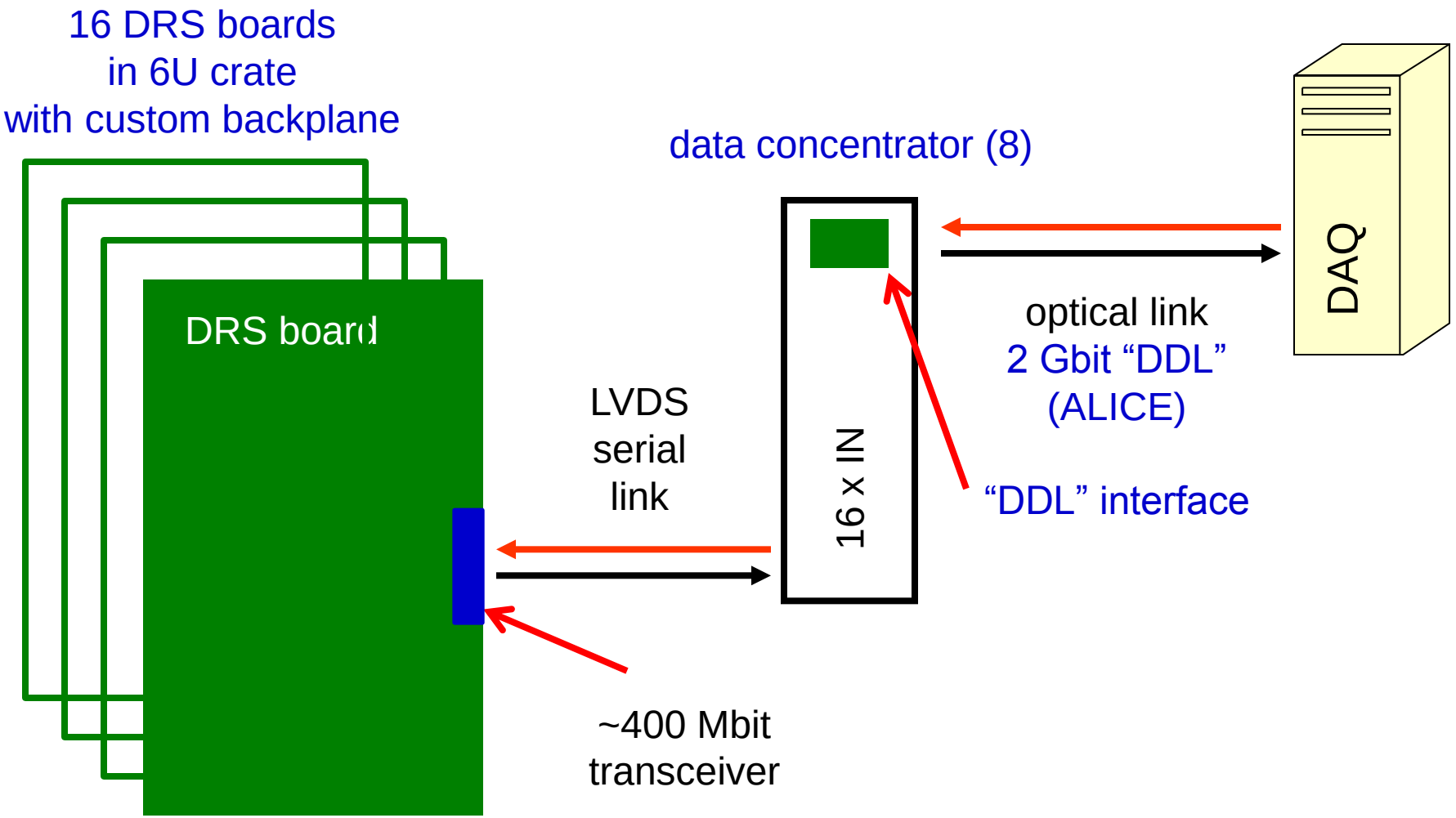
1 clock master to synchronize all DRS boards

low power ~0.5 W / ch. @ 5 GHz
(most in the analogue part)

under consideration a "deep buffer" version to record waveform segments
for ~10 μsec (i.e. ± 5 μsec around trigger time)

costing
(excluding development and prototyping)
~60 CHF / ch. all inclusive (DRS baords + PS + clock + …)
~35 CHF / ch. DRS boards only (5 GHz sampling !)

NA61 DAQ


16 DRS boards
in 6U crate
with custom backplane
DRS board
data concentrator (8)
16 x IN
DAQ
optical link
2 Gbit “DDL”
(ALICE)
“DDL” interface
LVDS
serial
link
~400 Mbit
transceiver

Performance

To achieve desired performance (time and energy resolution) need to calibrate often the DRS capacitor arrays:

Energy (voltage) calibration:

voltage sweep through the chip

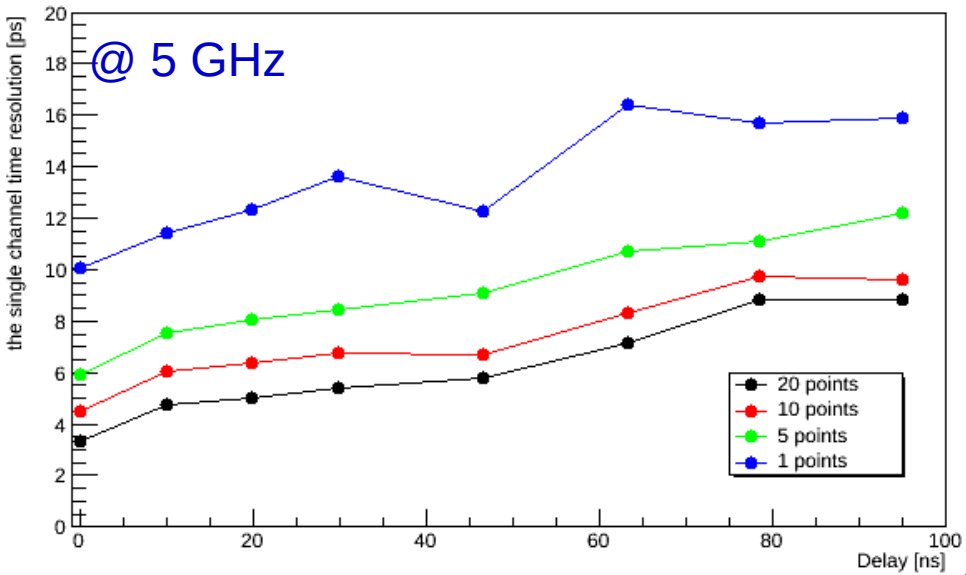
→ determine gain and offset for each capacitor in the array

Time calibration:

record ~100 sinus like waveforms (10–100 MHz) with random phases w.r.t. DRS PLL

→ determine the time “width” of each capacitor in the array

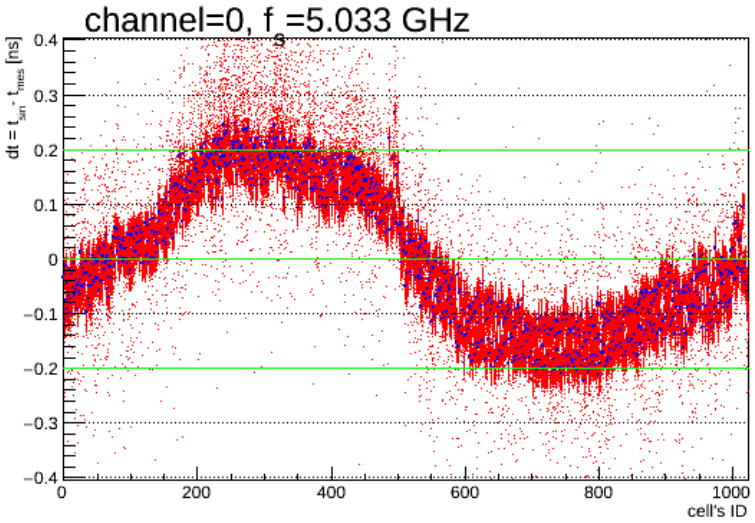
time resolution
using the split signal technique
and CFD algorithms



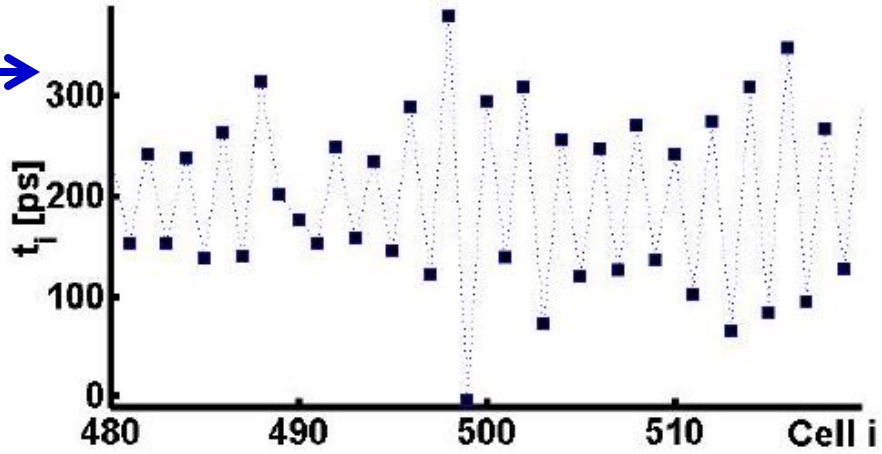
Repeat calibrations when environmental conditions change (temperature!)

Timing Performance @ 5 GHz

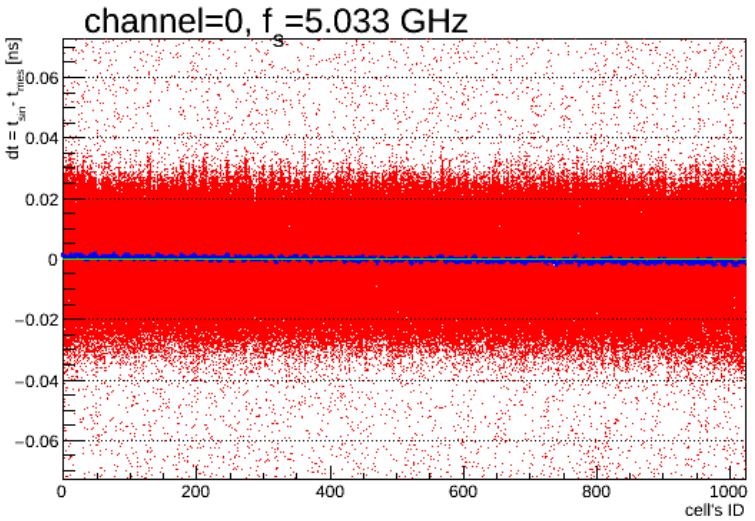
uncalibrated



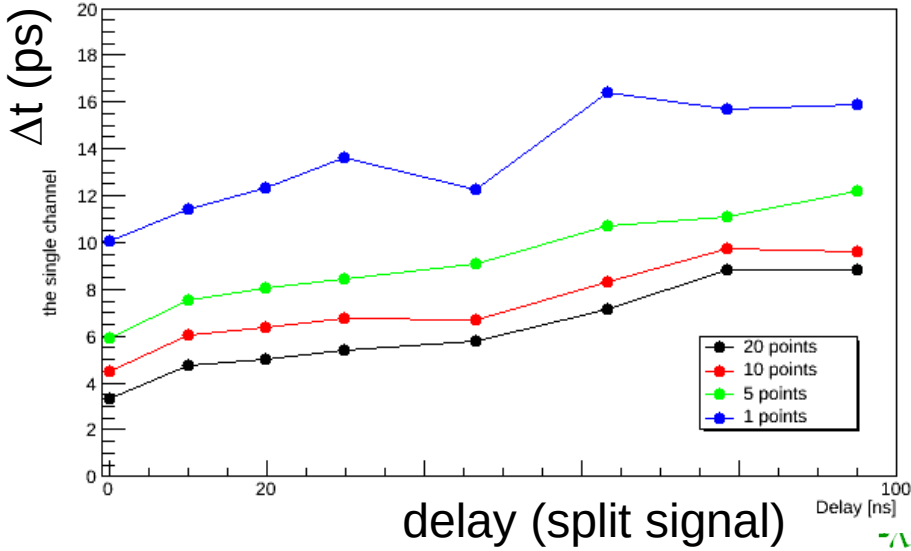
time “width”



calibrated (last iteration)



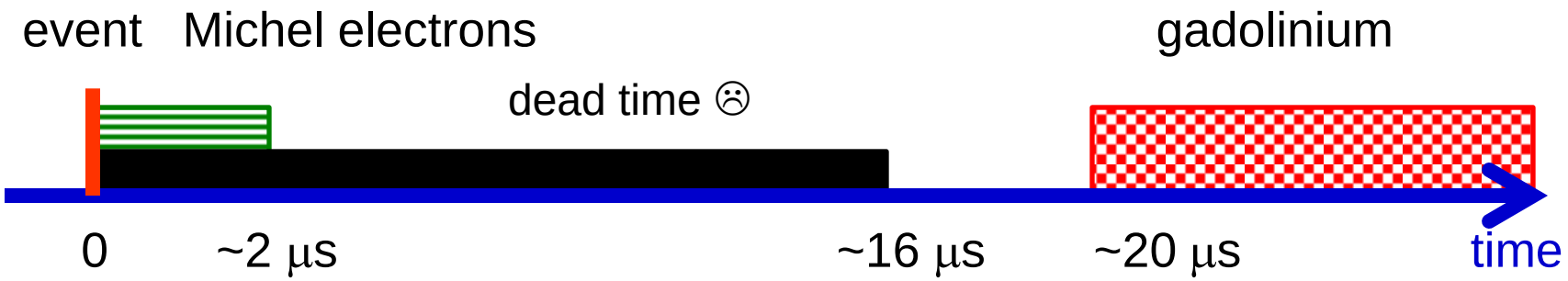
intrinsic time resolution



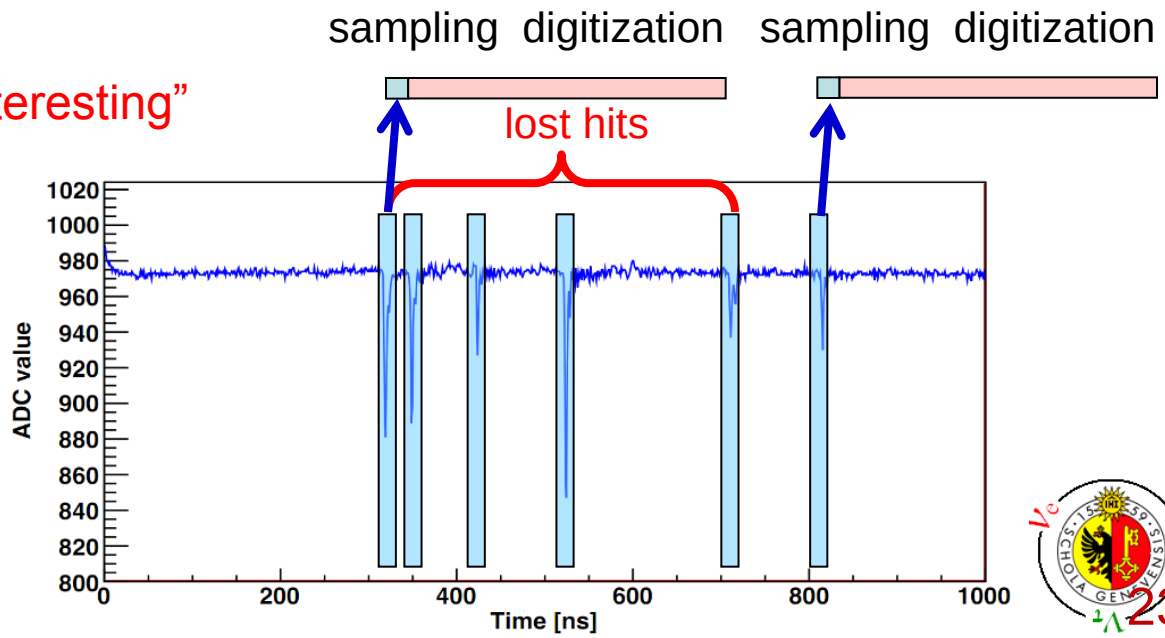
delay (split signal)

The Deadtime Issue

With capacitor arrays cannot sample and digitize simultaneously → deadtime
For a low rate experiment the deadtime should not be an issue,
however for correlated events it can become a problem
for example:



however
only part of the waveform is “interesting”



Around the Deadtime

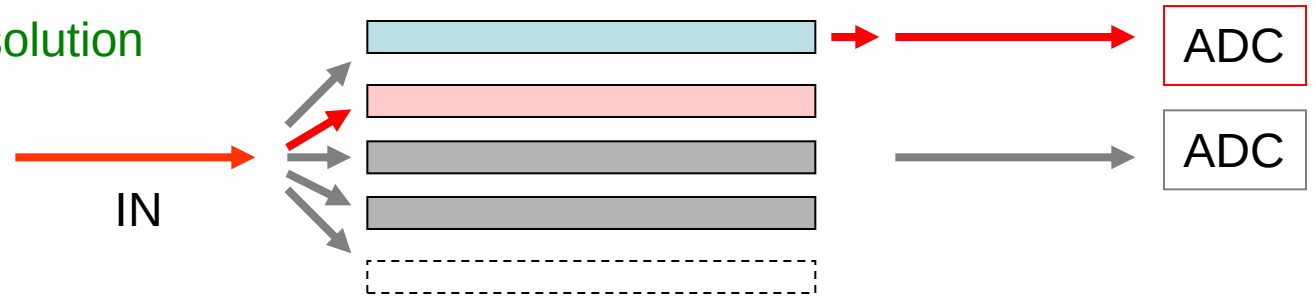
however only part of the waveform is “interesting”

Use several capacitor arrays looking at the same input:

- while digitizing the signal recorded in one array
  continue sampling the signal on the following array

- add as many SCA as necessary to guarantee a deadtimeless sampling
  (rate dependent)

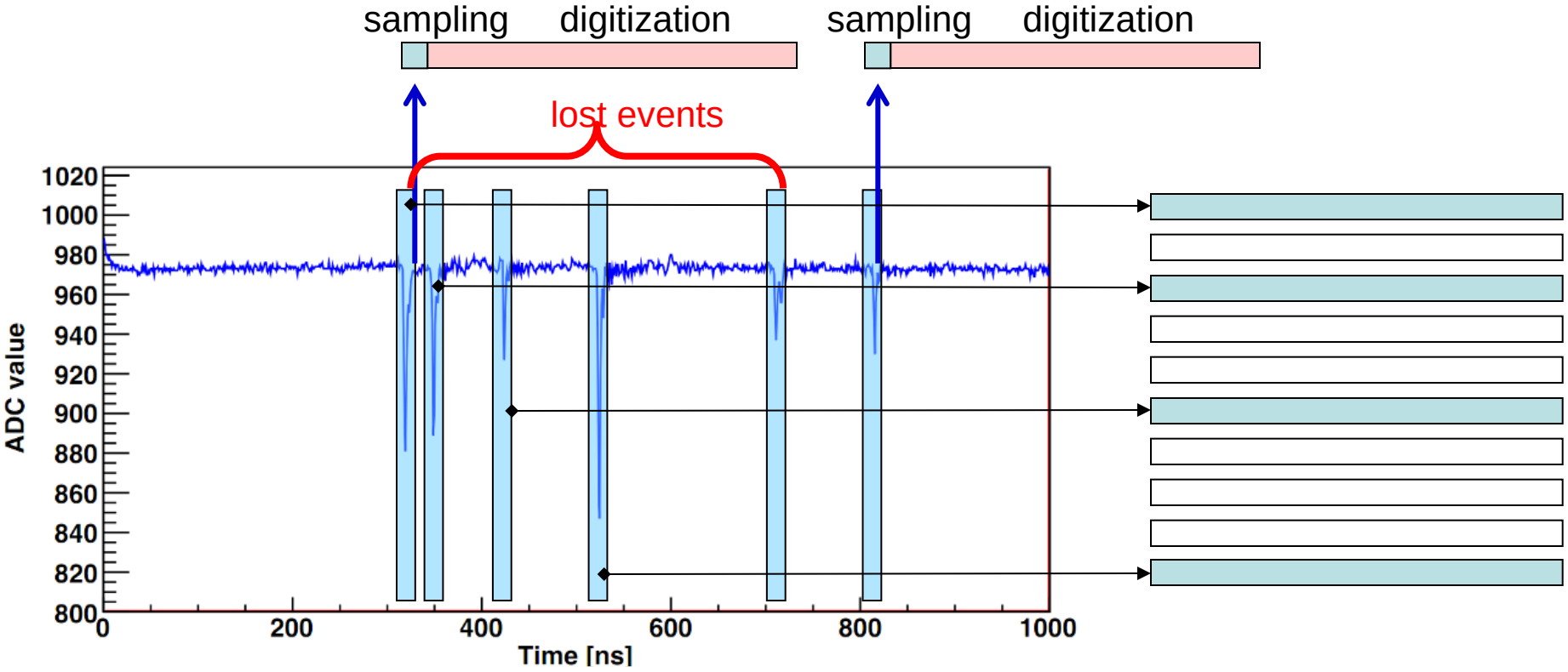
☺ virtually deadtimeless solution



one of the features of the (8 ch.) DRS4 ASIC is the
possibility to sample the input of one capacitor array
and to digitize the content of another channel at the same time
(not optimal, since the segments are very long)

using all 8 channels on the chip can sustain rates of up to 500 kHz with virtually no DT
ex.: at 2 GHz sampling can digitize up to 500 k, 500 ns long waveform segments / sec

The Dead Time Issue – DRS5 Solution



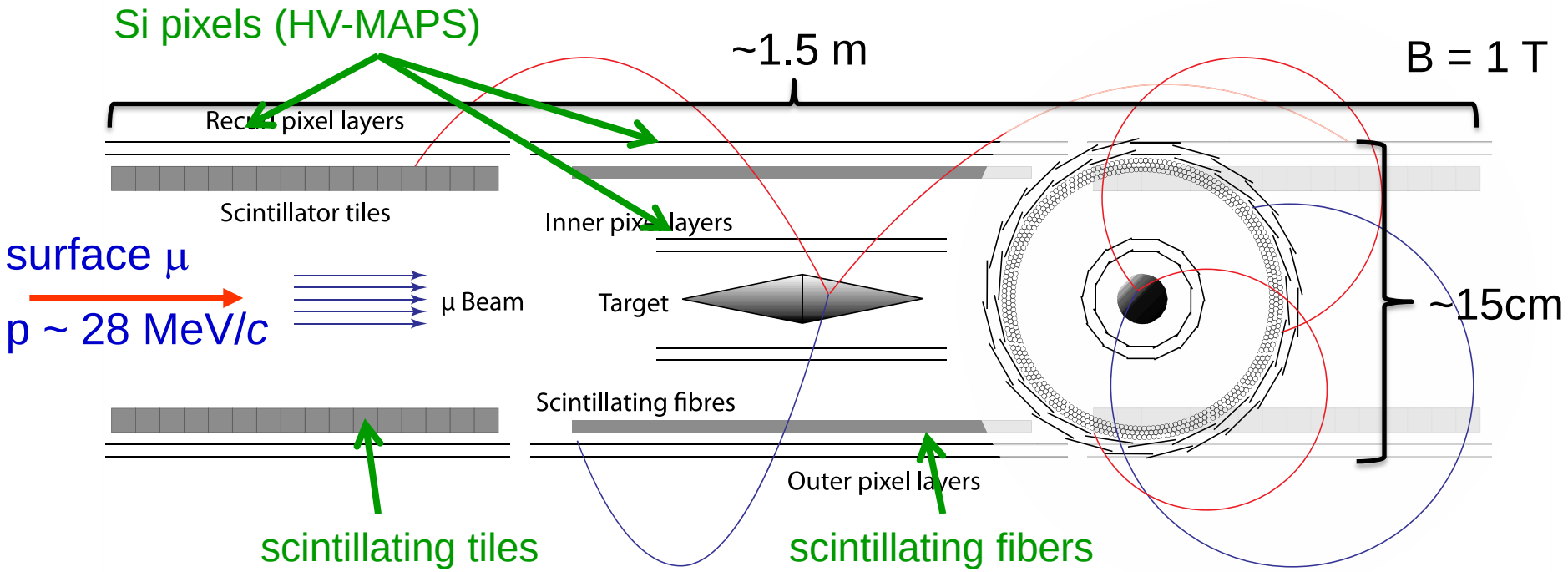
Only short segments of waveform are of interest

developed at PSI S. Ritt et al.
www.psi.ch/drs
expected in 2017
first user Mu3e

DRS5 solution:
store sampled waveform in a 2D array
digitize only interesting segments
sampling and digitization asynchronous
virtually deadtime less up to
average rate = f_{ADC} / window size

The Mu3e Experiment at PSI

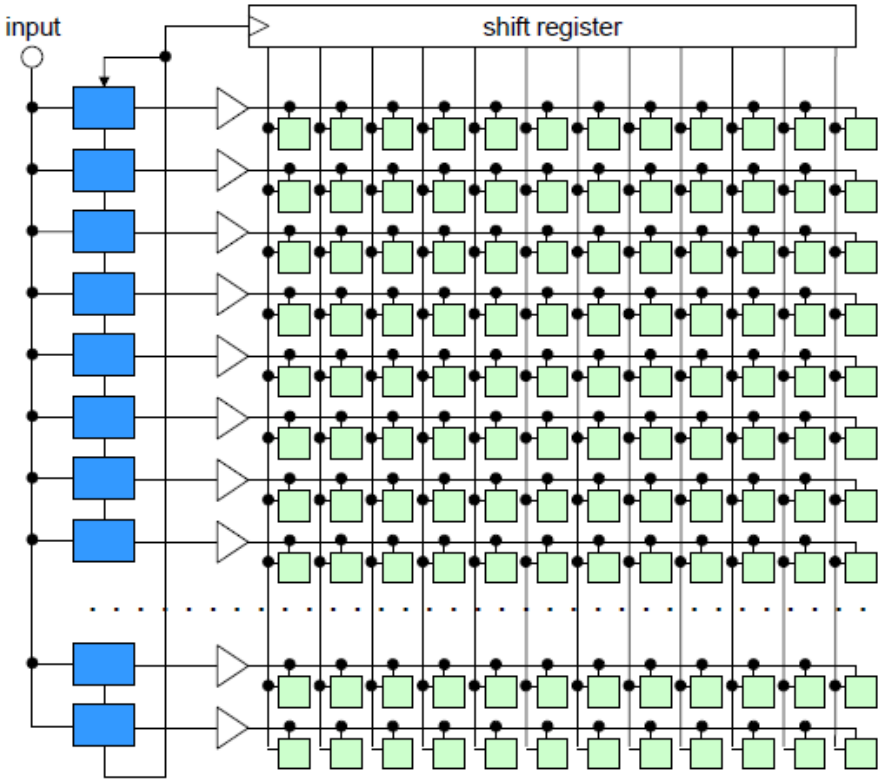
neutrinoless $\mu^+ \rightarrow e^+ e^- e^+$ decay



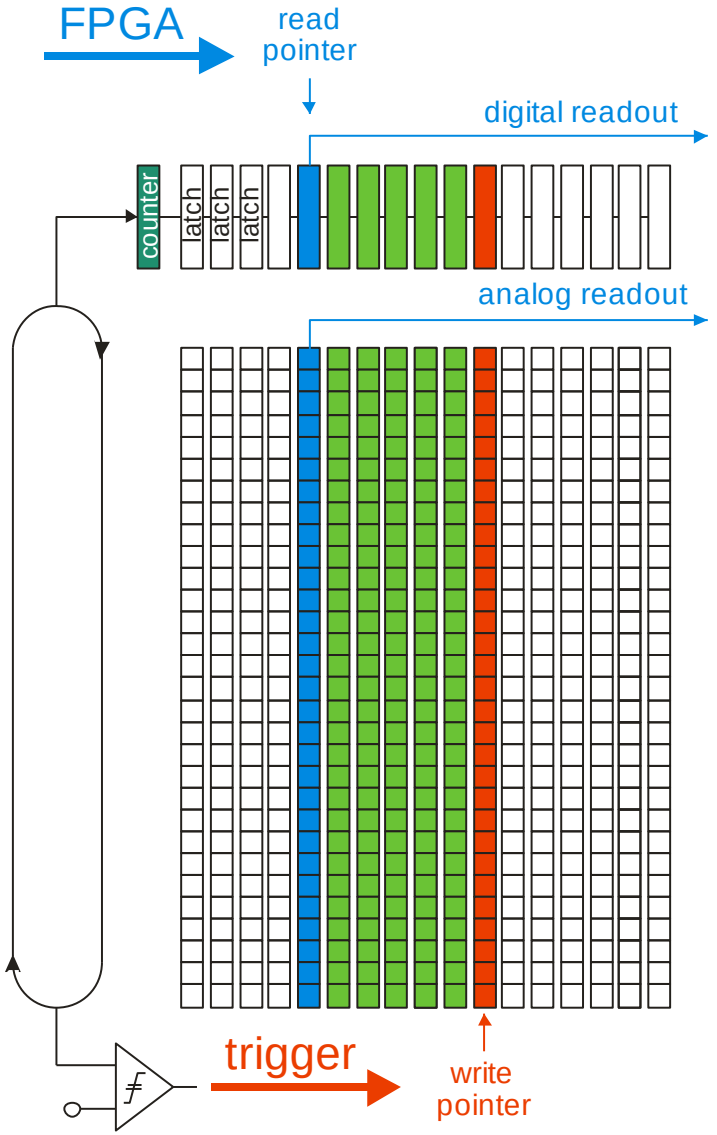
rate: 2×10^9 μ decays / s

timing detectors read out with DRS5
rate > 1 MHz / Si-PM ch.

The DRS5 Digitizer



fast sampling storage of segments



10 GHz sampling, 3.1 ns hold time
2-5 times better timing resolution

data driven readout

(almost) dead-time-less waveform digitizing
can sustain continuous rates up to few MHz

Outlook

Can be used to start testing various ideas / solutions
i.e. what additional information → performance can be gained?

We could develop a digitizer board closer to HK than the NA61 design over a short time (parallel readout, faster fADC, …)

Cheap design for a GHz digitizer

DRS4 digitizing electronics being developed for NA61
First deployment in NA61 in Fall 2016
(have not discussed the synchronization of DRS chips and boards)

The DRS4 can be run in a virtually deadtime free mode
(one of operation modes)

Improved version, DRS4.1 under consideration → before end of 2016
(new DRS5 developed for Mu3e at PSI in 2017)

Should consider the possibility of developing a chip tailored for Hyper-K