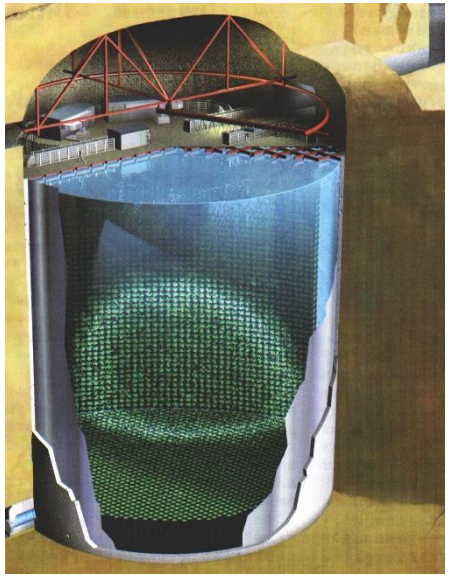
Electronics and DAQ system for Hyper-Kamiokande

Yoshinari Hayato
(Kamioka obs., ICRR, Univ. of Tokyo)
for the Hyper-K electronics & DAQ working group

Introduction

Hyper-Kamiokande

~ Gigantic underground water Cherenkov detector



What we want to do? (necessary functionalities)

Measure charge from photo sensors

Measure arrival timing of photons

What we need?

Self gating signal digitizer (ADC + TDC)

Accurate clock synchronization system

(Sync. Clock + Counter)

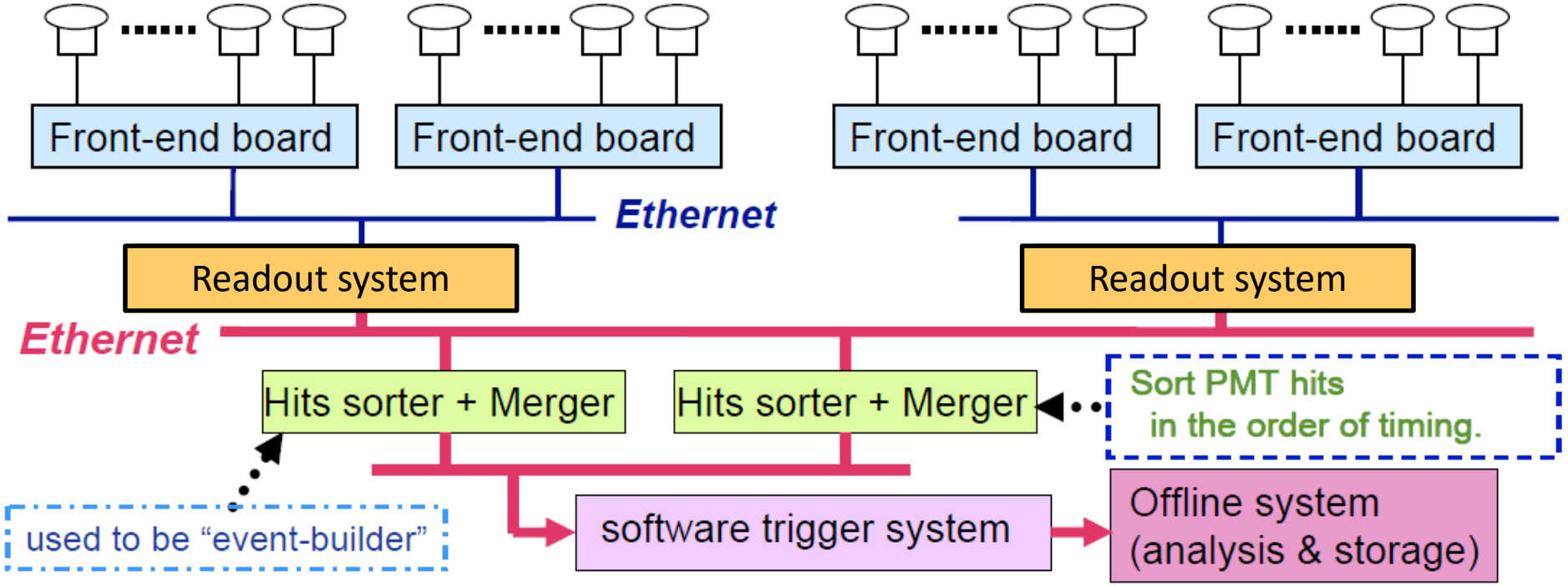
and GPS

We also need

Stable power supplies for photo sensors

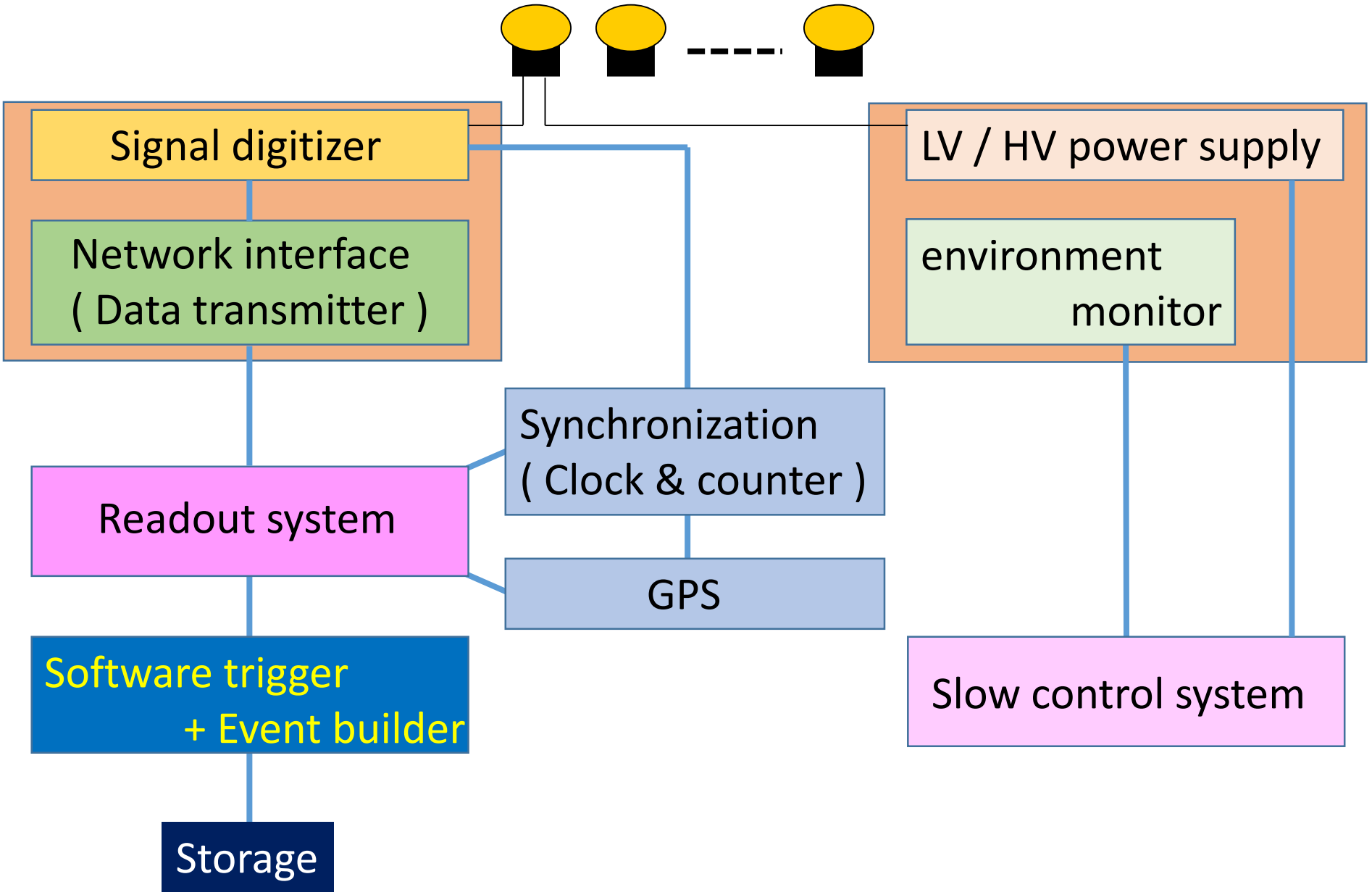
and various system / environment monitors

Schematic diagram of the HK electronics / DAQ system



1) Signals from the photo sensor above discriminator threshold are continuously digitized.
2) All the "digitized" hit information including dark noise are sent to the readout computers.
3) Define events using the software trigger and send them to the offline system and also store the events in the disk.

Major components of the HK electronics / DAQ system



Location of the front-end electronics

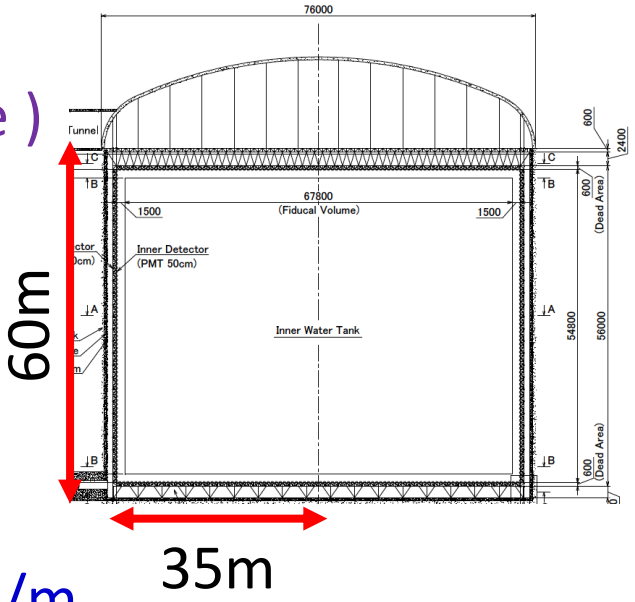
It is better to have front-end electronics on the roof of the detector.

However, there are several problems in running the cables from each photo sensor

a) Length of the cable

Necessary length of the signal cable > 150 m

40 m (bottom) + 65 m (wall)
+ 40 m (surface)



- Degradation of the signal is expected.
- Different lengths of the cables may make calibrations difficult.

b) weight of the cable is 100 ~ 200 g /m

-> 15 kg ~ 30 kg / 150m –> **675 ~ 1350 tons!**

-> non negligible weight

-> affect the design & cost of the structure

Location of the front-end electronics

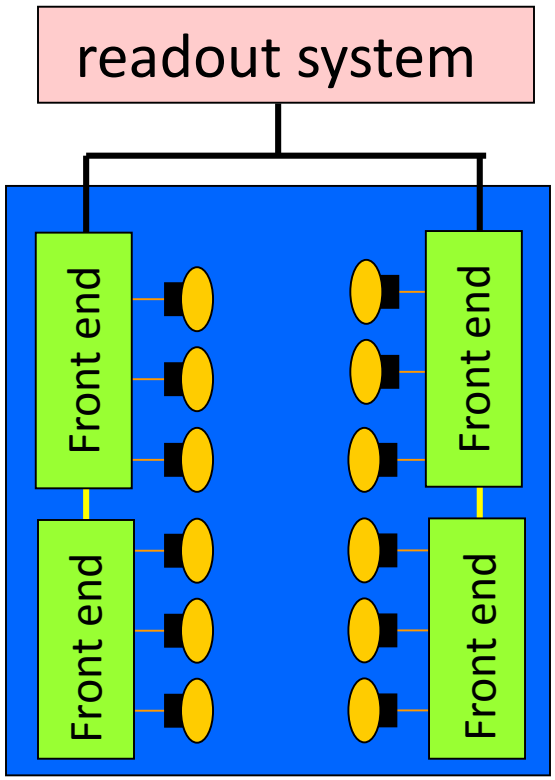
Possible problems in running the cables to each photo sensor

a) Length of the cable ~ signal degradation

b) Weight of the cable ~ cost of the detector

There are advantages to put front-end electronics modules close to photo-sensors.

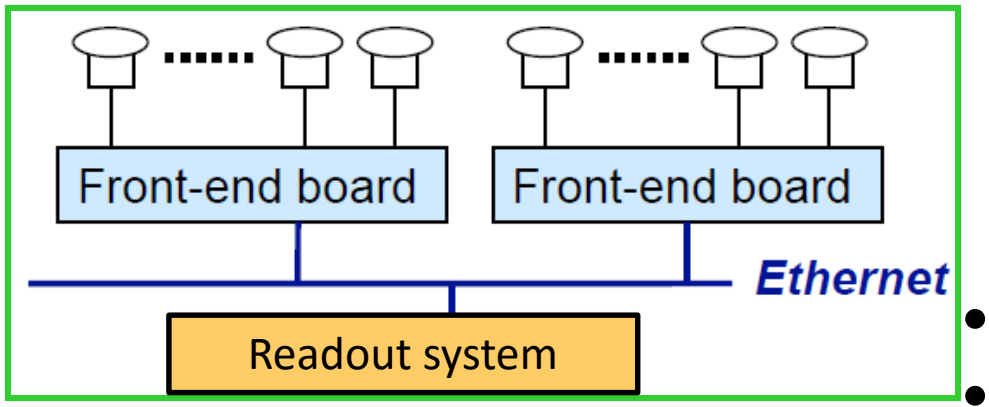
~ Putting front-end electronics modules in the water ~

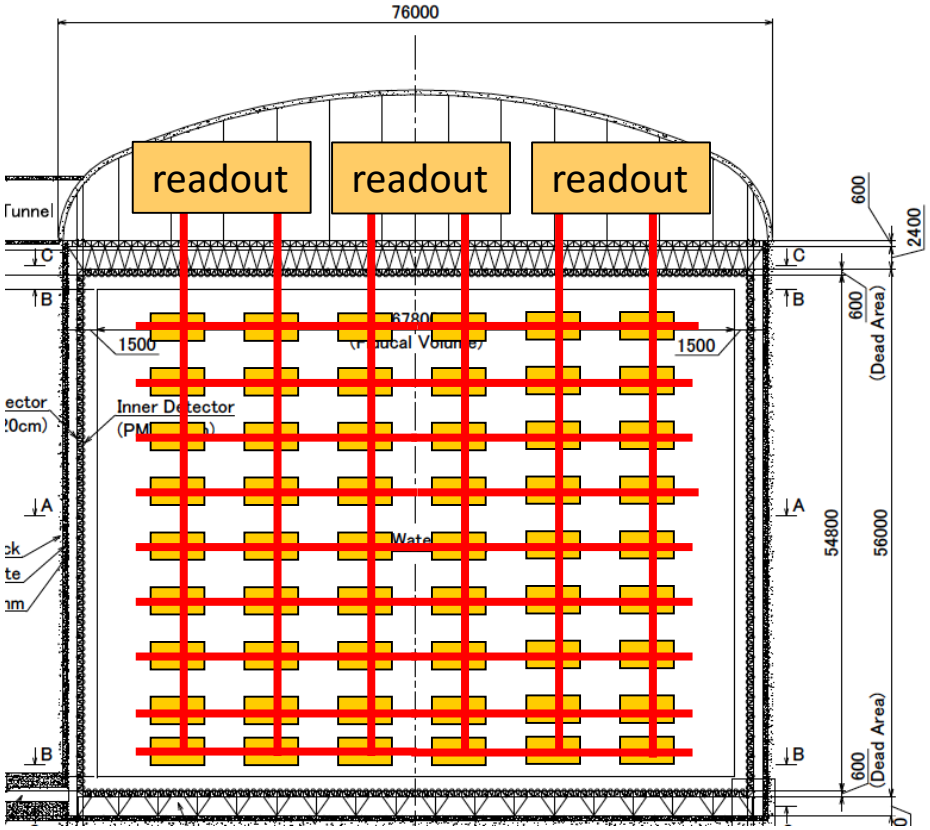


- Shorter length of the cables provides better signal quality.
- Reduce the number of cables from the tank to the top floor.
  -> reduction of weight of the cable, and cost of structure.

Further reduction of the cables is possible if data transfer lines from front-end modules are connected each other.

Possible front-end electronics module connections





Advantage to connect neighboring front-end boards each other

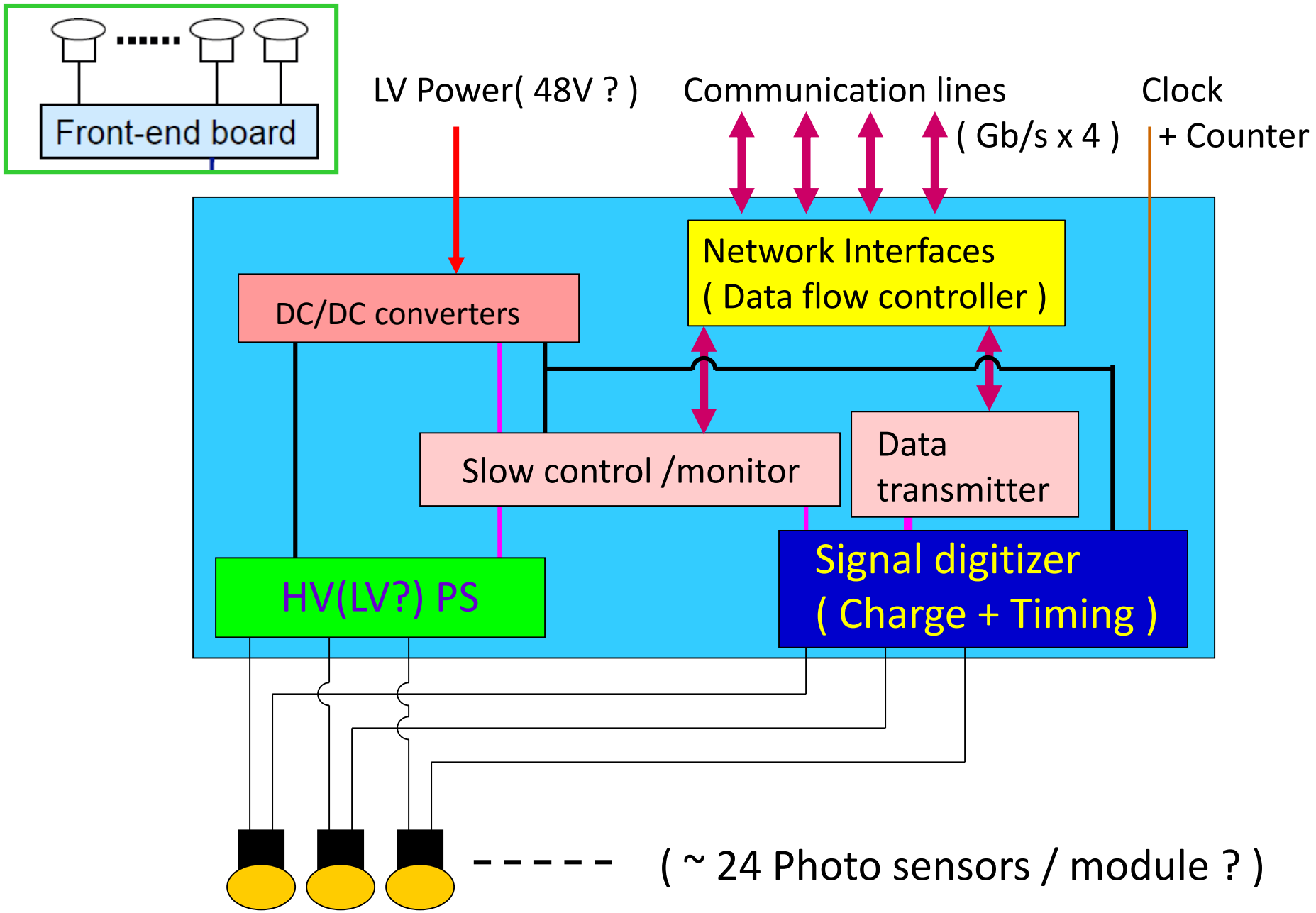
- Reduce total length of the cables
- Avoid single point failure

Usually, data collected by a module are transferred to the upper module (vertically)

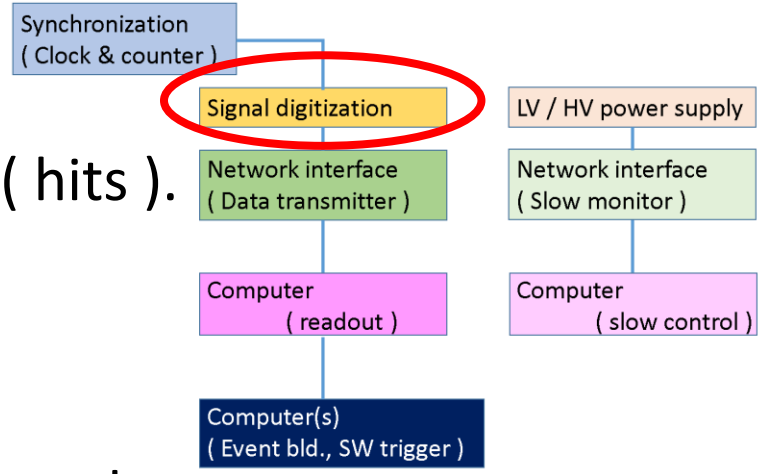
If one module failed, transfer data to the other module instead of the failed module (horizontally).

Data rate at the upper modules has to be enough smaller than maximum bandwidth.

Schematic diagram of the front-end module



Signal digitization ~ requirements ~



- ***Dark noise*** dominates the input signal (hits).
  Expected dark rate is ***5 ~ 10 kHz***.

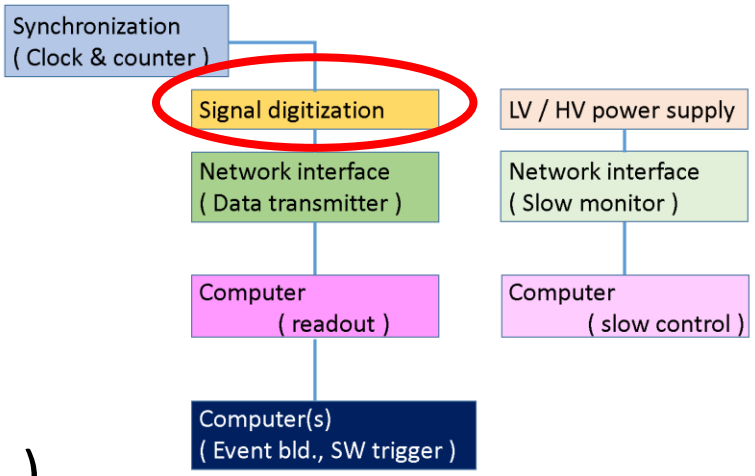
- ***Low occupancy for low energy events***.
  O(<1%) for typical solar neutrino events
  and background gamma-ray events.

- ***High energy event*** (mainly Cosmic ray muons) rate is rather low.
  Depend on the location of the detector but ***<< 100Hz***.

- Geometrical distribution of hit sensors for an event is rather broad.

- ***Possibility to have repeated hits in a channel is quite small.***
  After pulse from a photo sensor, signal reflections etc.
  O(1μs) of single channel dead-time is acceptable.
- All the modules (TDCs) has to be synchronized.

Signal digitization ~ requirements ~



~ Some parameters ~

- Self triggering for each channel
- High Sensitivity for single p.e.
  - Discriminator threshold
    ~ ¼ p.e. *) (well below 1 p.e.)
- Processing speed/hit (channel dead-time)
  ~ 1 μsec / hit
- Charge dynamic range
  0.1 ~ 1250 p.e. (0.2 ~ 2500 pC)
- Charge resolution
  ~ 0.05p.e. (< 25 p.e.) in RMS
- Timing LSB
  ~ 0.52 ns
- Timing resolution
  0.3ns (@1 p.e.) in RMS
  0.2ns (> 5 p.e.) in RMS

*) QBEE : ¼ p.e. ~ 3 mV

Water tight chassis

Suggested design (from one company)

SUS 316L (or 304) + Urethane seal

Thickness of the surface plates **~ 4mm**

Entire chassis is (better) to be filled with silicon or the other material (like R3600 PMT base)

Assuming 500mm x 500mm x 75mm (d = 4mm)

(VME 9U board : 360 mm x 340mm)

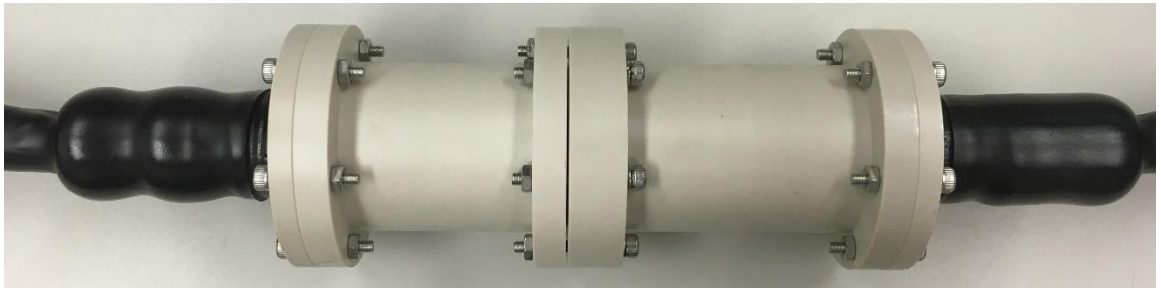
Chassis	~ 20 kg
Filler	~ 20 kg
Elec. components	~ 3 kg
Total	***~ 43 kg !?***

This may be bit heavy to handle, but possible to install.

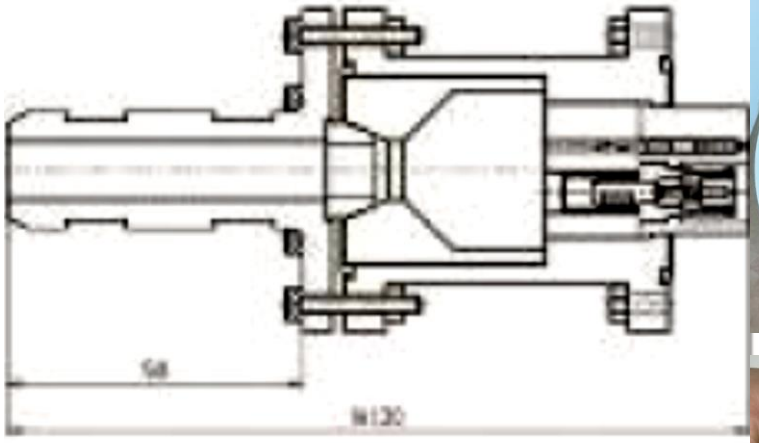
(Weight of the photo sensor with the protection cover is almost comparable.)

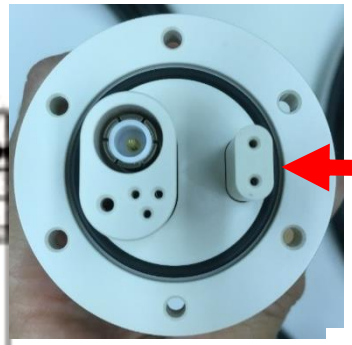
Composite connector R&D

R&D of the HV(8kV) + LV (signal + control) water tight connector.



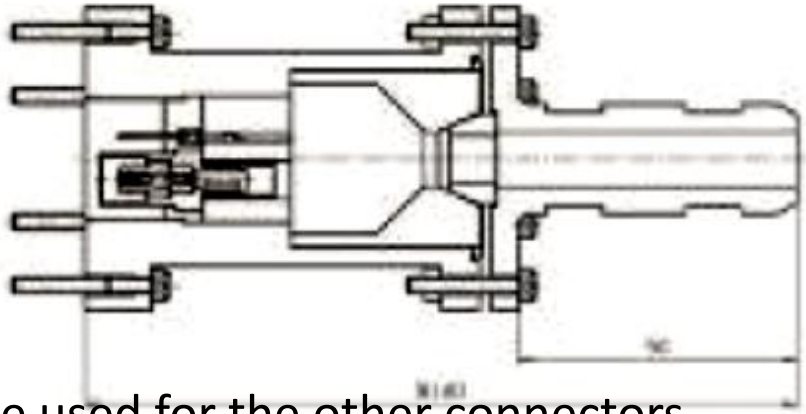
(diameter is ~ 50 mm)





HV (8KV) lines

Control lines
and HPD signal (COAX)

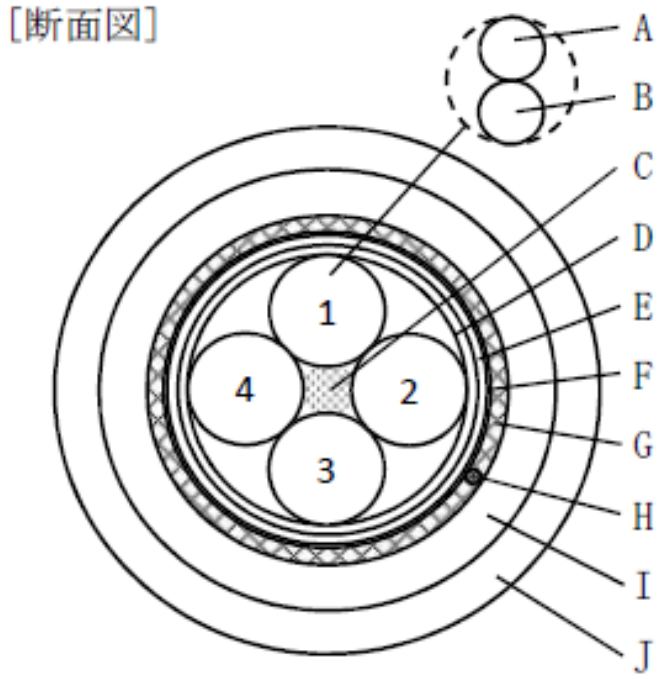


Design of the outer shell is universal and can be used for the other connectors,
Ethernet (RJ45), optical fibers and power supplies.

Pressure tolerant Ethernet cable

Usual Ethernet cable can not be used in the water
because the compressed cable can not transmit
the differential signals properly.

Drawing of the pressure-tolerant Ethernet cable
was prepared by a company.

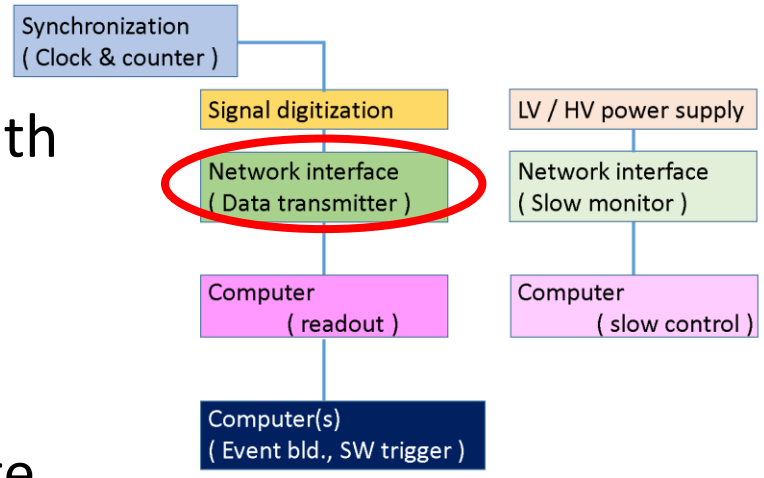


We have asked to produce this cable
(~ 200m)
and perform pressure tolerance test
using a small pressure vessel
from April.

cable weight : ~ 90g / m

Network interface

Expected data rate and required bandwidth



Assumption

24 channels / board

6 bytes / hits

10kHz photo sensor dark rate

Nominal data rate

10 kHz x 6 bytes = 60 kBytes/s/channel

-> 24 channels * 60 kBytes/s ~ ***1.5 MBytes/s***

Considering fluctuation

(high dark rate tube > 100 kHz)

If there are two high rate tubes (@ 100 kHz)

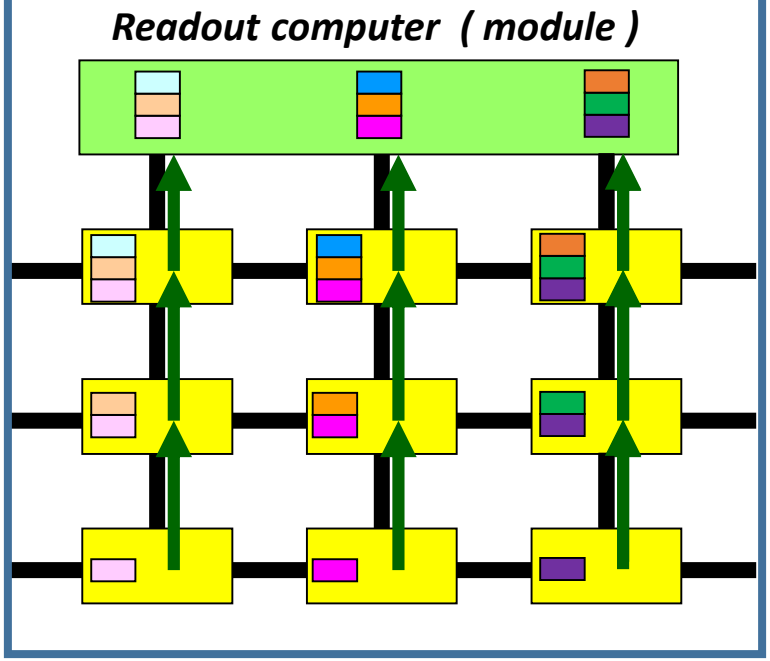
100kHz x 6 bytes * 2 channels = 1.2 MBytes / s

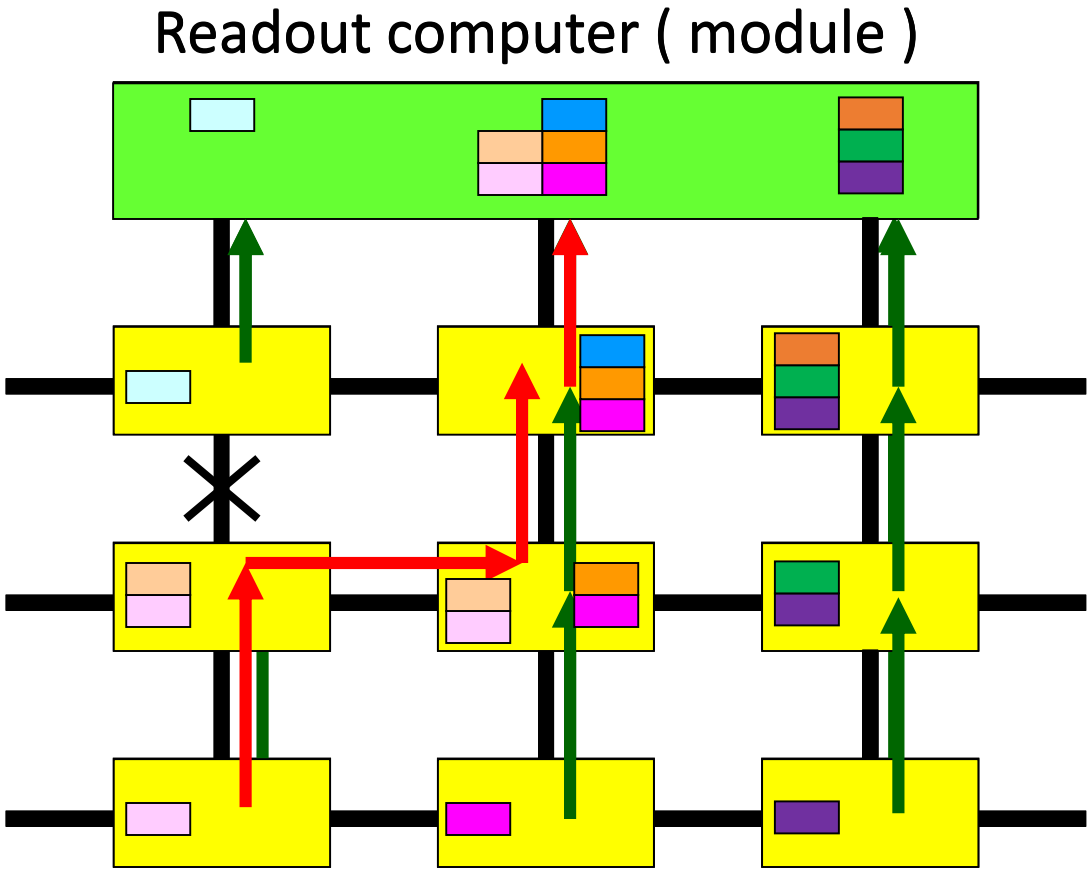
→ ***~2.5 MBytes/s/board*** seems to be sufficient under normal situation

Fault tolerant data transfer

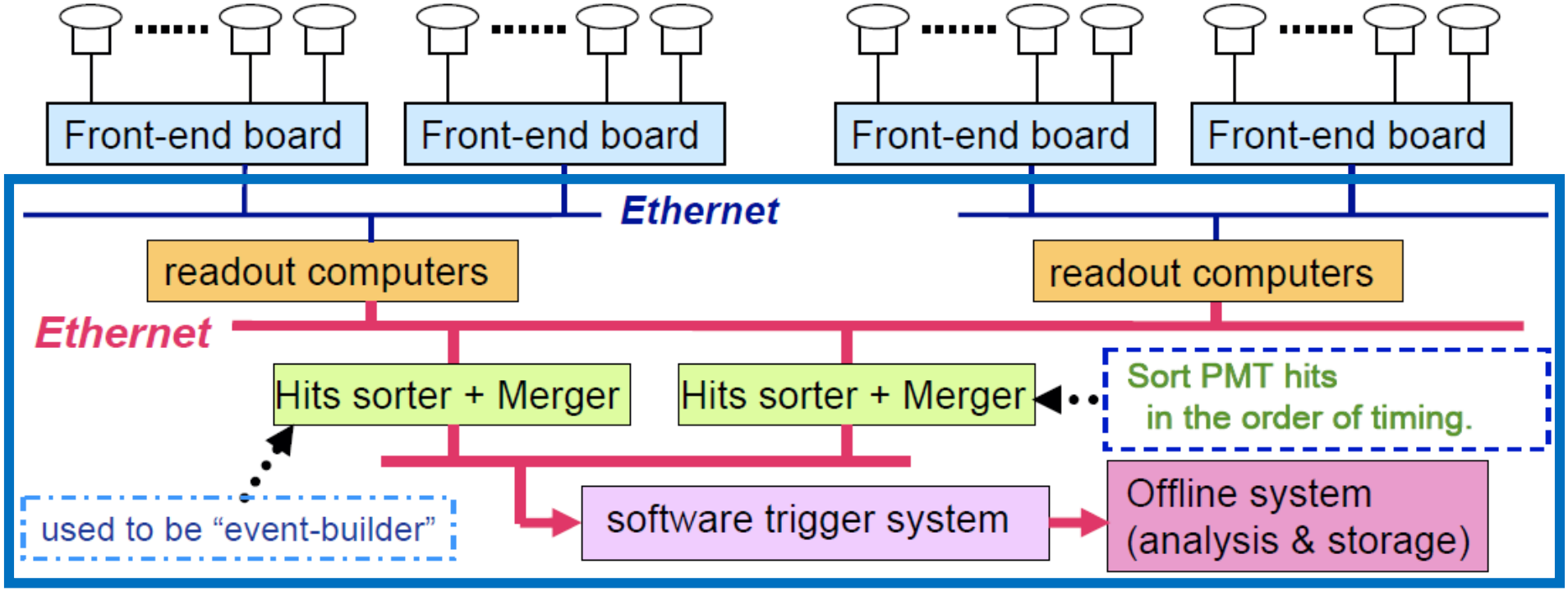
Considering to connect modules and relay the data.
In order to eliminate single point failure,
mesh type connection and possible implementation
of the `data flow' control methods are being studied.

Possible module connections



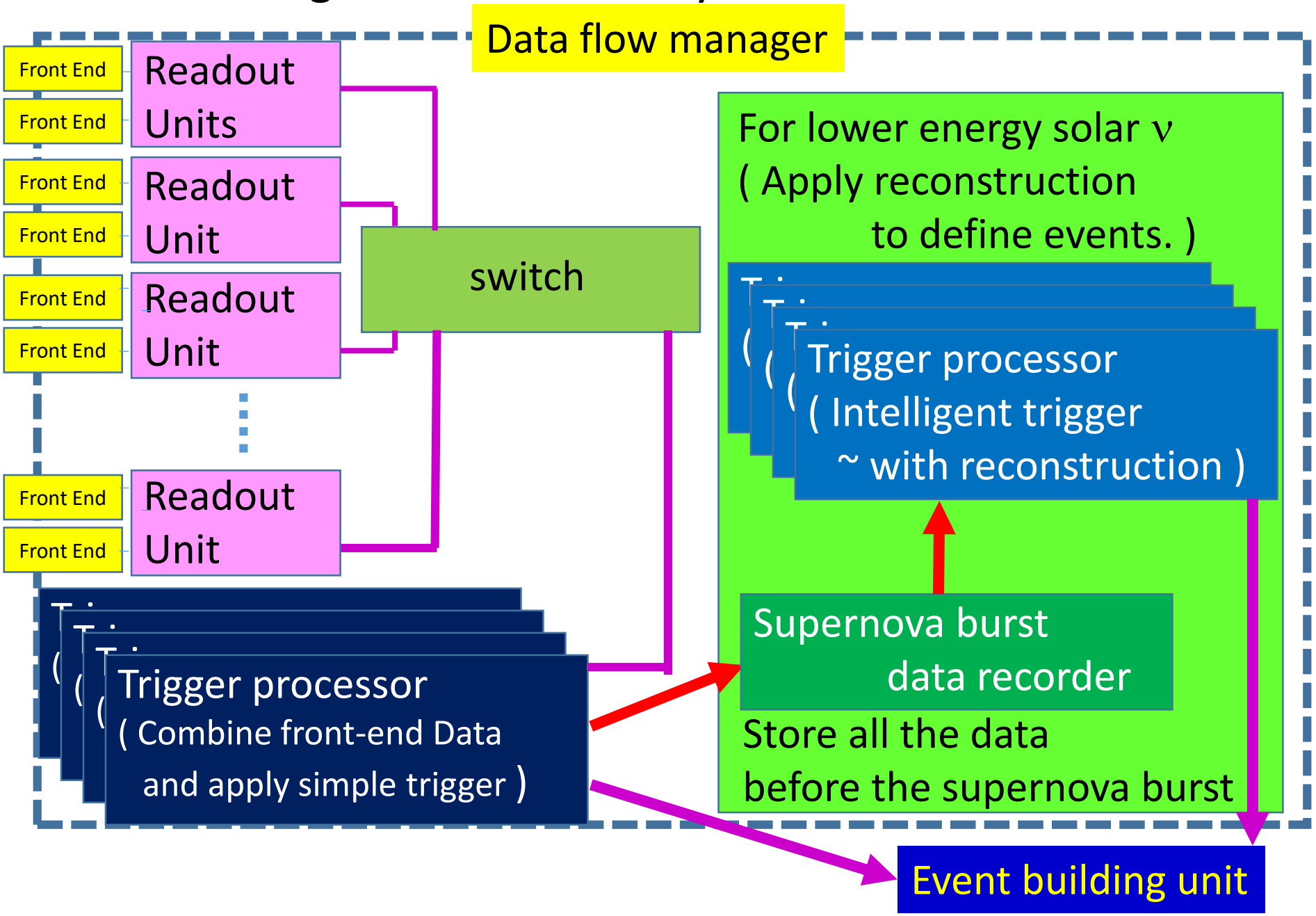


DAQ ~ readout & software trigger system ~



- *UK Group is working on to design implementations*
  - DAQ Framework evaluation including custom framework
  - Scalable architecture
  - Sophisticated algorithms are being develop
    to improve the sensitivity to low energy events

Schematic diagram of the DAQ system



Software trigger system

Simple majority trigger has been used in SK4

Count # of hits within 200ns and determine the trigger

~ similar to the hardware trigger in SK1~3

Currently, the lowest threshold is 31 hits in 200ns in SK4.

# of dark hits is 8.5 ~ 9 hits in 200ns

Energy threshold is 3.5 ~ 4 MeV

~ (31 – 9) [hits] / 6 [hits/MeV]

Trigger rate is ~ 12 kHz @ 31 hits in 200ns

(Most of them concentrate in the detector surface.)

In order to lower the threshold,

another “intelligent” software trigger

with event reconstruction

have been developed in SK.

Software trigger system

Differences between SK and HK

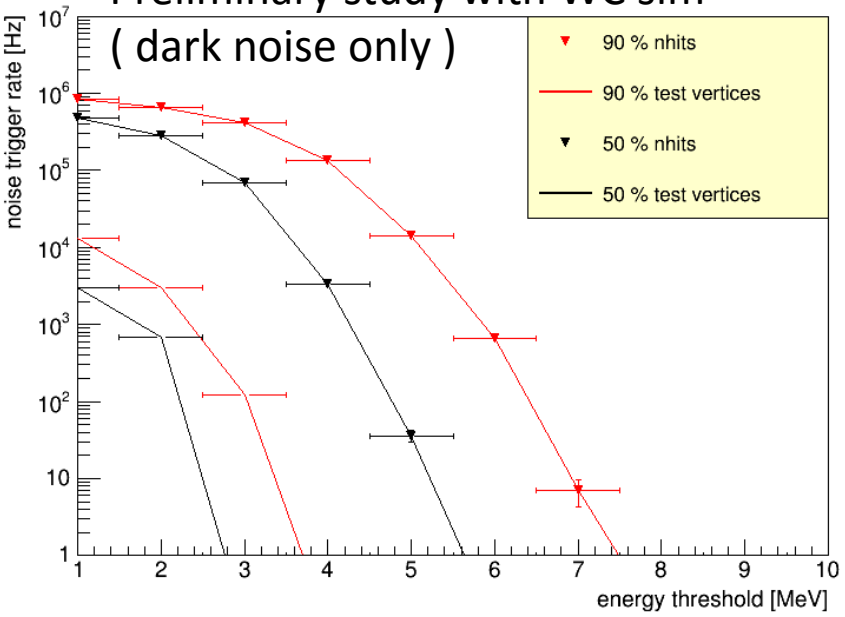
	SK	HK
Trigger window	200ns	400ns
Dark rate	3 ~ 4 kHz	< 8.4 kHz
# of PMTs	~11,100	~40,000
Expected # of dark hits in trigger window	8.5 ~ 9 hits	~135 hits
# of hits / MeV	6	10 ~ 12

In HK, random dark noises
produce fake events.
O (> several kHz) @ 5MeV

Possible to handle
but need to be reduced.

1) Offline reduction
2) (Semi-) Online reduction

Preliminary study with WC sim
(dark noise only)



Study of the intelligent trigger system

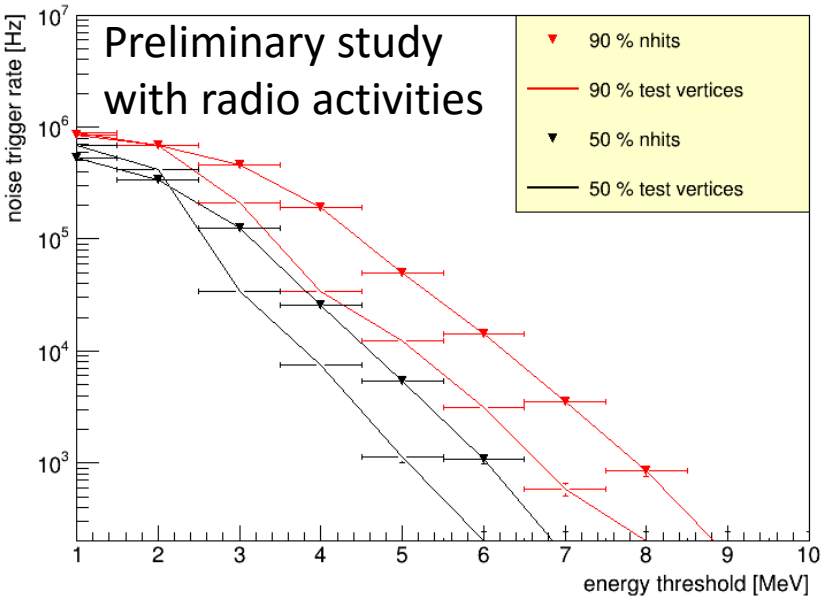
Most of the background events (in SK)
seems to be coming from the fringe region of the detector.
Originated from the radio activities
in the photo-sensor, covers, support structures
and/or surrounding rocks.

→ Possible to reject by reconstructing the event vertex

Fast vertex trigger (UK DAQ group)

Pre-calc light propagation to PMT from grid of test vertices.

- Adjust PMT hit times by ToF for each vertex
- Apply NHits type trigger (10 ns window)
- Trigger issued if any vertex above threshold
- Implement on Graphical Processing Unit



Possible implementation of BONSAI on GPU is under study by Swiss group. (BONSAI = reconstruction software for SK low energy events)

Summary

Experience in Super-Kamiokande is useful in designing the system.

R&D of individual components for Hyper-Kamiokande
are going on to maximize the detector performance
and to reduce the cost.

Rough estimate of the cost

Digitization module (QTC+TDC case)
~ 6,000 yen per channel

High voltage + peripheral (incl. communication)
~ 10,000 yen per channel

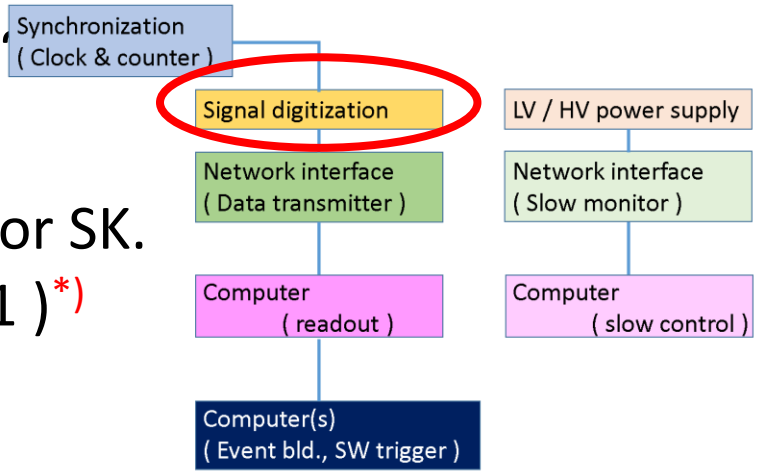
Chassis + connectors
~ 10,000 yen per channel

Total cost of the electronics part ~ 13 oku-yen (for 50k ch.)

Total cost of the DAQ part

Expect to rent from company (several year contracts)
Estimated to be ~ 1 oku yen/year for 5 years contract.

Signal digitization ~ Possible designs ‘



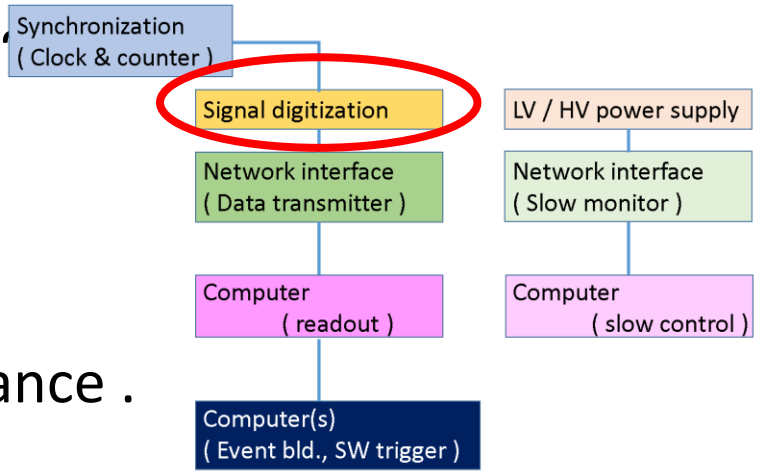
1) QTC + TDC

Similar to the current electronics for SK.
SK uses custom build QTC (CLC101)*)

QTC has 3 channels in one chip.
Each channel has three ranges to cover wide dynamic range.
Different gains for different ranges
Outputs from all three ranges
are individually recorded by external TDC.
Process rule of QTC is CMOS 0.35 μm and
still possible to reproduce the same chip.
(As far as the production facility of the company
is available.)

Est. price **@ ~ ¥ 6,000 / chip** for 100,000 chips
(¥ 2000 / channel)

Signal digitization ~ Possible designs ‘



1) QTC + TDC

FPGA based TDC is proposed.

Recent low cost FPGA is reported to have sufficient performance .

(FPGA-based “Wave Union” TDC by Jin-Yuan Wu, Fermilab)

32 ch. TDC was implemented in *$75 FPGA* chip.

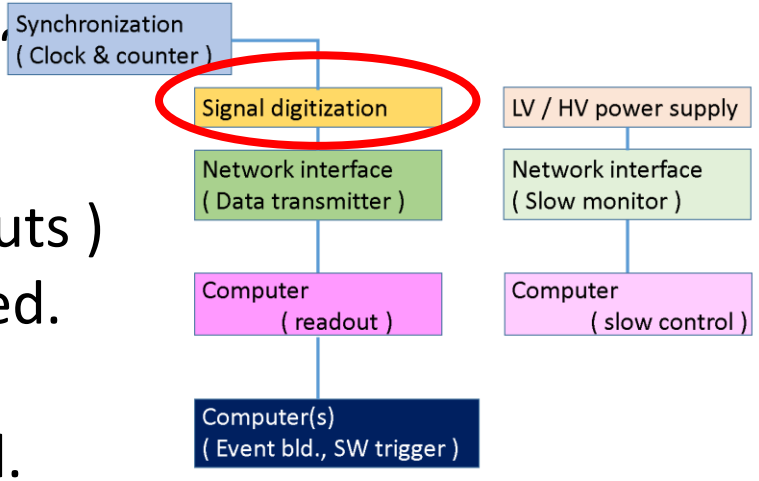
Estimated costs of ***these two core components***:

Assuming 24 ch. / board,

8 QTCs + 4 FPGAs (32ch.) are necessary.

~ ¥5,000 / channel for 100k sensors.

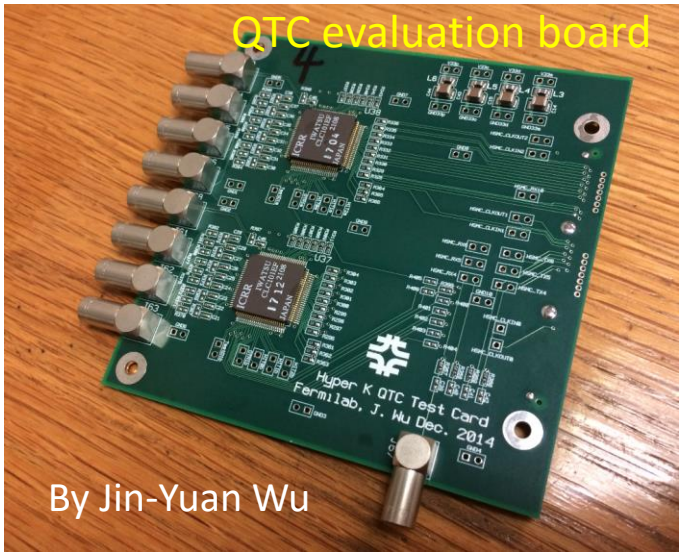
Signal digitization ~ Possible designs ~

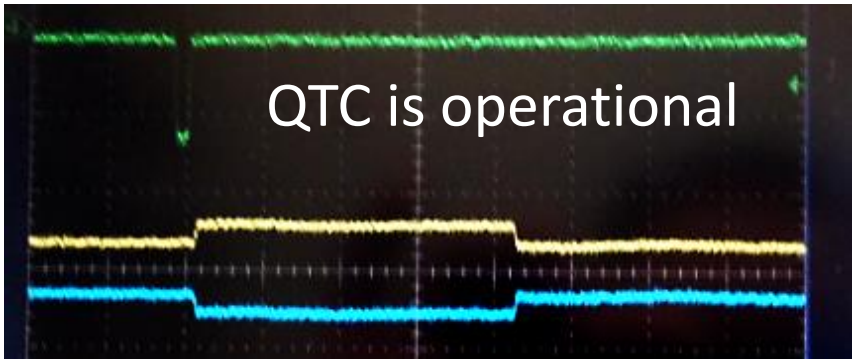


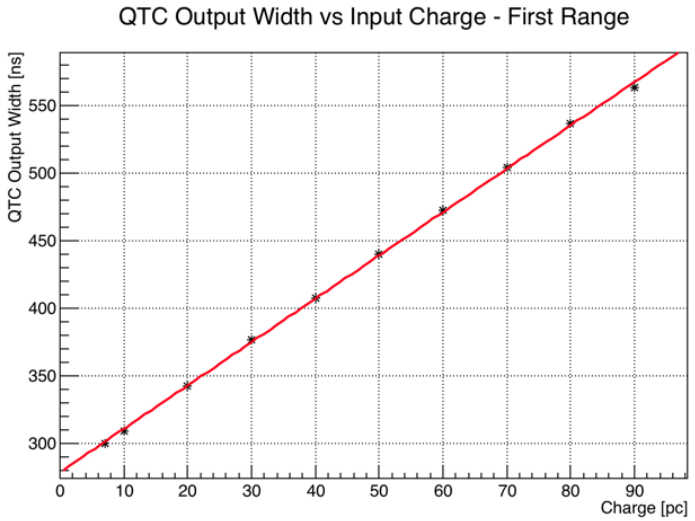
1) QTC + TDC

QTC test board (2 QTCs = 6 ch inputs)
was designed and fabricated.
(FNAL/BU)

This board works with FPGA board.

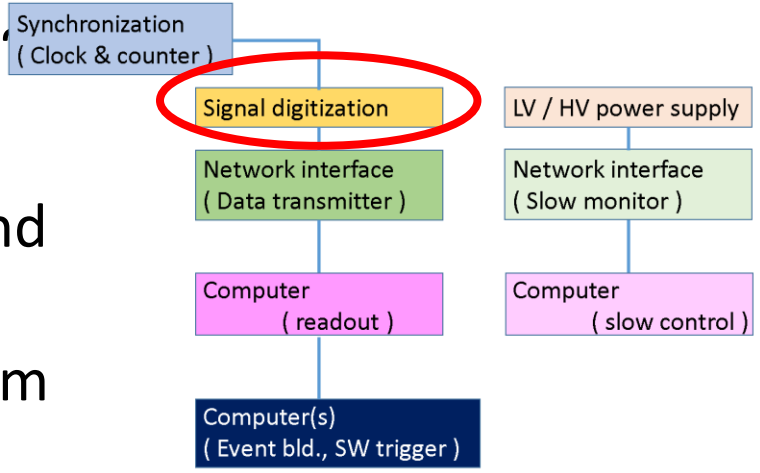






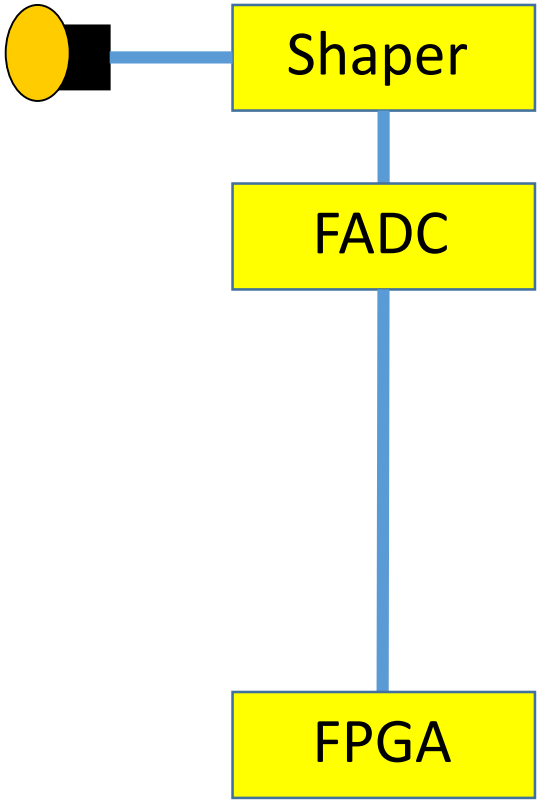
Evaluation with FPGA-TDC
has been started.

Signal digitization ~ Possible designs



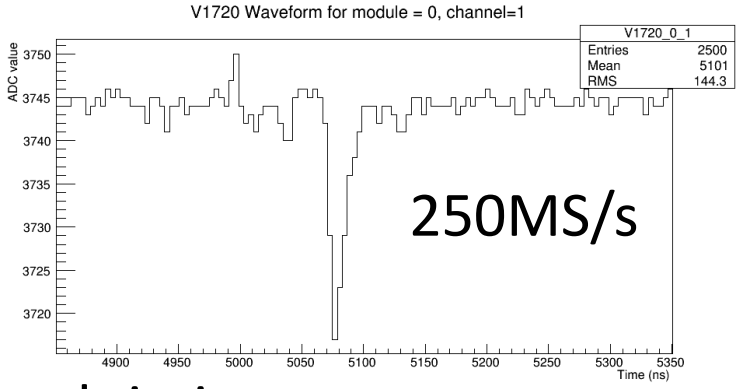
2) Shaper + FADC (+ FPGA)

Another proposal to use shaper and FADC to record waveform and process the digitized wave form with FPGA.



Sampling frequency 100 ~ 500MHz

resolution 12 ~ 14 bits

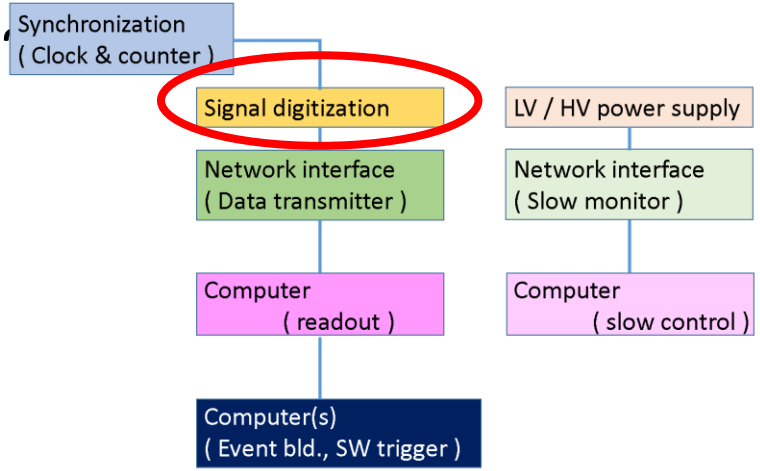


Fit signal timing

Integrate charge

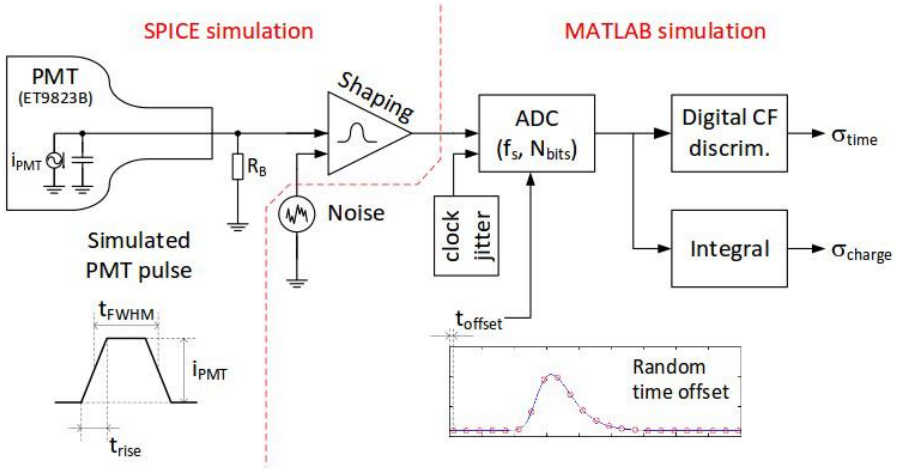
(Canada & Poland)

Signal digitization ~ Possible designs ~



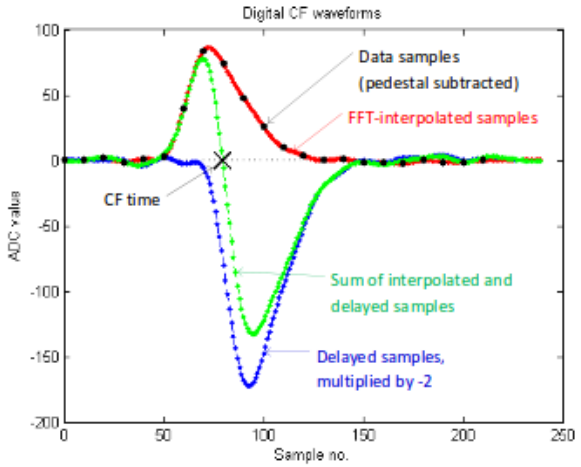
2) Shaper + FADC (+ FPGA)

Design of the shaper with FADC using simulation.

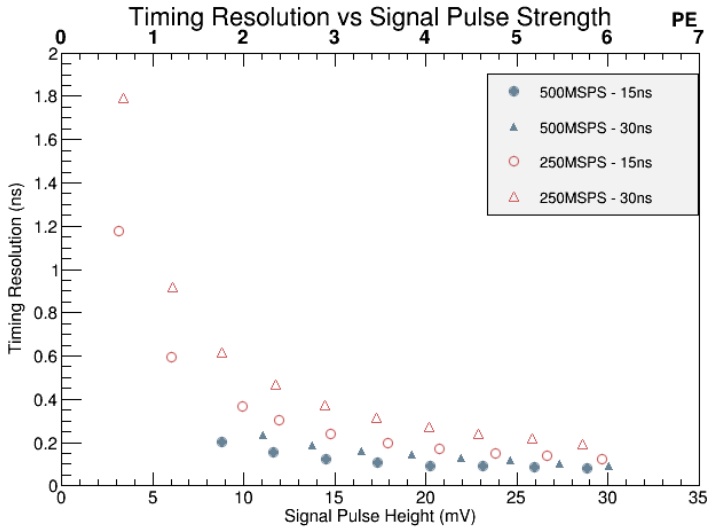


Designed shaper was evaluated using existing FADC module and wave form generator.

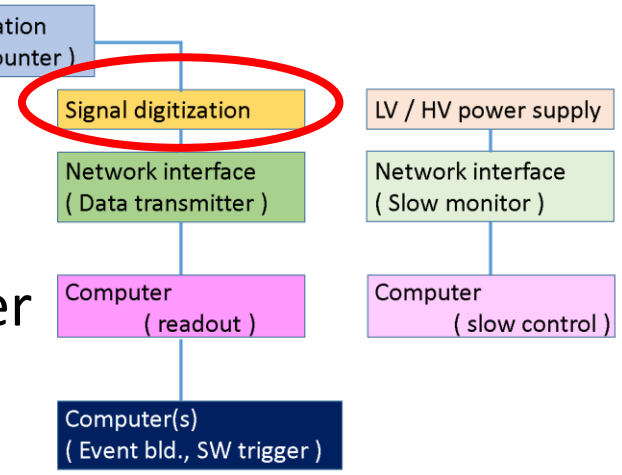
Digital Constant-Fraction



T resolution vs charge



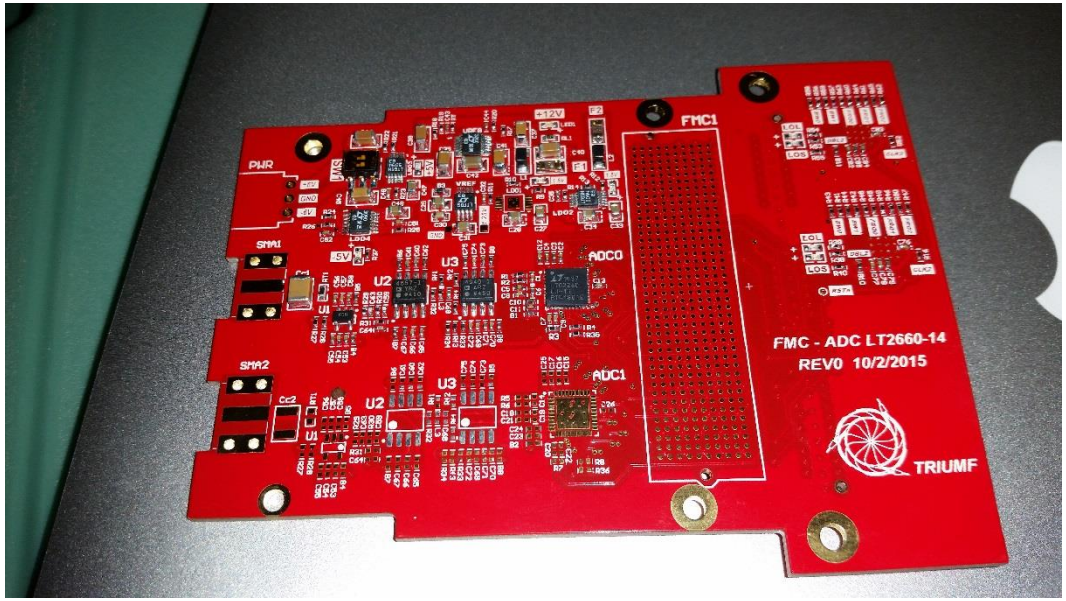
Signal digitization ~ Possible designs ‘



2) Shaper + FADC (+ FPGA)

Based on reasonable benchtop tests,
a prototype board with 100MHz digitizer
with shaper was designed.
Use low power shaper amplifiers
and low power 14bit 100MSPS ADC.

PCBs are assembled
and firmware being
prepared.



Also, another possibility to use capacitor array chip (DRS)
has been proposed and under study. (Switzerland)

Cost of the front end module
(digitization board only)

Rough cost estimate (~ QTC + TDC case ~)

QTC (CLC 101)

Est. price**@ ~ ¥6,000 / chip** (¥2,000 / channel)

TDC (FPGA CYCLONE III (EP3C25F324C6N))

Est. price**@ ~ ¥10,000 / chip** (¥300 / channel)

Assuming 24 ch./ board,

8QTCs + 4 FPGAs (32ch.) are necessary.

¥6,000 x 8 + ¥10,000 x 4

FPGA for communication, other parts etc…

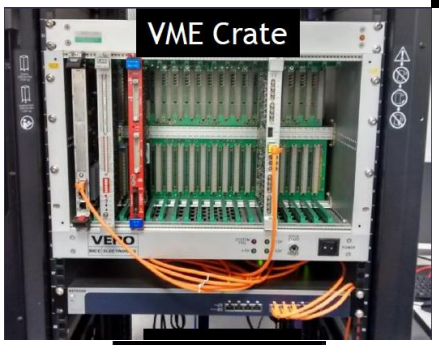
~¥50,000 / board

Total ~ ¥150,000 ~ ***¥ 6,000 / channel***

Evaluation of the hardware for the DAQ system

Investigation of GPUs for triggering

Test hardware set-up



Gb switch

2x Dell Xeon Servers

Struck SIS3316
16 Channel VME Digitizer

Motorola MVME 5500